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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b70l7b9ecx

List of tables

Table 2. SPC564Bxx and SPC56ECxx family comparison[1]

Feature		SPC564B64		SPC56EC64			SPC564B70		SPC56EC70			SPC564B74		SPC56EC74		
Package		LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256
CPU		e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h		
Execution speed[2]		Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]		
Code flash memory		1.5 MB					2 MB					3 MB				
Data flash memory		4 x16 KB														
SRAM		128 KB		192 KB			160 KB		256 KB			192 KB		256 KB		
MPU		16-entry														
eDMA[4]		32 ch														
10-bit ADC		27 ch	33 ch	27 ch	33 ch		27 ch	33 ch	27 ch	33 ch		27 ch	33 ch	27 ch	33 ch	
	dedicated[5], [6]															
	shared with 12-bit ADC[7]	19 ch														
12-bit ADC		5 ch	10 ch	5 ch	10 ch		5 ch	10 ch	5 ch	10 ch		5 ch	10 ch	5 ch	10 ch	
	dedicated[8]															
	shared with 10-bit ADC[7]	19 ch														
CTU		64 ch														
Total timer I/O[9] eMIOS		64 ch, 16-bit														
SCI (LINFlexD)		10														
SPI (DSPI)		8														
CAN (FlexCAN)[10]		6														

Table 3. SPC564Bxx and SPC56ECxx series block summary (continued)

Block	Function
LinFlexD (Local Interconnect Network Flexible with DMA support)	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Non-Maskable Interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection
Nexus Development Interface (NDI)	Provides real-time development capabilities for e200z0h and e200z4d core processor
Periodic interrupt timer/ Real Time Interrupt Timer (PIT_RTI)	Produces periodic interrupts and triggers
Real-time counter (RTC/API)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode). Supports autonomous periodic interrupt (API) function to generate a periodic wakeup request to exit a low power mode or an interrupt request
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AutoSAR and operating system tasks
Semaphores	Provides the hardware support needed in multi-core systems for sharing resources and provides a simple mechanism to achieve lock/unlock operations via a single write access.
Wake Unit (WKPU)	Supports external sources that can generate interrupts or wakeup events, of which can cause non-maskable interrupt requests or wakeup events.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[15]	PB[2]	PC[13]	PI[1]	PE[7]	PH[8]	PE[2]	PE[4]	PC[4]	PE[3]	PH[9]	PI[4]	PH[11]	PE[14]	PA[10]	PG[11]	A
B	PH[13]	PC[14]	PC[8]	PC[12]	PI[3]	PE[6]	PH[5]	PE[5]	PC[5]	PC[0]	PC[2]	PH[12]	PG[10]	PA[11]	PA[9]	PA[8]	B
C	PH[14]	VDD_HV_A	PC[9]	PL[0]	PI[0]	PH[7]	PH[6]	VSS_LV	VDD_HV_A	PA[5]	PC[3]	PE[15]	PG[14]	PE[12]	PA[7]	PE[13]	C
D	PG[5]	PI[6]	PJ[4]	PB[3]	PK[15]	PI[2]	PH[4]	VDD_LV	PC[1]	PH[10]	PA[6]	PI[5]	PG[15]	PF[14]	PF[15]	PH[2]	D
E	PG[3]	PI[7]	PH[15]	PG[2]	VDD_LV	VSS_LV	PK[10]	PK[9]	PM[1]	PM[0]	PL[15]	PL[14]	PG[0]	PG[1]	PH[0]	VDD_HV_A	E
F	PA[2]	PG[4]	PA[1]	PE[1]	PL[2]	PM[6]	PL[1]	PK[11]	PM[5]	PL[13]	PL[12]	PM[2]	PH[1]	PH[3]	PG[12]	PG[13]	F
G	PE[8]	PE[0]	PE[10]	PA[0]	PL[3]	VSS_HV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	PK[12]	VDD_HV_B	PI[13]	PI[12]	PA[3]	G
H	PE[9]	VDD_HV_A	PE[11]	PK[1]	PL[4]	VSS_LV	VSS_LV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	PK[13]	VDD_HV_A	VDD_LV	VSS_LV	PI[11]	H
J	VSS_HV	VRC_CTRL	VDD_LV	PG[9]	PL[5]	VSS_LV	VSS_LV	VSS_LV	VSS_HV	VSS_HV	VSS_HV	PK[14]	PD[15]	PI[8]	PI[9]	PI[10]	J
K	RESET	VSS_LV	PG[8]	PC[11]	PL[6]	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_LV	VDD_LV	PM[3]	PD[14]	PD[13]	PB[14]	PB[15]	K
L	PC[10]	PG[7]	PB[0]	PK[2]	PL[7]	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_LV	VDD_LV	PM[4]	PD[12]	PB[12]	PB[13]	VDD_HV_ADC1	L
M	PG[6]	PB[1]	PK[4]	PF[9]	PK[5]	PK[6]	PK[7]	PK[8]	PL[8]	PL[9]	PL[10]	PL[11]	PB[11]	PD[10]	PD[11]	VSS_HV_ADC1	M
N	PK[3]	PF[8]	PC[6]	PC[7]	PJ[13]	VDD_HV_A	PB[10]	PF[6]	VDD_HV_A	PJ[1]	PD[2]	PJ[5]	PB[5]	PB[6]	PJ[6]	PD[9]	N
P	PF[12]	PF[10]	PF[13]	PA[14]	PJ[9]	PA[12]	PF[0]	PF[5]	PF[7]	PJ[3]	PI[15]	PD[4]	PD[7]	PD[8]	PJ[8]	PJ[7]	P
R	PF[11]	PA[15]	PJ[11]	PJ[15]	PA[13]	PF[2]	PF[3]	PF[4]	VDD_LV	PJ[2]	PJ[0]	PD[0]	PD[3]	PD[6]	VDD_HV_ADC0	PB[7]	R
T	PJ[12]	PA[4]	PK[0]	PJ[14]	PJ[10]	PF[1]	XTAL	EXTAL	VSS_LV	PB[9]	PB[8]	PI[14]	PD[1]	PD[5]	VSS_HV_ADC0	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Notes:
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], PA[3], PM[3], and PM[4].
2)Availability of port pin alternate functions depends on product selection.

Figure 4. 256-pin BGA configuration

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ADC0_S[9]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	64	80	T6
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ADC0_S[10]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	65	81	R6
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	66	82	R7
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	67	83	R8
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	68	84	P8
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	69	85	N8
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	S	Tristate	70	86	P9

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX —	SIUL eMIOS_0 LINFlexD_8 —	I/O I/O O —	S	Tristate	172	196	C5
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKPU[24] LIN8RX	SIUL eMIOS_0 — — WKPU LINFlexD_8	I/O I/O — — I I	S	Tristate	171	195	A4
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX —	SIUL eMIOS_0 LINFlexD_9 —	I/O I/O O —	S	Tristate	170	194	D6
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKPU[23] LIN9RX	SIUL eMIOS_0 — — WKPU LINFlexD_9	I/O I/O — — I I	S	Tristate	169	193	B5
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	M/S	Tristate	143	167	A12
PI[5]	PCR[133]	AF0 AF1 AF2 AF3 ALT4	GPIO[133] E1UC[29] SCK_4 CS2_5 CS2_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O O O	M/S	Tristate	142	166	D12
PI[6]	PCR[134]	AF0 AF1 AF2 AF3 ALT4	GPIO[134] E1UC[30] CS0_4 CS0_5 CS0_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O I/O I/O	S	Tristate	11	11	D2

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PJ[3]	PCR[147]	AF0 AF1 AF2 AF3 —	GPIO[147] CS1_5 CS1_6 CS1_7 ADC0_S[27]	SIUL DSPI_5 DSPI_6 DSPI_7 ADC_0	I/O O O O I	S	Tristate	71	87	P10
PJ[4]	PCR[148]	AF0 AF1 AF2 AF3	GPIO[148] SCK_5 E1UC[18] —	SIUL DSPI_5 eMIOS_1 —	I/O I/O I/O —	M/S	Tristate	5	5	D3
PJ[5]	PCR[149]	AF0 AF1 AF2 AF3 —	GPIO[149] — — — ADC0_S[28]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	113	N12
PJ[6]	PCR[150]	AF0 AF1 AF2 AF3 —	GPIO[150] — — — ADC0_S[29]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	112	N15
PJ[7]	PCR[151]	AF0 AF1 AF2 AF3 —	GPIO[151] — — — ADC0_S[30]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	111	P16
PJ[8]	PCR[152]	AF0 AF1 AF2 AF3 —	GPIO[152] — — — ADC0_S[31]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	110	P15
PJ[9]	PCR[153]	AF0 AF1 AF2 AF3 —	GPIO[153] — — — ADC1_S[8]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	68	P5

Table 16. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		P			I_{OL} = 1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 17. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		C			I_{OL} = 1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.7 RESET electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 6. Start-up reset requirements

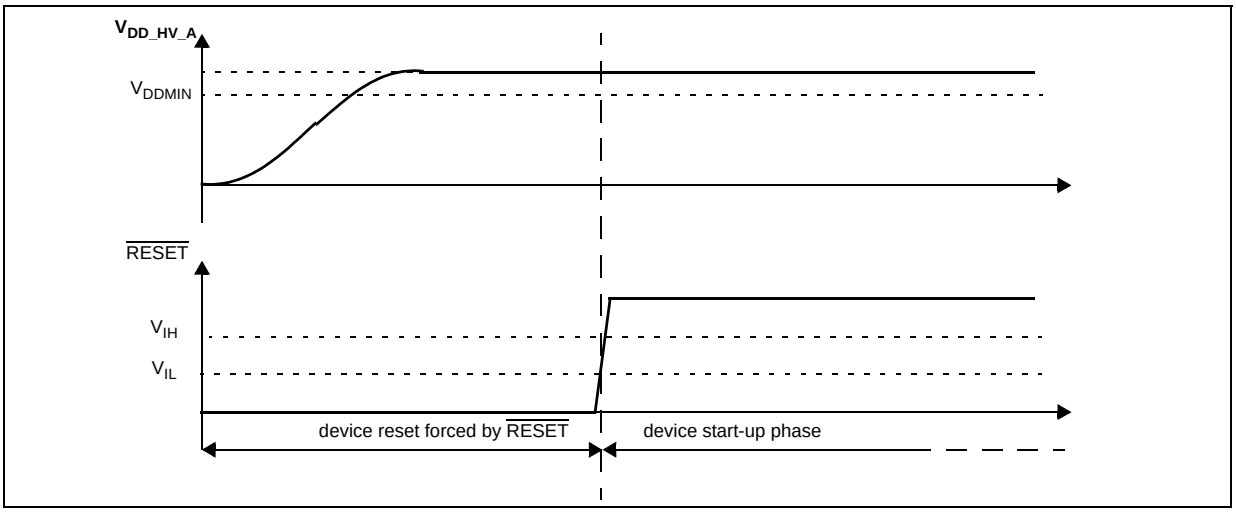


Figure 7. Noise filtering on reset signal

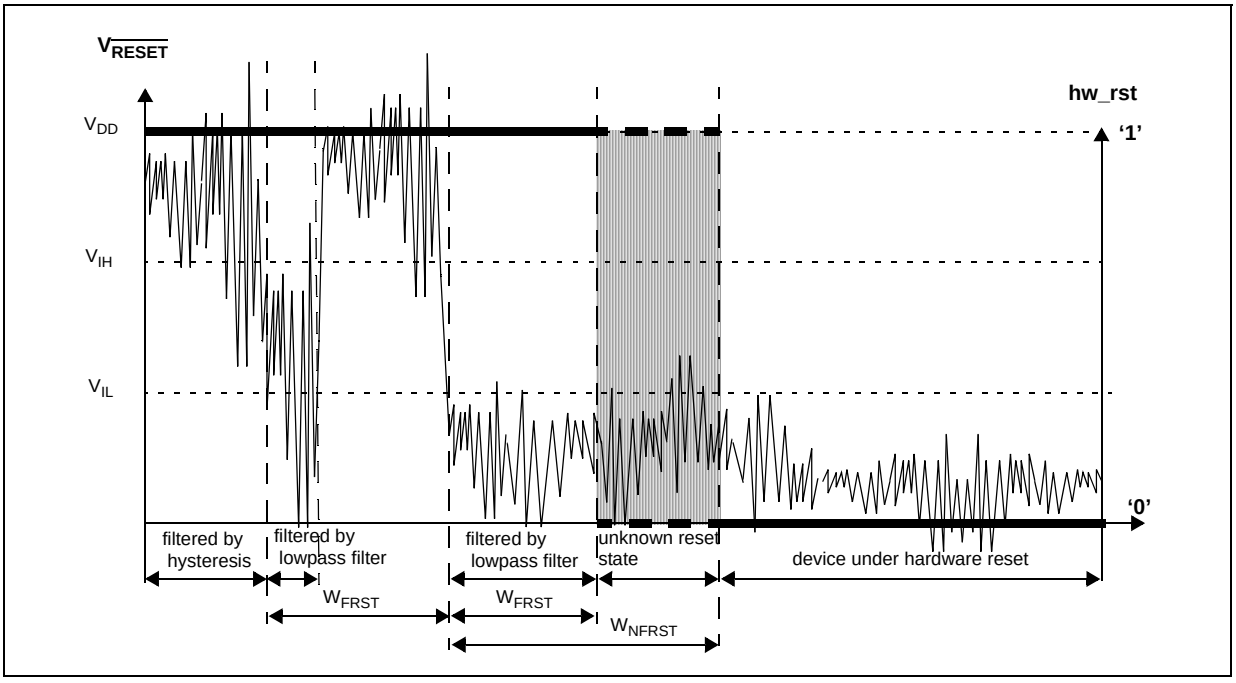


Figure 9. Low voltage monitor vs. Reset

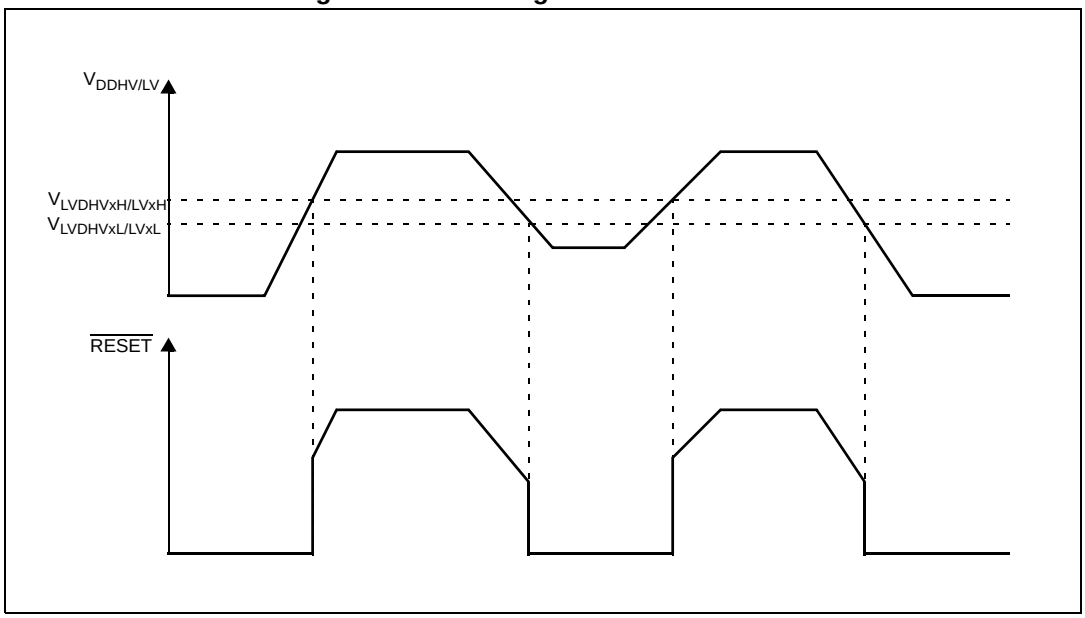


Table 24. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{PORUP}	SR	P	Supply for functional POR module	—	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold	—	1.5	—	2.6	
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold	—	2.7	—	2.85	
$V_{LVDHV3L}$	CC	T	LVDHV3 low voltage detector low threshold	—	2.6	—	2.74	
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold	—	4.3	—	4.5	
$V_{LVDHV5L}$	CC	T	LVDHV5 low voltage detector low threshold	—	4.2	—	4.4	
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold	T_A = 25 °C, after trimming	1.08	—	1.17	
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.17	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.

3.9 Low voltage domain power consumption

Table 25 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

3.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz low power internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 41. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		untrimmed, across temperatures	84	—	205	
I_{SIRC}[3]	CC	C	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA
T_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	+2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Variation in f_{SIRC} across temperature and fluctuation in supply voltage, post trimming	—	–10	—	+10	%

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.17 ADC electrical characteristics

3.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

Note: Due to ADC limitations, the two ADCs cannot sample a shared channel at the same time i.e., their sampling windows cannot overlap if a shared channel is selected. If this is done, neither of the ADCs can guarantee their conversion accuracies.

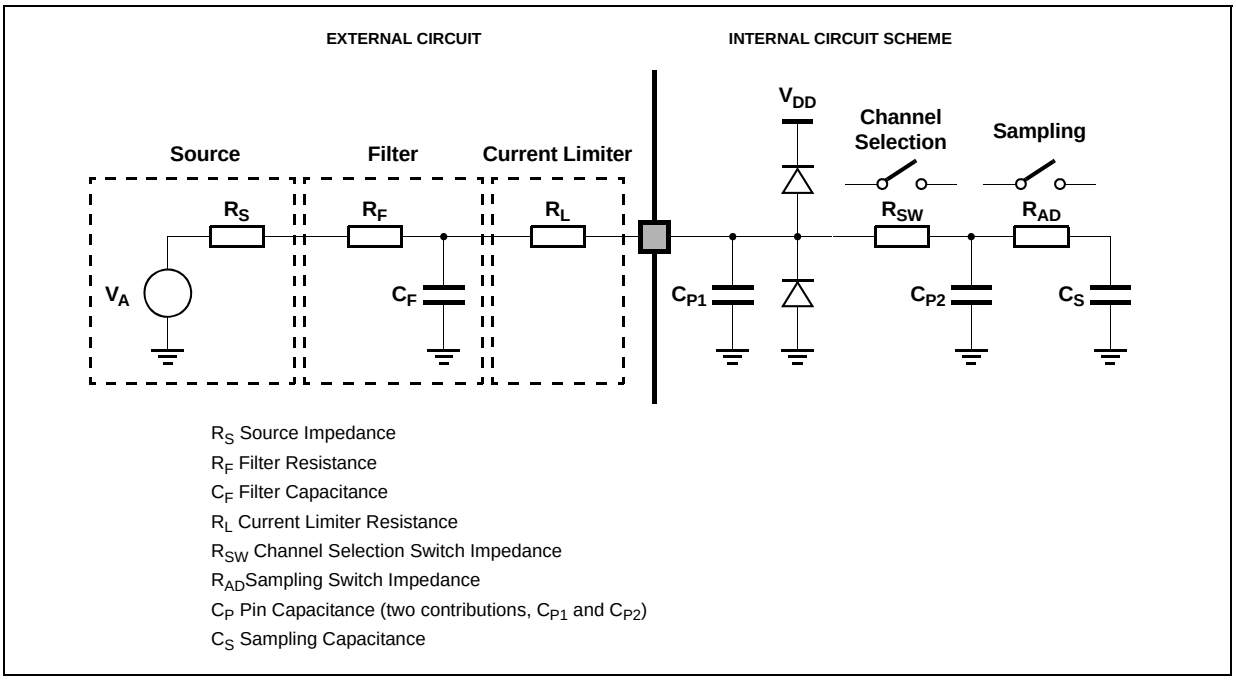
In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being CS and Cp_2 substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1MHz, with CS+Cp_2 equal to 3pF, a resistance of 330KΩ is obtained (Reqiv = 1 / (fc*(CS+Cp_2)), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on CS+Cp_2) and the sum of R_S + R_F, the external circuit must be designed to respect the following relation

Equation 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

The formula above provides a constraint for external network design, in particular on resistive path.

Figure 16. Input equivalent circuit (precise channels)



R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW} Channel Selection Switch Impedance
R_{AD}Sampling Switch Impedance
C_P Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S Sampling Capacitance

3.17.1.2 ADC electrical characteristics

Table 42. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 43. ADC conversion characteristics (10-bit ADC_0)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC0}	SR	—	Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V_{SS_HV})[2]	—	–0.1	—	0.1	V
V_{DD_ADC0}	SR	—	Voltage on VDD_HV_ADC0 pin (ADC_0 reference) with respect to ground (V_{SS_HV})	—	$V_{DD\_HV\_A}$ – 0.1	—	$V_{DD\_HV\_A}$ + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC0} – 0.1	—	V_{DD_ADC0} + 0.1	V
f_{ADC0}	SR	—	ADC_0 analog frequency	—	6	—	32 + 2%	MHz
t_{ADC0_PU}	SR	—	ADC_0 power up delay	—	—	—	1.5	µs
t_{ADC0_S}	CC	T	Sample time[4]	f_{ADC} = 32 MHz	500	—		ns
t_{ADC0_C}	CC	P	Conversion time[5],[6]	f_{ADC} = 32 MHz	0.625	—		µs
				f_{ADC} = 30 MHz	0.700	—		
C_S	CC	D	ADC_0 input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC_0 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_0 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_0 input pin capacitance 3	—	—	—	1	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	3	kΩ

Table 44. Conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
C_{P3}	CC	D	ADC_1 input pin capacitance 3	—			1.5		pF
R_{SW1}	CC	D	Internal resistance of analog source	—				1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—				2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—				0.3	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC_1 input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
INLP	CC	T	Absolute Integral non-linearity-Precise channels	No overload			1	3	LSB
INLS	CC	T	Absolute Integral non-linearity-Standard channels	No overload			1.5	5	LSB
DNL	CC	T	Absolute Differential non-linearity	No overload			0.5	1	LSB
OFS	CC	T	Absolute Offset error	—			2		LSB
GNE	CC	T	Absolute Gain error	—			2		LSB
TUEP[9]	CC	P	Total Unadjusted Error for precise channels, input only pins	Without current injection		–6		6	LSB
		T		With current injection		–8		8	LSB
TUES[9]	CC	T	Total Unadjusted Error for standard channel	Without current injection		–10		10	LSB
		T		With current injection		–12		12	LSB

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS_HV} must be common (to be tied together externally).

3.18.2 MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency in 2:1 mode and two times the TX_CLK frequency in 1:1 mode.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

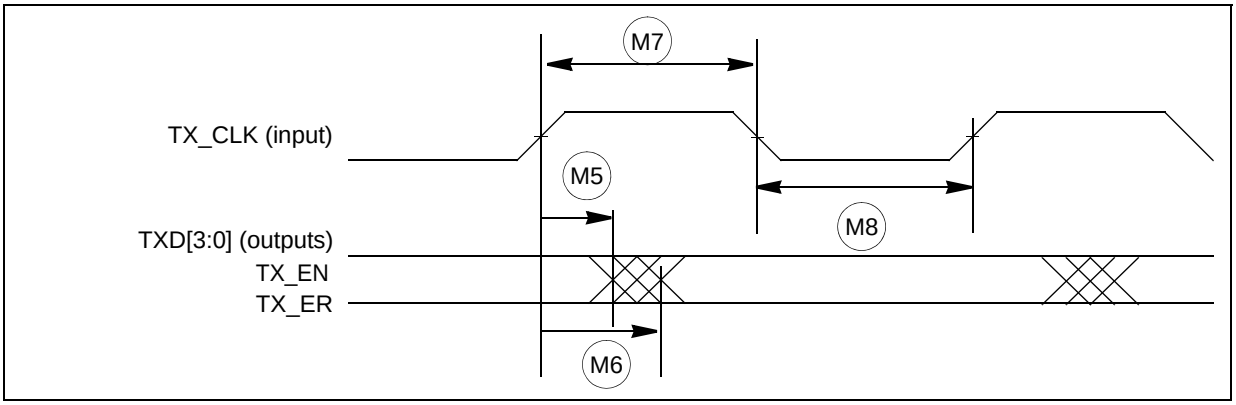
Refer to the Fast Ethernet Controller (FEC) chapter of the SPC564B74 and SPC56EC74 Reference Manual for details of this option and how to enable it.

Table 46. MII transmit signal timing(1)

Spec	Characteristic	Min	Max	Unit
M5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1. Output pads configured with SRE = 0b11.

Figure 22. MII transmit signal timing diagram



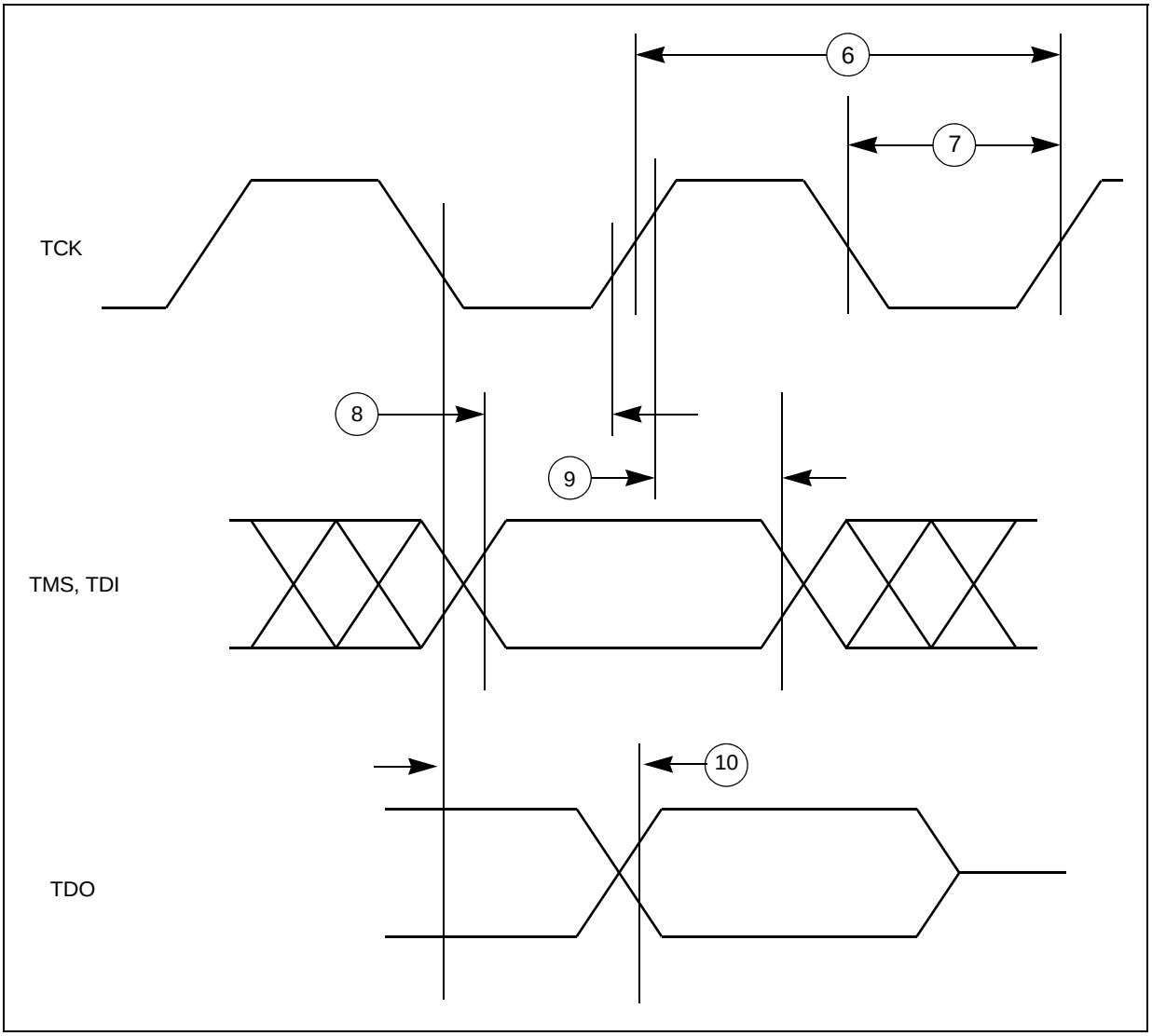
3.18.3 MII Async Inputs Signal Timing (CRS and COL)

Table 47. MII Async Inputs Signal Timing(1)

Spec	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

1. Output pads configured with SRE = 0b11.

Figure 35. Nexus TDI, TMS, TDO timing



3.19.4 JTAG characteristics

Table 52. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	10	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns
4	t_{TMSS}	CC	D	TMS setup time	10	—	—	ns
5	t_{TMSH}	CC	D	TMS hold time	5	—	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns

Table 54. LQFP208 mechanical data

Ref	mm			mm		
	Min	Typ	Max	Min	Typ	Max
A			1.6			1.6
A1	0.05		0.15	0.05	0.1	0.15
A2	1.3	1.35	1.45	1.3	1.35	1.45
B	0.17		0.27	0.17	0.22	0.27
c	0.09		0.2	0.11	0.15	0.19
D		30		29.8	30	30.2
D1		28		27.8	28	28.2
D3		25.5			25.5	
e		0.5			0.5	
E		30		29.8	30	30.2
E1		28		27.8	28	28.2
E3		25.5			25.5	
L	0.45	0.6	0.75	0.4	0.5	0.6
L1		1		1		
K	0 °	3.5 °	7.0 °	1 °	3 °	5 °

Table 57. Revision history (continued)

Date	Revision	Changes
01-Dec-2011	4	– Interchanged the denominator with numerator in Equation 11 of Input impedance and ADC accuracy section – Removed the note (All ADC conversion characteristics described in the table below are applicable only for the precision channels. The data for semi-precision and extended channels is awaited and same will be subsequently updated in later revs.) in the ADC electrical characteristics section. – *Table 49* (On-chip peripherals current consumption). Replaced IDD_HV_ADC with IDD_HV_ADC0 and IDD_HV_ADC1 values as per ADC specs – In *Table 43*, the minimum sample time of ADC0 changed to 500 at 32 MHz – In *Table 43*, removed the entry for sample time at 30 MHz – In *Table 44*, changed TUEX to TUES and INLX to INLS (Extended channels are not supported by the device. So, changed to standard channel.)
04-Mar-2013	5	– Updated the pins 23 and 24 of *Figure 2: 176-pin LQFP configuration*. – Updated unit of measure in *Table 44: Conversion characteristics (12-bit ADC_1)* – Modified the value to typical value in *Table 49: On-chip peripherals current consumption* – Added footnote to t_{ESRT} parameter in *Table 26: Code flash memory—Program and erase specifications* – Added footnote to t_{ESRT} parameter in *Table 27: Data flash memory—Program and erase specifications* – Updated *Table 29: Flash memory read access timing*. – Updated Notes 2 and Notes 3 of *Table 10: Recommended operating conditions (3.3 V)* and *Table 11: Recommended operating conditions (5.0 V)* respectively. – Updated the footnote1 of *Table 10: Recommended operating conditions (3.3 V)* and *Table 11: Recommended operating conditions (5.0 V)* – Updated $V_{DD\_HV\_A}$ to V_{DD_BV} for C_{DEC2} and $I_{DD\_HV\_A}$ in *Table 23: Voltage regulator electrical characteristics* and deleted footnote3 – Updated the dedicated number of channels for 12-bit ADC in family comparison tables – Updated the values of $f_{SIRC,}$ parameters and conditions of $\Delta_{SIRCVAR}$ in *Table 41: Slow internal RC oscillator (128 kHz) electrical characteristics* – Updated second footnote in *Table 11: Recommended operating conditions (5.0 V)*, – Updated the value of t_{ADC0_PU} in *Table 43: ADC conversion characteristics (10-bit ADC_0)* – Updated the IDD values in *Table 25: Low voltage power domain electrical characteristics* – Added footnote to *Table 25: Low voltage power domain electrical characteristics* related to current drawn from $V_{DD\_HV\_A}$ and $V_{DD\_HV\_B}$ – Updated entire *Section 3.17.1.1: Input impedance and ADC accuracy* – Updated the values of VLPREG in *Table 23: Voltage regulator electrical characteristics*. – Updated the values of V_{LPREG} in *Table 23: Voltage regulator electrical characteristics*. – Added T_A = 25 °C, min and max values of V_{MREG} in *Table 23: Voltage regulator electrical characteristics* – Added T_A = 25 °C, min and max values of V_{LPREG} in *Table 23: Voltage regulator electrical characteristics*

Table 57. Revision history (continued)

Date	Revision	Changes
28-Nov-2014	7 (cont.)	– Added Category column in *Table 44: Conversion characteristics (12-bit ADC_1)*. – Added the IDD_HV_ADC0 values in *Table 49: On-chip peripherals current consumption*.
16-Jun-2015	8	Updated *Figure 37: LQFP176 package mechanical drawing* and *Figure 40: Ordering information scheme*.
11-Mar-2016	9	– Added package silhouette on the cover page – Removed *Figure 4: LBGA208 configuration* – Removed LBGA208 column in *Table 4: System pin descriptions* and in *Table 5: Functional port pin descriptions* – *Table 12: LQFP thermal characteristics*: for "$R_{\theta JA}$" row, changed Max value relating to conditions "Single-layer board—1s" and "Four-layer board—2s2p" from "TBD" to "43" and "33.9", respectively – Removed *Table 13: LBGA208 thermal characteristics* – *Table 13: LBGA256 thermal characteristics*: for "$R_{\theta JA}$" row, changed Max value relating to conditions "Single-layer board—1s" and "Four-layer board—2s2p" from "TBD" to "44.3" and "31", respectively – Removed LBGA208 row in *Table 20: I/O supplies* – Removed *Section 4.2.3: LBGA208 package mechanical drawing* – In *Table 25: Low voltage power domain electrical characteristics*, updated notes "Only for the "P" classification: LPreg ON, HPVreg OFF, 96 KB RAM ON, device configured for...", "LPreg ON, HPVreg OFF, 64 KB RAM ON, device configured for...", and "LPreg ON, HPVreg OFF, 8 KB RAM ON, device configured for..." – In *Table 49: On-chip peripherals current consumption*, changed IDD_HV_ADC1 value from "300 × f_{periph}" to "300"

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