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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b70l7c9e0x

Table 1. Device summary

Package	Part number		
	1.5 MByte	2 MByte	3 MByte
LQFP176	SPC564B64L7 SPC56EC64L7	SPC564B70L7 SPC56EC70L7	SPC564B74L7 SPC56EC74L7
LQFP208	SPC564B64L8 SPC56EC64L8	SPC564B70L8 SPC56EC70L8	SPC564B74L8 SPC56EC74L8
LBGA256	SPC56EC64B3	SPC56EC70B3	SPC56EC74B3

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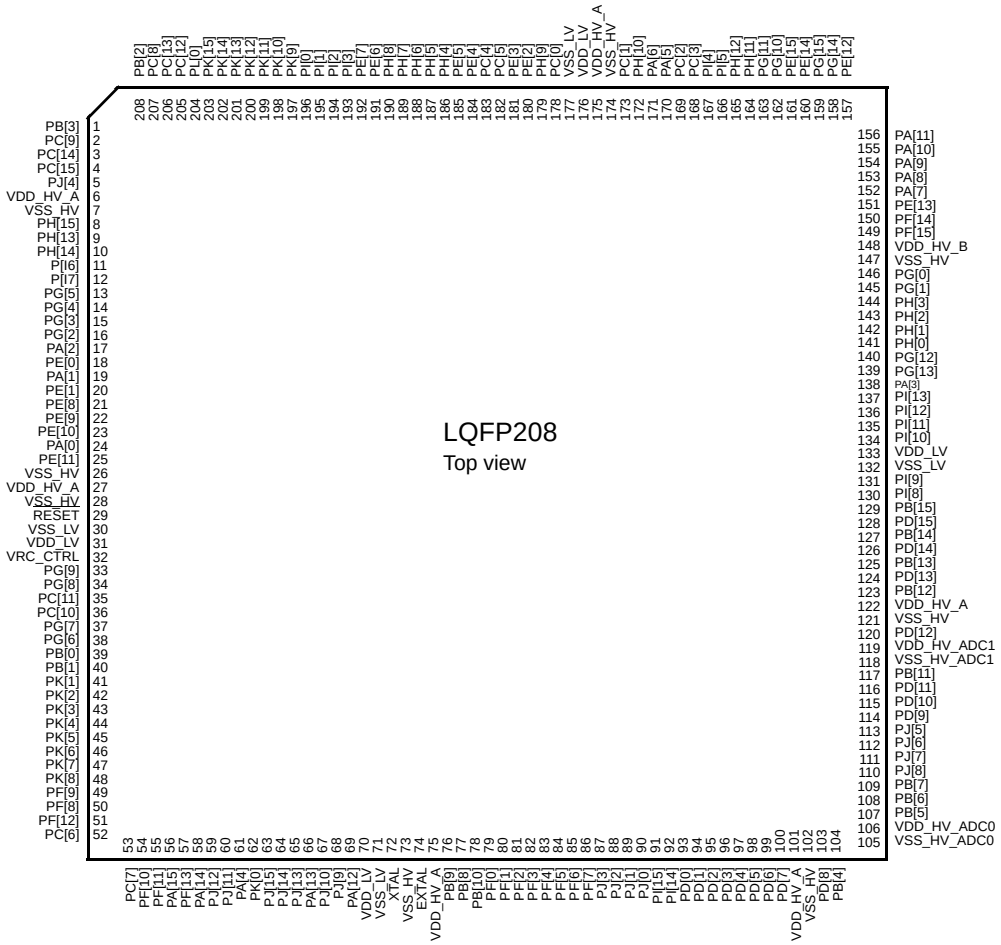
Figure 3. 208-pin LQFP configuration



NOTE
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], and PA[3].
2) Availability of port pin alternate functions depends on product selection.

2.1 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[a]

M = Medium[a],[b]

F = Fast[a],[b]

I = Input only with analog feature[a]

A = Analog

2.2 System pins

The system pins are listed in *Table 4*.

Table 4. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET config.	Pin number		
					LQFP 176	LQFP 208	LBGA 256
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	29	29	K1
EXTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	A[1]	—	58	74	T8
XTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	A[1]	—	56	72	T7

1. For analog pads, it is not recommended to enable IBE if APC is enabled to avoid extra current in middle range voltage.

a. See the I/O pad electrical characteristics in the device datasheet for details.

b. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium. For example, Fast/Medium pad will be Medium by default at reset. Similarly, Slow/Medium pad will be Slow by default. Only exception is PC[1] which is in medium configuration by default (refer to PCR.SRC in the reference manual, Pad Configuration Registers (PCR0—PCR198)).

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 — —	GPI[22] — — — ADC0_P[2] ADC1_P[2]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	92	108	N14
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 — —	GPI[23] — — — ADC0_P[3] ADC1_P[3]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	93	109	R16
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — — — —	GPI[24] — — — ADC0_S[0] ADC1_S[4] WKPU[25] OSC32k_XTAL[4]	SIUL — — — ADC_0 ADC_1 WKPU SXOSC	I — — — I I I I	I	—	61	77	T11
PB[9][5]	PCR[25]	AF0 AF1 AF2 AF3 — — — —	GPI[25] — — — ADC0_S[1] ADC1_S[5] WKPU[26] OSC32k_EXTAL[4]	SIUL — — — ADC_0 ADC_1 WKPU SXOSC	I — — — I I I I	I	—	60	76	T10
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — — —	GPIO[26] SOUT_1 CAN3TX — ADC0_S[2] ADC1_S[6] WKPU[8]	SIUL DSPI_1 FlexCAN_3 — ADC_0 ADC_1 WKPU	I/O O — — I I I	S	Tristate	62	78	N7

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlexD_2 eMIOS_0 —	I/O O I/O —	S	Tristate	175	207	B3
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13]	SIUL — eMIOS_0 — LINFlexD_2 WKPU	I/O — I/O — I I	S	Tristate	2	2	C3
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M/S	Tristate	36	36	L1
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] CAN1RX CAN4RX WKPU[5]	SIUL — — ADC_0 FlexCAN_1 FlexCAN_4 WKPU	I/O — — O I I I	S	Tristate	35	35	K4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[44] E0UC[12] — — FR_DBG[0] SIN_2 EIRQ[19]	SIUL eMIOS_0 — — Flexray DSPI_2 SIUL	I/O I/O — — O I I	M/S	Tristate	173	205	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3 ALT4	GPIO[45] E0UC[13] SOUT_2 — FR_DBG[1]	SIUL eMIOS_0 DSPI_2 — Flexray	I/O I/O O — O	M/S	Tristate	174	206	A3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PE[5]	PCR[69]	AF0 AF1 AF2 AF3 — —	GPIO[69] E0UC[21] CS0_1 MA[2] FR_B_RX WKPU[30]	SIUL eMIOS_0 DSPI_1 ADC_0 Flexray WKPU	I/O I/O I/O O I I	M/S	Tristate	161	185	B8
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	167	191	B6
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M/S	Tristate	168	192	A5
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M/S	Tristate	21	21	G1
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKPU[7] CAN2RX CAN3RX	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	22	22	H1
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 E1UC[30] EIRQ[10]	SIUL LINFlexD_3 DSPI_1 eMIOS_1 SIUL	I/O O O I/O I	S	Tristate	23	23	G3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ADC0_S[9]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	64	80	T6
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ADC0_S[10]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	65	81	R6
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	66	82	R7
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	67	83	R8
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	68	84	P8
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	69	85	N8
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	S	Tristate	70	86	P9

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PI[13]	PCR[141]	AF0 AF1 AF2 AF3 —	GPIO[141] CS1_3 CS1_2 — ADC0_S[21]	SIUL DSPI_3 DSPI_2 — ADC_0	I/O O O — I	S	Tristate	113	137	G14
PI[14]	PCR[142]	AF0 AF1 AF2 AF3 — —	GPIO[142] — — — ADC0_S[22] SIN_4	SIUL — — — ADC_0 DSPI_4	I/O — — — I I	S	Tristate	76	92	T12
PI[15]	PCR[143]	AF0 AF1 AF2 AF3 —	GPIO[143] CS0_4 CS2_2 — ADC0_S[23]	SIUL DSPI_4 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	75	91	P11
PJ[0]	PCR[144]	AF0 AF1 AF2 AF3 —	GPIO[144] CS1_4 CS3_2 — ADC0_S[24]	SIUL DSPI_4 DSPI_2 — ADC_0	I/O O O — I	S	Tristate	74	90	R11
PJ[1]	PCR[145]	AF0 AF1 AF2 AF3 — —	GPIO[145] — — — ADC0_S[25] SIN_5	SIUL — — —— ADC_0 DSPI_5	I/O — — — I I	S	Tristate	73	89	N10
PJ[2]	PCR[146]	AF0 AF1 AF2 AF3 —	GPIO[146] CS0_5 CS0_6 CS0_7 ADC0_S[26]	SIUL DSPI_5 DSPI_6 DSPI_7 ADC_0	I/O I/O I/O I/O I	S	Tristate	72	88	R10

3 Electrical Characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS_HV}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 6* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 NVUSRO register

Portions of the device configuration, such as high voltage supply is controlled via bit values in the Non-Volatile User Options Register (NVUSRO). For a detailed description of the NVUSRO register, see SPC564Bxx and SPC56ECxx Reference Manual.

3.4 Recommended operating conditions

Table 10. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$(1)	SR	Voltage on $V_{DD\_HV\_A}$ pins with respect to ground (V_{SS_HV})	—	3.0	3.6	V
$V_{DD\_HV\_B}$(1)	SR	Voltage on $V_{DD\_HV\_B}$ pins with respect to ground (V_{SS_HV})	—	3.0	3.6	V
V_{SS_LV}(2)	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
V_{RC_CTRL}(3)		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
$V_{DD\_HV\_ADC0}$(4)	SR	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	3.0(5)	3.6	V
			Relative to $V_{DD\_HV\_A}$(6)	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
$V_{DD\_HV\_ADC1}$(7)	SR	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_A}$(6)	$V_{DD\_HV\_A}$ – 0.1	$V_{DD\_HV\_A}$ + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	—	V
			Relative to $V_{DD\_HV\_A/HV\_B}$	—	$V_{DD\_HV\_A/HV\_B}$ + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	$V_{DD\_HV\_A}$ slope to ensure correct power up(8)	—	—	0.5	V/µs
			—	0.5	—	V/min

Table 10. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
T_A	SR	Ambient temperature under bias	f_{CPU} up to 120 MHz + 2%	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	

1. 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
2. 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 µF bulk capacitance needs to be provided as CREG on each VDD_LV pin. For details refer to the Power Management chapter of the MPC5646C Reference Manual.
3. This voltage is internally generated by the device and no external voltage should be supplied.
4. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
6. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.
7. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.
8. Guaranteed by the device validation.

Table 11. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$(1)	SR	Voltage on VDD_HV_A pins with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
$V_{DD\_HV\_B}$	SR	Generic GPIO functionality	—	3.0	5.5	V
		Ethernet/3.3 V functionality (See the notes in all figures in *Section 2: Package pinouts and signal descriptions* for the list of channels operating in $V_{DD\_HV\_B}$ domain)	—	3.0	3.6	V
V_{SS_LV}(3)	SR	Voltage on VSS_LV (Low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
V_{RC_CTRL}(4)		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V

Table 16. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		P			I_{OL} = 1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 17. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		C			I_{OL} = 1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

The internal voltage regulator requires external bulk capacitance (C_{REGn}) to be connected to the device to provide a stable low voltage digital supply to the device. Also required for stability is the C_{DEC2} capacitor at ballast collector. This is needed to minimize sharp injection current when ballast is turning ON. Apart from the bulk capacitance, user should connect EMI/decoupling cap (C_{REGP}) at each V_{DD_LV}/V_{SS_LV} pin pair.

3.8.1.1 Recommendations

- The external NPN driver must be BCP68 type.
- V_{DD_LV} should be implemented as a power plane from the emitter of the ballast transistor.
- 10 µF capacitors should be connected to the 4 pins closest to the outside of the package and should be evenly distributed around the package. For BGA packages, the balls should be used are D8, H14, R9, J3–one cap on each side of package.
  - There should be a track direct from the capacitor to this pin (pin also connects to V_{DD_LV} plane). The tracks ESR should be less than 100 mΩ.
  - The remaining V_{DD_LV} pins (exact number will vary with package) should be decoupled with 0.1 µF caps, connected to the pin as per 10 µF.

(see *Section 3.4: Recommended operating conditions*).

3.8.2 V_{DD_BV} options

- Option 1: V_{DD_BV} shared with $V_{DD\_HV\_A}$

  V_{DD_BV} must be star routed from $V_{DD\_HV\_A}$ from the common source. This is to eliminate ballast noise injection on the MCU.
- Option 2: V_{DD_BV} independent of the MCU supply

  V_{DD_BV} > 2.6 V for correct functionality. The device is not monitoring this supply hence the external component must meet the 2.6 V criteria through external monitoring if required.

Table 23. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	External ballast stability capacitance	—	40	—	60	µF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	—	—	—	0.2	W
C_{REGP}	SR	—	Decoupling capacitance (Close to the pin)	$V_{DD\_HV\_A/HV\_B}/V_{SS\_HV}$ pair		100	—	nF
				V_{DD_LV}/V_{SS_LV} pair		100	—	nF
C_{DEC2}	SR	—	Stability capacitance regulator supply (Close to the ballast collector)	V_{DD_BV}/V_{SS_HV}	10	—	40	µF
V_{MREG}	CC	P	Main regulator output voltage	After trimming T_A = 25 °C	1.20	1.28	1.32	V

Table 25. Low voltage power domain electrical characteristics(1)

Symbol		C	Parameter	Conditions(2)		Value			Unit
						Min	Typ(3)	Max(4)	
I_{DDMAX}(5)	CC	D	RUN mode maximum average current	—		—	210	300(6), (7)	mA
I_{DDRUN}	CC	P	RUN mode typical average current(8)	at 120 MHz	T_A = 25 °C	—	150	208(9)	mA
		D		at 80 MHz	T_A = 25 °C	—	110(8)	150(10)	mA
		C		at 120 MHz	T_A = 125 °C	—	180	280	mA
I_{DDHALT}	CC	P	HALT mode current(11)	at 120 MHz	T_A = 25 °C	—	20	27	mA
		C		at 120 MHz	T_A = 125 °C	—	35	100	mA
I_{DDSTOP}	CC	P	STOP mode current(12)	No clocks active	T_A = 25 °C	—	0.4	5	mA
		C			T_A = 125 °C	—	16	72	mA
$I_{DDSTDBY3}$ (96 KB RAM retained)	CC	P	STANDBY3 mode current(13)	No clocks active	T_A = 25 °C	—	50	96	µA
		C			T_A = 125 °C	—	630	2400	µA
$I_{DDSTDBY2}$ (64 KB RAM retained)	CC	C	STANDBY2 mode current(14)	No clocks active	T_A = 25 °C	—	40	92	µA
		C			T_A = 125 °C	—	500	2000	µA
$I_{DDSTDBY1}$ (8 KB RAM retained)	CC	C	STANDBY1 mode current(15)	No clocks active	T_A = 25 °C	—	25	85	µA
		C			T_A = 125 °C	—	230	1100	µA
Adders in LP mode	CC	T	32 KHz OSC	—	T_A = 25 °C	—	—	5	µA
			4–40 MHz OSC	—	T_A = 25 °C	—	—	3	mA
			16 MHz IRC	—	T_A = 25 °C	—	—	500	µA
			128 KHz IRC	—	T_A = 25 °C	—	—	5	µA

1. Except for I_{DDMAX}, all the current values are total current drawn from $V_{DD\_HV\_A}$.
2. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified All temperatures are based on an ambient temperature.
3. Target typical current consumption for the following typical operating conditions and configuration. Process = typical, Voltage = 1.2 V.
4. Target maximum current consumption for mode observed under typical operating conditions. Process = Fast, Voltage = 1.32 V.
5. Running consumption is given on voltage regulator supply (V_{DDREG}). It does not include consumption linked to I/Os toggling. This value is highly dependent on the application. The given value is thought to be a worst case value with all cores and peripherals running, and code fetched from code flash while modify operation on-going on data flash. It is to be noticed that this value can be significantly reduced by application: switch-off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.
6. Higher current may sunk by device during power-up and standby exit. Please refer to in rush current in *Table 23*.
7. Maximum “allowed” current is package dependent.
8. Only for the “P” classification: Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled. RUN current measured with typical application with accesses on both code flash and RAM.

Table 27. Data flash memory—Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ(1)	Initial max(2)	Max(3)	
$T_{wprogram}$	CC	C	Word (32 bits) program time(4)	—	30	70	500	µs
$T_{16Kpperase}$			16 KB block pre-program and erase time	—	700	800	5000	ms
T_{eslat}		D	Erase Suspend Latency	—	—	30	30	µs
t_{ESRT}(5)		C	Erase Suspend Request Rate	10	—	—	—	ms
t_{PABT}		D	Program Abort Latency	—	—	12	12	µs
t_{EAPT}		D	Erase Abort Latency	—	—	30	30	µs

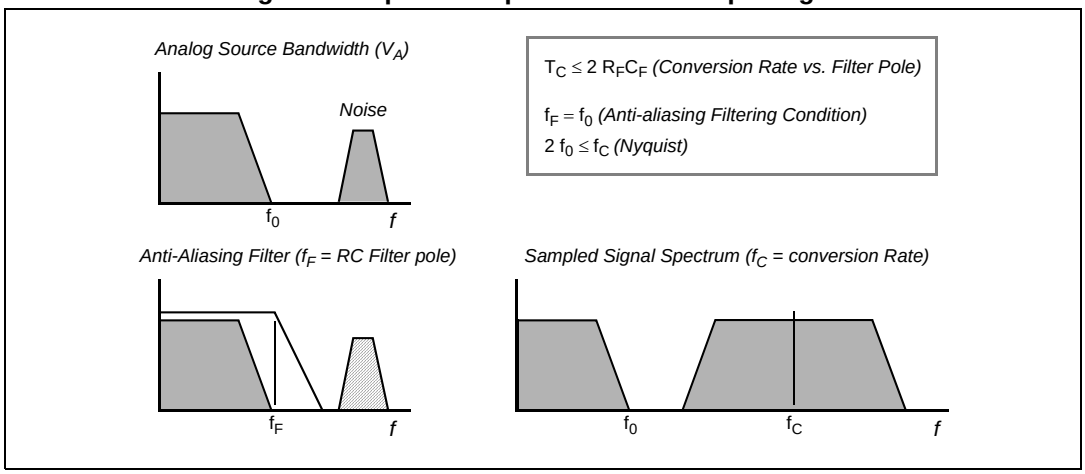
1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. It is time between erase suspend resume and next erase suspend.

Table 28. Flash memory module life

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Typ	
P/E	CC	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100000	100000	cycles
			Number of program/erase cycles per block for 32 Kbyte blocks over the operating temperature range (T_J)	—	10000	100000	cycles
			Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0–1000 P/E cycles	20	—	years
				Blocks with 10000 P/E cycles	10	—	years
				Blocks with 100000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Figure 19. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S:

Equation 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

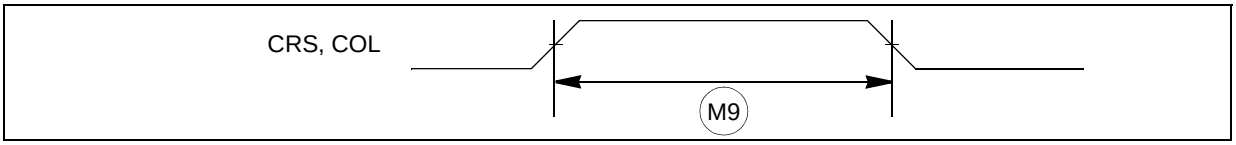
Equation 12 ADC_0 (10-bit)

$$C_F > 2048 \bullet C_S$$

Equation 13 ADC_1 (12-bit)

$$C_F > 8192 \bullet C_S$$

Figure 23. MII async inputs timing diagram



3.18.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 48. MII serial management channel timing(1)

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	28	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1. Output pads configured with SRE = 0b11.

Figure 24. MII serial management channel timing diagram

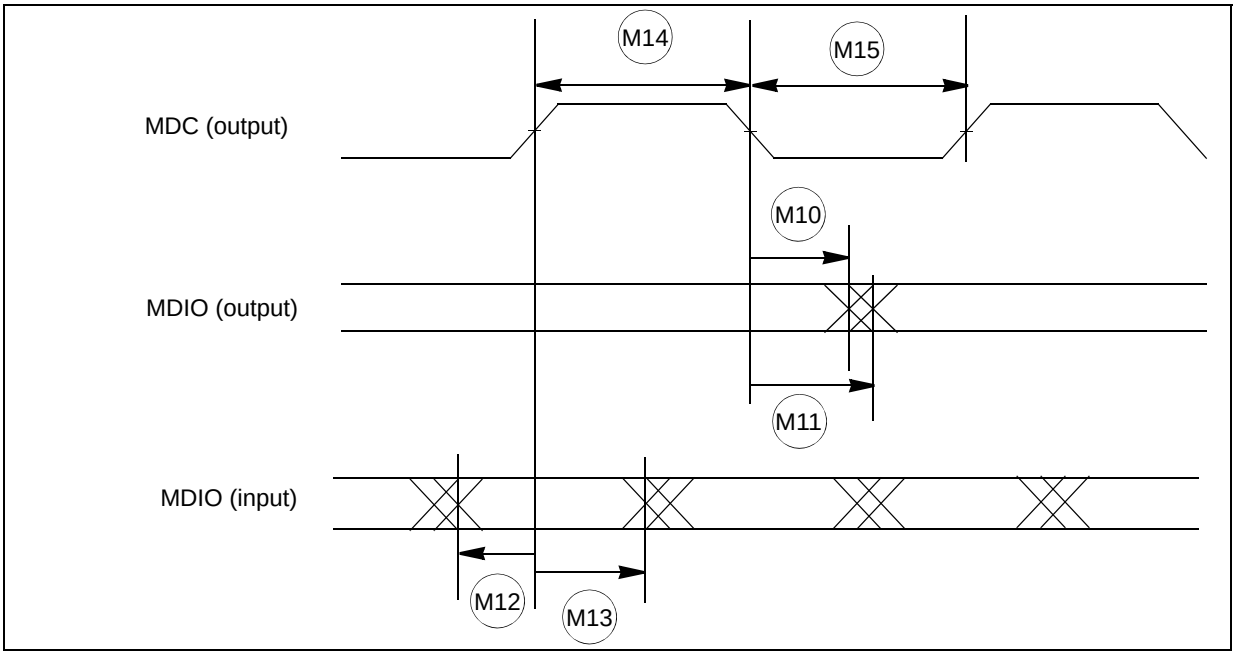
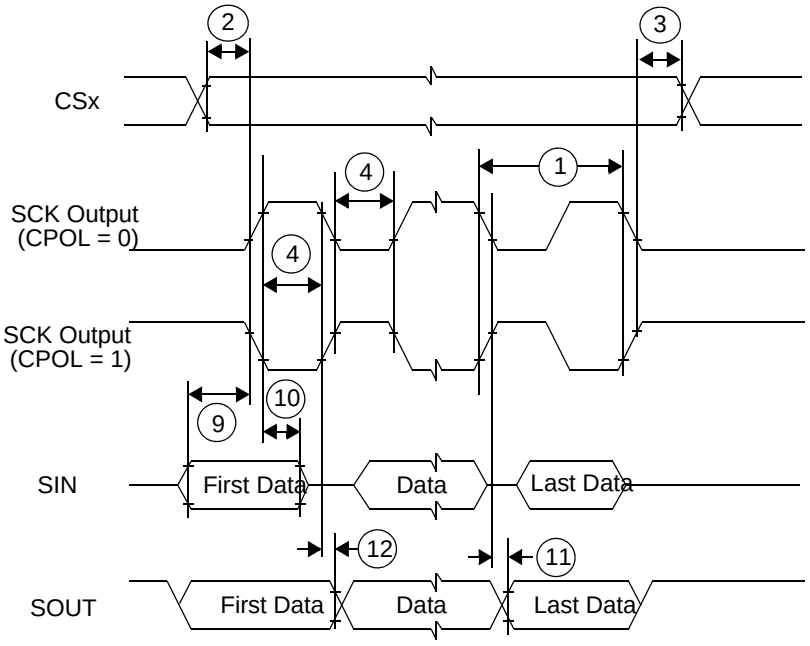
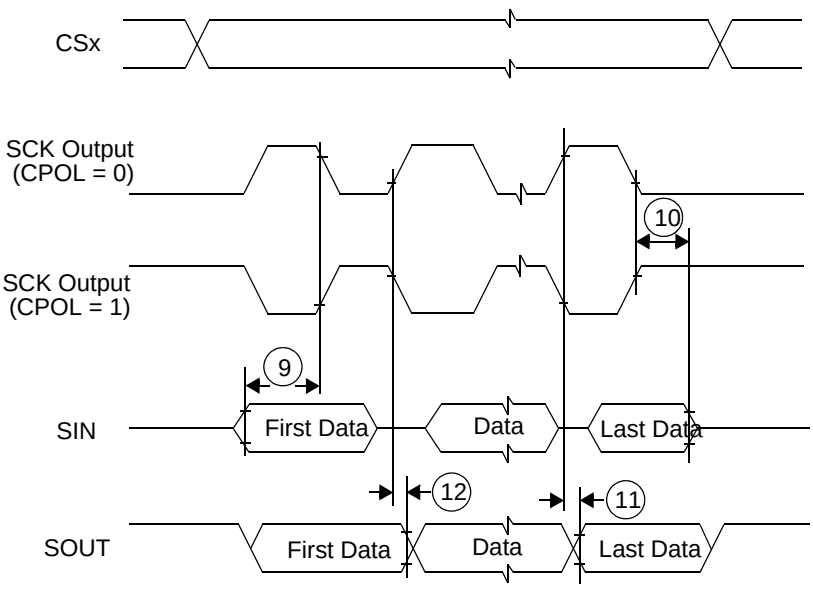


Figure 25. DSPI classic SPI timing–master, CPHA = 0



Note: Numbers shown reference *Table 50*.

Figure 26. DSPI classic SPI timing–master, CPHA = 1



Note: Numbers shown reference *Table 50*.

Appendix A Abbreviations

Table 56 lists abbreviations used but not defined elsewhere in this document.

Table 56. Abbreviations

Abbreviation	Meaning
CS	Chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select