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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	199
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x10b, 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-LBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b74b3b9e0y

List of figures

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[15]	PB[2]	PC[13]	PI[1]	PE[7]	PH[8]	PE[2]	PE[4]	PC[4]	PE[3]	PH[9]	PI[4]	PH[11]	PE[14]	PA[10]	PG[11]	A
B	PH[13]	PC[14]	PC[8]	PC[12]	PI[3]	PE[6]	PH[5]	PE[5]	PC[5]	PC[0]	PC[2]	PH[12]	PG[10]	PA[11]	PA[9]	PA[8]	B
C	PH[14]	VDD_HV_A	PC[9]	PL[0]	PI[0]	PH[7]	PH[6]	VSS_LV	VDD_HV_A	PA[5]	PC[3]	PE[15]	PG[14]	PE[12]	PA[7]	PE[13]	C
D	PG[5]	PI[6]	PJ[4]	PB[3]	PK[15]	PI[2]	PH[4]	VDD_LV	PC[1]	PH[10]	PA[6]	PI[5]	PG[15]	PF[14]	PF[15]	PH[2]	D
E	PG[3]	PI[7]	PH[15]	PG[2]	VDD_LV	VSS_LV	PK[10]	PK[9]	PM[1]	PM[0]	PL[15]	PL[14]	PG[0]	PG[1]	PH[0]	VDD_HV_A	E
F	PA[2]	PG[4]	PA[1]	PE[1]	PL[2]	PM[6]	PL[1]	PK[11]	PM[5]	PL[13]	PL[12]	PM[2]	PH[1]	PH[3]	PG[12]	PG[13]	F
G	PE[8]	PE[0]	PE[10]	PA[0]	PL[3]	VSS_HV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	PK[12]	VDD_HV_B	PI[13]	PI[12]	PA[3]	G
H	PE[9]	VDD_HV_A	PE[11]	PK[1]	PL[4]	VSS_LV	VSS_LV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	PK[13]	VDD_HV_A	VDD_LV	VSS_LV	PI[11]	H
J	VSS_HV	VRC_CTRL	VDD_LV	PG[9]	PL[5]	VSS_LV	VSS_LV	VSS_LV	VSS_HV	VSS_HV	VSS_HV	PK[14]	PD[15]	PI[8]	PI[9]	PI[10]	J
K	RESET	VSS_LV	PG[8]	PC[11]	PL[6]	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_LV	VDD_LV	PM[3]	PD[14]	PD[13]	PB[14]	PB[15]	K
L	PC[10]	PG[7]	PB[0]	PK[2]	PL[7]	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_LV	VDD_LV	PM[4]	PD[12]	PB[12]	PB[13]	VDD_HV_ADC1	L
M	PG[6]	PB[1]	PK[4]	PF[9]	PK[5]	PK[6]	PK[7]	PK[8]	PL[8]	PL[9]	PL[10]	PL[11]	PB[11]	PD[10]	PD[11]	VSS_HV_ADC1	M
N	PK[3]	PF[8]	PC[6]	PC[7]	PJ[13]	VDD_HV_A	PB[10]	PF[6]	VDD_HV_A	PJ[1]	PD[2]	PJ[5]	PB[5]	PB[6]	PJ[6]	PD[9]	N
P	PF[12]	PF[10]	PF[13]	PA[14]	PJ[9]	PA[12]	PF[0]	PF[5]	PF[7]	PJ[3]	PI[15]	PD[4]	PD[7]	PD[8]	PJ[8]	PJ[7]	P
R	PF[11]	PA[15]	PJ[11]	PJ[15]	PA[13]	PF[2]	PF[3]	PF[4]	VDD_LV	PJ[2]	PJ[0]	PD[0]	PD[3]	PD[6]	VDD_HV_ADC0	PB[7]	R
T	PJ[12]	PA[4]	PK[0]	PJ[14]	PJ[10]	PF[1]	XTAL	EXTAL	VSS_LV	PB[9]	PB[8]	PI[14]	PD[1]	PD[5]	VSS_HV_ADC0	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Notes:
1) VDD_HV_B supplies the IO voltage domain for the pins PE[12], PA[11], PA[10], PA[9], PA[8], PA[7], PE[13], PF[14], PF[15], PG[0], PG[1], PH[3], PH[2], PH[1], PH[0], PG[12], PG[13], PA[3], PM[3], and PM[4].
2)Availability of port pin alternate functions depends on product selection.

Figure 4. 256-pin BGA configuration

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC0_S[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — I/O I	S	Tristate	97	117	M13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC0_X[0]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	101	123	L14
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC0_X[1]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	103	125	L15
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC0_X[2]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	105	127	K15
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC0_X[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	S	Tristate	107	129	K16
PC[0][6]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M/S	Input, weak pull-up	154	178	B10
PC[1][6]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F/M	Tristate	149	173	D9

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlexD_2 eMIOS_0 —	I/O O I/O —	S	Tristate	175	207	B3
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13]	SIUL — eMIOS_0 — LINFlexD_2 WKPU	I/O — I/O — I I	S	Tristate	2	2	C3
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M/S	Tristate	36	36	L1
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] CAN1RX CAN4RX WKPU[5]	SIUL — — ADC_0 FlexCAN_1 FlexCAN_4 WKPU	I/O — — O I I I	S	Tristate	35	35	K4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[44] E0UC[12] — — FR_DBG[0] SIN_2 EIRQ[19]	SIUL eMIOS_0 — — Flexray DSPI_2 SIUL	I/O I/O — — O I I	M/S	Tristate	173	205	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3 ALT4	GPIO[45] E0UC[13] SOUT_2 — FR_DBG[1]	SIUL eMIOS_0 DSPI_2 — Flexray	I/O I/O O — O	M/S	Tristate	174	206	A3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 — —	GPI[51] — — — ADC0_P[7] ADC1_P[7]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	80	96	R13
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 — —	GPI[52] — — — ADC0_P[8] ADC1_P[8]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	81	97	P12
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 — —	GPI[53] — — — ADC0_P[9] ADC1_P[9]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	82	98	T14
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 — —	GPI[54] — — — ADC0_P[10] ADC1_P[10]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	83	99	R14
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 — —	GPI[55] — — — ADC0_P[11] ADC1_P[11]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	84	100	P13
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 — —	GPI[56] — — — ADC0_P[12] ADC1_P[12]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	87	103	P14

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX CS4_0 CAN2TX	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M/S	Tristate	42	50	N2
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — — —	GPIO[89] E1UC[1] CS5_0 — CAN2RX CAN3RX WKPU[22]	SIUL eMIOS_1 DSPI_0 — FlexCAN_2 FlexCAN_3 WKPU	I/O I/O O — I I I	S	Tristate	41	49	M4
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] CS1_0 LIN4TX E1UC[2]	SIUL DSPI_0 LINFlexD_4 eMIOS_1	I/O O O I/O	M/S	Tristate	46	54	P2
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 — —	GPIO[91] CS2_0 E1UC[3] — LIN4RX WKPU[15]	SIUL DSPI_0 eMIOS_1 — LINFlexD_4 WKPU	I/O O I/O — I I	S	Tristate	47	55	R1
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] LIN5TX —	SIUL eMIOS_1 LINFlexD_5 —	I/O I/O O —	M/S	Tristate	43	51	P1
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] — — LIN5RX WKPU[16]	SIUL eMIOS_1 — — LINFlexD_5 WKPU	I/O I/O — — I I	S	Tristate	49	57	P3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PJ[3]	PCR[147]	AF0 AF1 AF2 AF3 —	GPIO[147] CS1_5 CS1_6 CS1_7 ADC0_S[27]	SIUL DSPI_5 DSPI_6 DSPI_7 ADC_0	I/O O O O I	S	Tristate	71	87	P10
PJ[4]	PCR[148]	AF0 AF1 AF2 AF3	GPIO[148] SCK_5 E1UC[18] —	SIUL DSPI_5 eMIOS_1 —	I/O I/O I/O —	M/S	Tristate	5	5	D3
PJ[5]	PCR[149]	AF0 AF1 AF2 AF3 —	GPIO[149] — — — ADC0_S[28]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	113	N12
PJ[6]	PCR[150]	AF0 AF1 AF2 AF3 —	GPIO[150] — — — ADC0_S[29]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	112	N15
PJ[7]	PCR[151]	AF0 AF1 AF2 AF3 —	GPIO[151] — — — ADC0_S[30]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	111	P16
PJ[8]	PCR[152]	AF0 AF1 AF2 AF3 —	GPIO[152] — — — ADC0_S[31]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	110	P15
PJ[9]	PCR[153]	AF0 AF1 AF2 AF3 —	GPIO[153] — — — ADC1_S[8]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	68	P5

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PL[6]	PCR[182]	AF0 AF1 AF2 AF3	GPIO[182] — MDO4 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	K5
PL[7]	PCR[183]	AF0 AF1 AF2 AF3	GPIO[183] — MDO5 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	L5
PL[8]	PCR[184]	AF0 AF1 AF2 AF3 —	GPIO[184] — — — EVTI	SIUL — — — Nexus	I/O — — — I	S	Pull-up	—	—	M9
PL[9]	PCR[185]	AF0 AF1 AF2 AF3	GPIO[185] — MSEO —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	M10
PL[10]	PCR[186]	AF0 AF1 AF2 AF3	GPIO[186] — MCKO —	SIUL — Nexus —	I/O — O —	F/S	Tristate	—	—	M11
PL[11]	PCR[187]	AF0 AF1 AF2 AF3	GPIO[187] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	M12
PL[12]	PCR[188]	AF0 AF1 AF2 AF3	GPIO[188] — EVTO —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F11
PL[13]	PCR[189]	AF0 AF1 AF2 AF3	GPIO[189] — MDO6 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F10

3.2.1 NVUSRO [PAD3V5V(0)] field description

Table 7 shows how NVUSRO [PAD3V5V(0)] controls the device configuration for $V_{DD\_HV\_A}$ domain.

Table 7. PAD3V5V(0) field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

3.2.2 NVUSRO [PAD3V5V(1)] field description

Table 8 shows how NVUSRO [PAD3V5V(1)] controls the device configuration the device configuration for $V_{DD\_HV\_B}$ domain.

Table 8. PAD3V5V(1) field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$	SR	Voltage on VDD_HV_A pins with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
$V_{DD\_HV\_B}$[1]	SR	Voltage on VDD_HV_B pins with respect to common ground (V_{SS_HV})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	$V_{SS\_HV} - 0.1$	$V_{SS\_HV} + 0.1$	V

Table 16. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		P			I_{OL} = 1.5 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 17. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		C			I_{OL} = 1.5 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 2 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.7 RESET electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 6. Start-up reset requirements

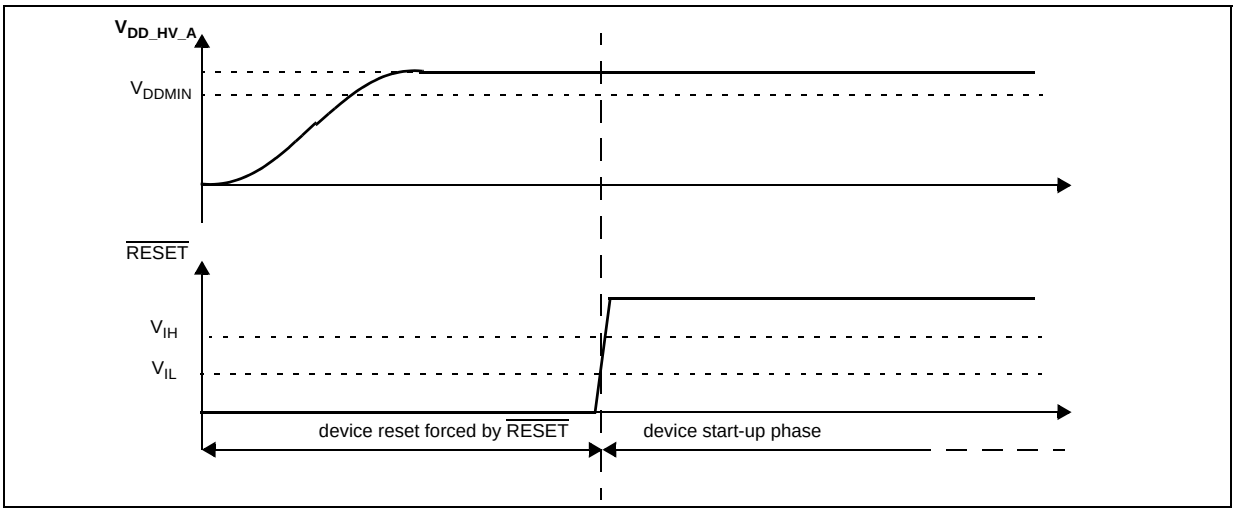
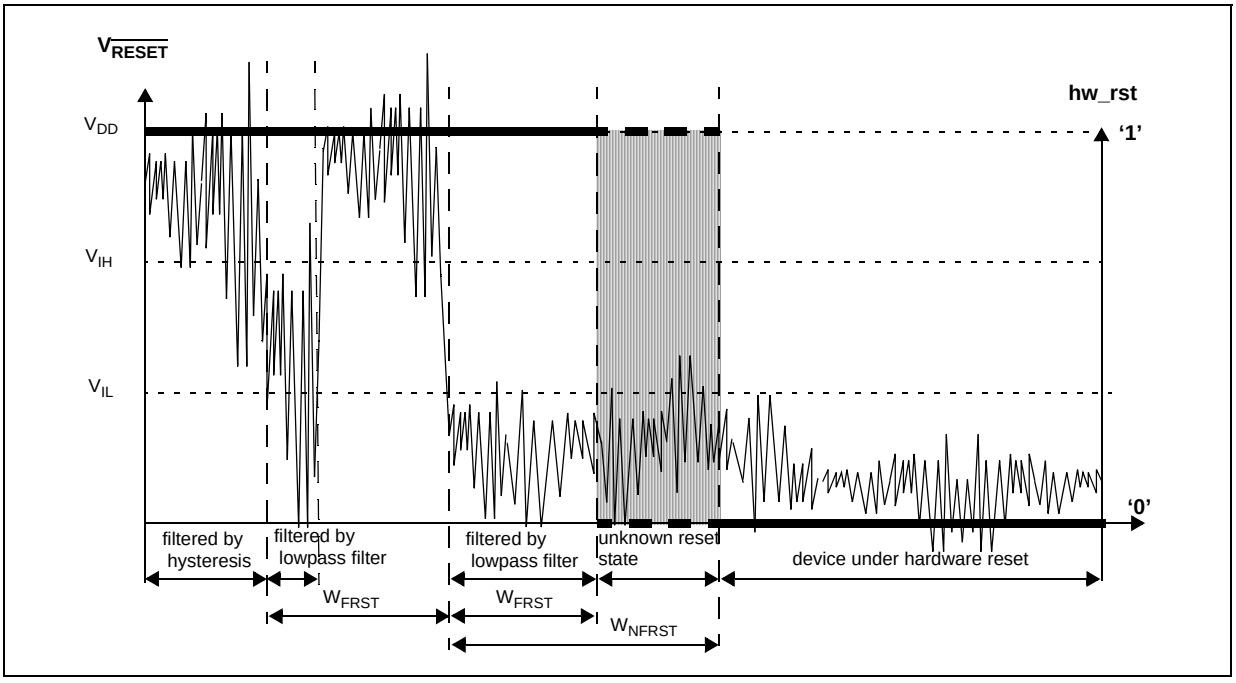


Figure 7. Noise filtering on reset signal



9. Subject to change, Configuration: 1 × e200z4d + 4 kbit/s Cache, 1 × e200z0h (1/2 system frequency), CSE, 1 × eDMA (10 ch.), 6 × FlexCAN (4 × 500 kbit/s, 2 × 125 kbit/s), 4 × LINFlexD (20 kbit/s), 6 × DSPI (2 × 2 Mbit/s, 3 × 4 Mbit/s, 1 × 10 Mbit/s), 16 × Timed I/O, 16 × ADC Input, 1 × FlexRay (2 ch., 10 Mbit/s), 1 × FEC (100 Mbit/s), 1 × RTC, 4 PIT channels, 1 × SWT, 1 × STM. For lower pin count packages reduce the amount of timed I/O's and ADC channels. RUN current measured with typical application with accesses on both code flash and RAM.
10. This value is obtained from limited sample set.
11. Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz ON. 16 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but no reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3-9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]-PA[11] and PC[12]-PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication, instance: 1-7 clocks gated). RTC/API ON. PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.
12. Only for the "P" classification: No clock, FIRC 16 MHz OFF, SIRC128 kHz ON, PLL OFF, HPvreg OFF, LPVreg ON. All possible peripherals off and clock gated. Flash in power down mode.
13. Only for the "P" classification: LPreg ON, HPVreg OFF, 96 KB RAM ON, device configured for minimum consumption, all possible modules switched-off. Measurement condition assumes T_j = Ta.
14. LPreg ON, HPVreg OFF, 64 KB RAM ON, device configured for minimum consumption, all possible modules switched-off. Measurement condition assumes T_j = Ta.
15. LPreg ON, HPVreg OFF, 8 KB RAM ON, device configured for minimum consumption, all possible modules switched OFF. Measurement condition assumes T_j = Ta.

3.10 Flash memory electrical characteristics

3.10.1 Program/Erase characteristics

Table 26 shows the code flash memory program and erase characteristics.

Table 26. Code flash memory—Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ(1)	Initial max(2)	Max(3)	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time(4)	—	18	50	500	µs
$T_{16Kpperase}$			16 KB block pre-program and erase time	—	200	500	5000	ms
$T_{32Kpperase}$			32 KB block pre-program and erase time	—	300	600	5000	ms
$T_{128Kpperase}$			128 KB block pre-program and erase time	—	600	1300	5000	ms
T_{eslat}		D	Erase Suspend Latency	—	—	30	30	µs
t_{ESRT}(5)		C	Erase Suspend Request Rate	20	—	—	—	ms
t_{PABT}		D	Program Abort Latency	—	—	10	10	µs
t_{EAPT}		D	Erase Abort Latency	—	—	30	30	µs

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. It is Time between erase suspend resume and the next erase suspend request.

Table 27 shows the data flash memory program and erase characteristics.

Table 27. Data flash memory—Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ(1)	Initial max(2)	Max(3)	
$T_{wprogram}$	CC	C	Word (32 bits) program time(4)	—	30	70	500	µs
$T_{16Kpperase}$			16 KB block pre-program and erase time	—	700	800	5000	ms
T_{eslat}		D	Erase Suspend Latency	—	—	30	30	µs
t_{ESRT}(5)		C	Erase Suspend Request Rate	10	—	—	—	ms
t_{PABT}		D	Program Abort Latency	—	—	12	12	µs
t_{EAPT}		D	Erase Abort Latency	—	—	30	30	µs

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. It is time between erase suspend resume and next erase suspend.

Table 28. Flash memory module life

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Typ	
P/E	CC	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100000	100000	cycles
			Number of program/erase cycles per block for 32 Kbyte blocks over the operating temperature range (T_J)	—	10000	100000	cycles
			Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0–1000 P/E cycles	20	—	years
				Blocks with 10000 P/E cycles	10	—	years
				Blocks with 100000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

3.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 32. EMI radiated emission measurement(1)(2)

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150		1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	120	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP176 package Test conforming to IEC 61967-2, f_{OSC} = 40 MHz/f_{CPU} = 120 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14(3)	dBµV

1. EMI testing and I/O port waveforms per IEC 61967-1, -2, -4.
2. For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.
3. All values need to be confirmed during device validation.

3.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

3.11.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard. For more details, refer to the application note *Electrostatic Discharge Sensitivity Measurement* (AN1181).

Table 33. ESD absolute maximum ratings(1)(2)

Symbol	Ratings	Conditions	Class	Max value(3)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
				750 (corners)	

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production.

3.11.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over-voltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 34. Latch-up results

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.12 Fast external crystal oscillator (4–40 MHz) electrical characteristics

The device provides an oscillator/resonator driver. *Figure 10* describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 35 provides the parameter description of 4 MHz to 40 MHz crystals used for the design simulations.

Figure 14. Slow external crystal oscillator (32 kHz) electrical characteristics

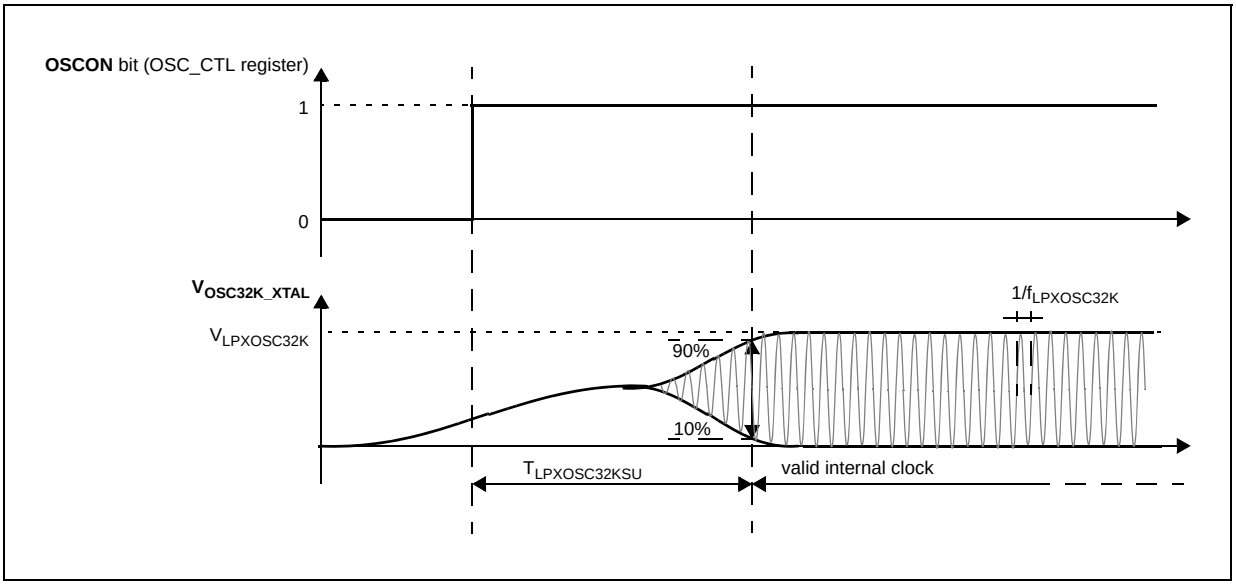


Table 38. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
g_{mSXOSC}	CC	—	Slow external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%,	13[3]	—	33[3]	µA/V
				V_{DD} = 5.0 V ± 10%	15[3]	—	35[3]	
V_{SXOSC}	CC	T	Oscillation amplitude	—	1.2	1.4	1.7	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—	1.2	—	4.4	µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	7	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[4]	s

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Based on ATE CZ
4. Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

3.17.1.2 ADC electrical characteristics

Table 42. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 43. ADC conversion characteristics (10-bit ADC_0)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC0}	SR	—	Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V_{SS_HV})[2]	—	–0.1	—	0.1	V
V_{DD_ADC0}	SR	—	Voltage on VDD_HV_ADC0 pin (ADC_0 reference) with respect to ground (V_{SS_HV})	—	$V_{DD\_HV\_A}$ – 0.1	—	$V_{DD\_HV\_A}$ + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC0} – 0.1	—	V_{DD_ADC0} + 0.1	V
f_{ADC0}	SR	—	ADC_0 analog frequency	—	6	—	32 + 2%	MHz
t_{ADC0_PU}	SR	—	ADC_0 power up delay	—	—	—	1.5	µs
t_{ADC0_S}	CC	T	Sample time[4]	f_{ADC} = 32 MHz	500	—		ns
t_{ADC0_C}	CC	P	Conversion time[5],[6]	f_{ADC} = 32 MHz	0.625	—		µs
				f_{ADC} = 30 MHz	0.700	—		
C_S	CC	D	ADC_0 input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC_0 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_0 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_0 input pin capacitance 3	—	—	—	1	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	3	kΩ

3. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence VDD_HV_ADC1 should be within ±100 mV of VDD_HV_B when these channels are used for ADC_1.
4. VDD_HV_ADC1 can operate at 5V condition while $V_{DD\_HV\_B}$ can operate at 3.3V provided that ADC_1 channels coming from $V_{DD\_HV\_B}$ domain are limited in max swing as $V_{DD\_HV\_B}$.
5. V_{AINx} may exceed V_{SS_ADC1} and V_{DD_ADC1} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.
6. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC1_S}. After the end of the sample time t_{ADC1_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC1_S} depend on programming.
7. Conversion time = Bit evaluation time + Sampling time + 1 Clock cycle delay.
8. Refer to ADC conversion table for detailed calculations.
9. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

3.18 Fast Ethernet Controller

MII signals use CMOS signal levels compatible with devices operating at 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

3.18.1 MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency in 2:1 mode and two times the RX_CLK frequency in 1:1 mode.

Table 45. MII Receive Signal Timing

Spec	Characteristic	Min	Max	Unit
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

Figure 21. MII receive signal timing diagram

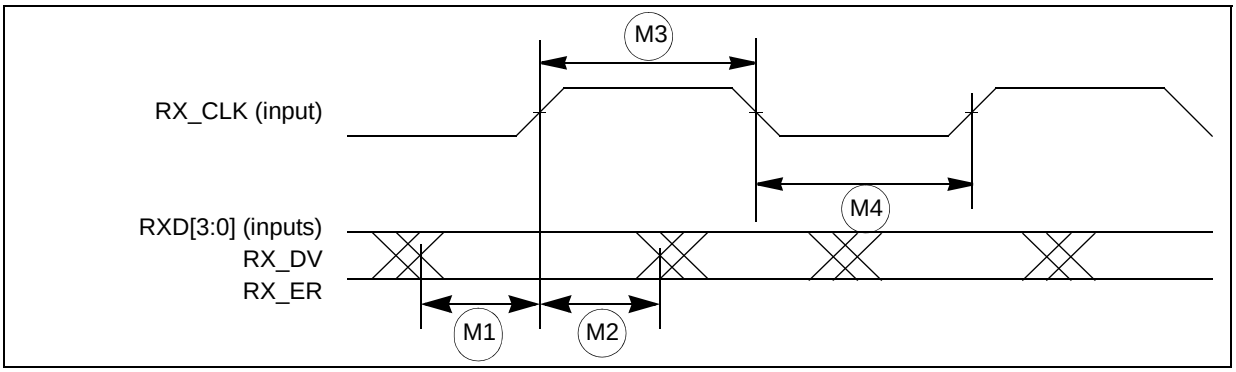
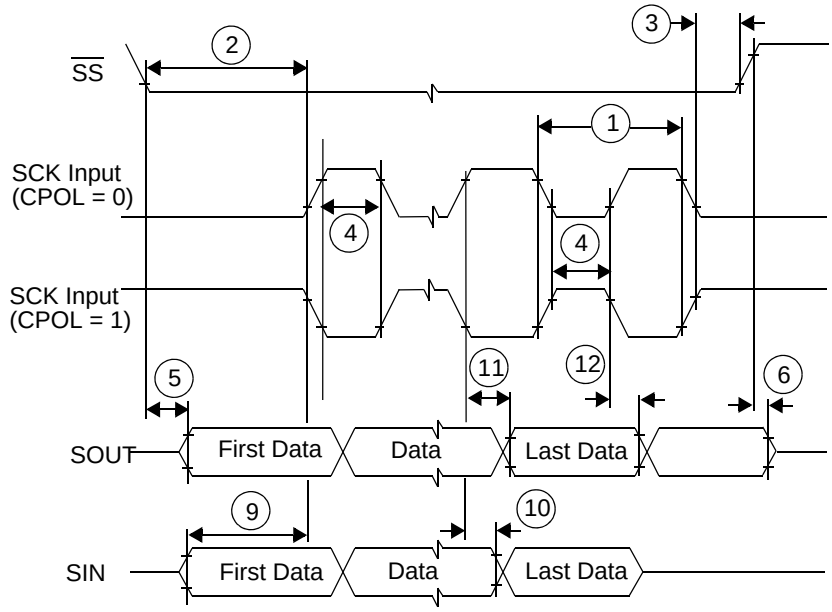
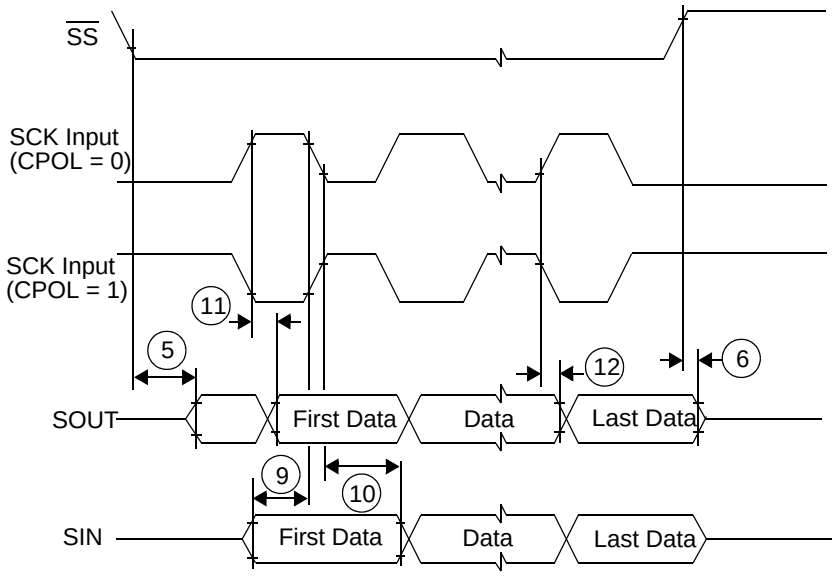


Figure 31. DSPI modified transfer format timing–slave, CPHA = 0



Note: Numbers shown reference *Table 50*.

Figure 32. DSPI modified transfer format timing–slave, CPHA = 1



Note: Numbers shown reference *Table 50*.

Appendix A Abbreviations

Table 56 lists abbreviations used but not defined elsewhere in this document.

Table 56. Abbreviations

Abbreviation	Meaning
CS	Chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select