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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	199
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x10b, 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-LBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b74b3c9e0x

Table 1. Device summary

Package	Part number		
	1.5 MByte	2 MByte	3 MByte
LQFP176	SPC564B64L7 SPC56EC64L7	SPC564B70L7 SPC56EC70L7	SPC564B74L7 SPC56EC74L7
LQFP208	SPC564B64L8 SPC56EC64L8	SPC564B70L8 SPC56EC70L8	SPC564B74L8 SPC56EC74L8
LBGA256	SPC56EC64B3	SPC56EC70B3	SPC56EC74B3

Contents

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX E0UC[30] LIN0TX	SIUL FlexCAN_0 eMIOS_0 LINFlexD_0	I/O O I/O I	M/S	Tristate	39	39	L3
PB[1]	PCR[17]	AF0 AF1 AF2 — — —	GPIO[17] — E0UC[31] LIN0RX WKPU[4] CAN0RX	SIUL — eMIOS_0 LINFlexD_0 WKPU FlexCAN_0	I/O — I/O I I I	S	Tristate	40	40	M2
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA E0UC[30]	SIUL LINFlexD_0 I^2C eMIOS_0	I/O O I/O I/O	M/S	Tristate	176	208	A2
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] E0UC[31] SCL — WKPU[11] LIN0RX	SIUL eMIOS_0 I^2C — WKPU LINFlexD_0	I/O I/O I/O — I I	S	Tristate	1	1	D4
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 — —	GPI[20] — — — ADC0_P[0] ADC1_P[0]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	88	104	T16
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 — —	GPI[21] — — — ADC0_P[1] ADC1_P[1]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	91	107	N13

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 — —	GPI[57] — — — ADC0_P[13] ADC1_P[13]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	94	114	N16
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 — —	GPI[58] — — — ADC0_P[14] ADC1_P[14]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	95	115	M14
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 — —	GPI[59] — — — ADC0_P[15] ADC1_P[15]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	96	116	M15
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC0_S[4]	SIUL DSPI_0 eMIOS_0 — ADC_0	I/O O I/O — I	S	Tristate	100	120	L13
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ADC0_S[5]	SIUL DSPI_1 eMIOS_0 — ADC_0	I/O I/O I/O — I	S	Tristate	102	124	K14
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[62] CS1_1 E0UC[26] — FR_DBG[0] ADC0_S[6]	SIUL DSPI_1 eMIOS_0 — Flexray ADC_0	I/O O I/O — O I	S	Tristate	104	126	K13

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ADC0_S[9]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	64	80	T6
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ADC0_S[10]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	65	81	R6
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	66	82	R7
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	67	83	R8
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	68	84	P8
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	69	85	N8
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	S	Tristate	70	86	P9

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX —	SIUL eMIOS_0 LINFlexD_8 —	I/O I/O O —	S	Tristate	172	196	C5
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKPU[24] LIN8RX	SIUL eMIOS_0 — — WKPU LINFlexD_8	I/O I/O — — I I	S	Tristate	171	195	A4
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX —	SIUL eMIOS_0 LINFlexD_9 —	I/O I/O O —	S	Tristate	170	194	D6
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKPU[23] LIN9RX	SIUL eMIOS_0 — — WKPU LINFlexD_9	I/O I/O — — I I	S	Tristate	169	193	B5
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	M/S	Tristate	143	167	A12
PI[5]	PCR[133]	AF0 AF1 AF2 AF3 ALT4	GPIO[133] E1UC[29] SCK_4 CS2_5 CS2_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O O O	M/S	Tristate	142	166	D12
PI[6]	PCR[134]	AF0 AF1 AF2 AF3 ALT4	GPIO[134] E1UC[30] CS0_4 CS0_5 CS0_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O I/O I/O	S	Tristate	11	11	D2

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PJ[3]	PCR[147]	AF0 AF1 AF2 AF3 —	GPIO[147] CS1_5 CS1_6 CS1_7 ADC0_S[27]	SIUL DSPI_5 DSPI_6 DSPI_7 ADC_0	I/O O O O I	S	Tristate	71	87	P10
PJ[4]	PCR[148]	AF0 AF1 AF2 AF3	GPIO[148] SCK_5 E1UC[18] —	SIUL DSPI_5 eMIOS_1 —	I/O I/O I/O —	M/S	Tristate	5	5	D3
PJ[5]	PCR[149]	AF0 AF1 AF2 AF3 —	GPIO[149] — — — ADC0_S[28]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	113	N12
PJ[6]	PCR[150]	AF0 AF1 AF2 AF3 —	GPIO[150] — — — ADC0_S[29]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	112	N15
PJ[7]	PCR[151]	AF0 AF1 AF2 AF3 —	GPIO[151] — — — ADC0_S[30]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	111	P16
PJ[8]	PCR[152]	AF0 AF1 AF2 AF3 —	GPIO[152] — — — ADC0_S[31]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	110	P15
PJ[9]	PCR[153]	AF0 AF1 AF2 AF3 —	GPIO[153] — — — ADC1_S[8]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	68	P5

Table 9. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{RC_CTRL} (2)		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	S R	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
$V_{DD\_HV\_ADC0}$	S R	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_A}$ (3)	$V_{DD\_HV\_A}$ – 0.3	$V_{DD\_HV\_A}$+0.3	
$V_{DD\_HV\_ADC1}$ (4)	S R	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_A}$ 2	$V_{DD\_HV\_A}$–0.3	$V_{DD\_HV\_A}$+0.3	
V_{IN}	S R	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A/HV\_B}$	$V_{DD\_HV\_A/HV\_B}$– 0.3	$V_{DD\_HV\_A/HV\_B}$+ 0.3	V
I_{INJPAD}	S R	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	S R	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG} (5)	S R	Sum of all the static I/O current within a supply segment ($V_{DD\_HV\_A}$ or $V_{DD\_HV\_B}$)	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		64	
$T_{STORAGE}$	S R	Storage temperature	—	–55 (6)	150	°C

1. $V_{DD\_HV\_B}$ can be independently controlled from $V_{DD\_HV\_A}$. These can ramp up or ramp down in any order. Design is robust against any supply order.
2. This voltage is internally generated by the device and no external voltage should be supplied.
3. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.
4. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±300 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.
5. Any temperature beyond 125 °C should limit the current to 50 mA (max).
6. This is the storage temperature for the flash memory.

Note: Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN} > $V_{DD\_HV\_A/HV\_B}$ or V_{IN} < V_{SS_HV}), the voltage on pins with respect to ground (V_{SS_HV}) must not exceed the recommended values.

Table 18. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1],[2]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull	I_{OH} = –14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus outputs (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.6.4 Output pin transition times

Table 19. Output pin transition times

Symbol		C	Parameter	Conditions[1],[2]		Value[3]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[4] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10 %, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10 %, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	
T_{tr}	CC	D	Output transition time output pin[4] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10 %, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10 %, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	

Table 21. I/O consumption

Symbol		C	Parameter	Conditions[1],[2]		Value[3]			Unit
						Min	Typ	Max	
I_{SWTSLW}[4]	CC	D	Peak I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	19.9	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	15.5	
I_{SWTMED}[4]	CC	D	Peak I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	28.8	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16.3	
I_{SWTFST}[4]	CC	D	Peak I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	113.5	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	52.1	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.22	mA
				C_L = 25 pF, 4 MHz		—	—	3.13	
				C_L = 100 pF, 2 MHz		—	—	6.54	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.51	
				C_L = 25 pF, 4 MHz		—	—	2.14	
				C_L = 100 pF, 2 MHz		—	—	4.33	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.5	mA
				C_L = 25 pF, 40 MHz		—	—	13.32	
				C_L = 100 pF, 13 MHz		—	—	18.26	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4.91	
				C_L = 25 pF, 40 MHz		—	—	8.47	
				C_L = 100 pF, 13 MHz		—	—	10.94	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	21.05	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	55.77	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	34.89	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65[4]	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. V_{DD} as mentioned in the table is $V_{DD\_HV\_A}$/$V_{DD\_HV\_B}$.
3. All values need to be confirmed during device validation.
4. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

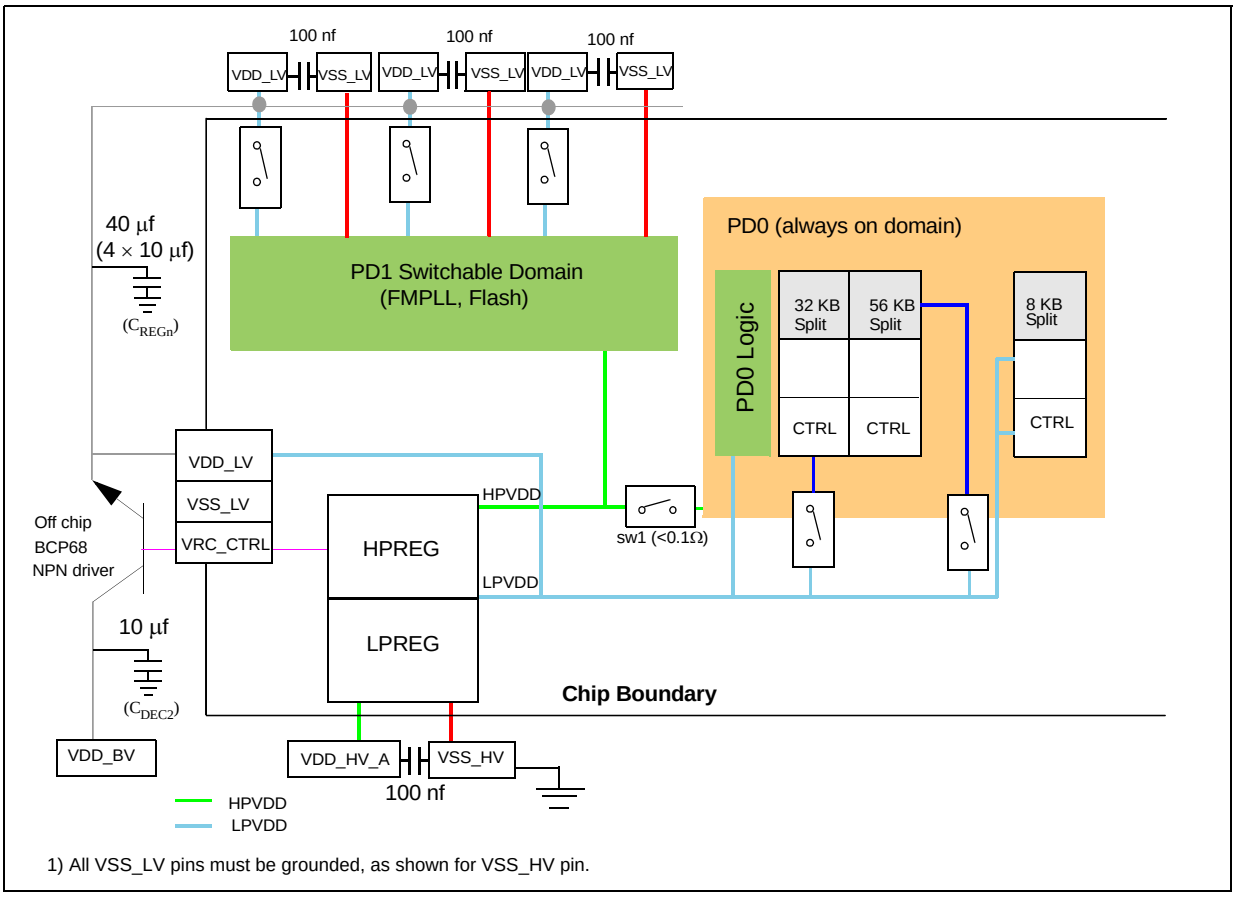
3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage supply $V_{DD\_HV\_A}$. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through $V_{DD\_HV\_A}$ power pin.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the on-chip VREG with an external ballast (BCP68 NPN device). It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV_CFLA0/CFLA1: Low voltage supply for the two code Flash modules. It is shorted with LV_COR through double bonding.
  - LV_DFLA: Low voltage supply for data Flash module. It is shorted with LV_COR through double bonding.
  - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

Figure 8. Voltage regulator capacitance connection



1) All VSS_LV pins must be grounded, as shown for VSS_HV pin.

Table 23. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	350	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low power regulator output voltage	After trimming T_A = 25 °C	1.17	1.27	1.32	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	50	mA
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	20	—	
$I_{VREGREF}$	CC	D	Main LVDs and reference current consumption (low power and main regulator switched off)	T_A = 55 °C	—	2	—	µA
$I_{VREDLVD12}$	CC	D	Main LVD current consumption (switch-off during standby)	T_A = 55 °C	—	1	—	µA
$I_{DD\_HV\_A}$	CC	D	In-rush current on V_{DD_BV} during power-up	—	—	—	600 (3)	mA

1. $V_{DD\_HV\_A}$ = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Inrush current is seen more like steps of 600 mA peak. The startup of the regulator happens in steps of 50 mV in ~25 steps to reach ~1.2 V V_{DD_LV}. Each step peak current is within 600 mA

3.8.3 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the $V_{DD\_HV\_A}$ and the V_{DD_LV} voltage while device is supplied:

- POR monitors $V_{DD\_HV\_A}$ during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors $V_{DD\_HV\_A}$ to ensure device is reset below minimum functional supply
- LVDHV5 monitors $V_{DD\_HV\_A}$ when application uses device in the 5.0 V±10 % range
- LVDLVCOR monitors power domain No. 1 (PD1)
- LVDLVBKP monitors power domain No. 0 (PD0). VDD_LV is same as PD0 supply.

Note: When enabled, PD2 (RAM retention) is monitored through LVD_DIGBKP.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 29. Flash memory read access timing(1)

Symbol		C	Parameter	Conditions(2)		Frequency range	Unit
				Code flash memory	Data flash memory		
f_{READ}	CC	P	Maximum frequency for Flash reading	5 wait states	13 wait states	120 —100	MHz
		C		4 wait states	11 wait states	100—80	
		D		3 wait states	9 wait states	80—64	
		C		2 wait states	7 wait states	64—40	
		C		1 wait states	4 wait states	40—20	
		C		0 wait states	2 wait states	20—0	

1. Max speed is the maximum speed allowed including PLL frequency modulation (FM).
2. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.

3.10.2 Flash memory power supply DC characteristics

Table 30 shows the flash memory power supply DC characteristics on external supply.

Table 30. Flash memory power supply DC electrical characteristics

Symbol		Parameter	Conditions(1)		Value(2)			Unit
					Min	Typ	Max	
I_{CFREAD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ on read access	Flash memory module read f_{CPU} = 120 MHz + 2%(4)	Code flash memory			33	mA
I_{DFREAD}(3)				Data flash memory			13	
I_{CFMOD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ (program/erase)	Program/Erase on-going while reading flash memory registers f_{CPU} = 120 MHz + 2% (4)	Code flash memory			52	mA
I_{DFMOD}(3)				Data flash memory			13	
I_{CFLPW}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ during flash memory low power mode		Code flash memory			1.1	mA
I_{CFPWD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ during flash memory power down mode		Code flash memory			150	µA
I_{DFPWD}(3)				Data flash memory			150	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Data based on characterization results, not tested in production.
4. f_{CPU} 120 MHz + 2 % can be achieved over full temperature 125 °C ambient, 150 °C junction temperature.

3.10.3 Flash memory start-up/switch-off timings

Table 31. Start-up time/Switch-off time

Symbol		C	Parameter		Conditions (1)	Value			Unit
						Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	D	Delay for flash memory module to exit reset mode	Code flash memory	—	—	—	125	µs
				Data flash memory		—	—		
$T_{FLALPEXIT}$	CC	T	Delay for flash memory module to exit low-power mode	Code flash memory	—	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for flash memory module to exit power-down mode	Code flash memory	—	—	—	30	
				Data flash memory		—	—		
$T_{FLALPENTRY}$	CC	T	Delay for flash memory module to enter low-power mode	Code flash memory	—	—	—	0.5	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.

3.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and pre-qualification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers)
- Pre-qualification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note *Software Techniques For Improving Microcontroller EMC Performance* (AN1015)).

Table 36. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics (continued)

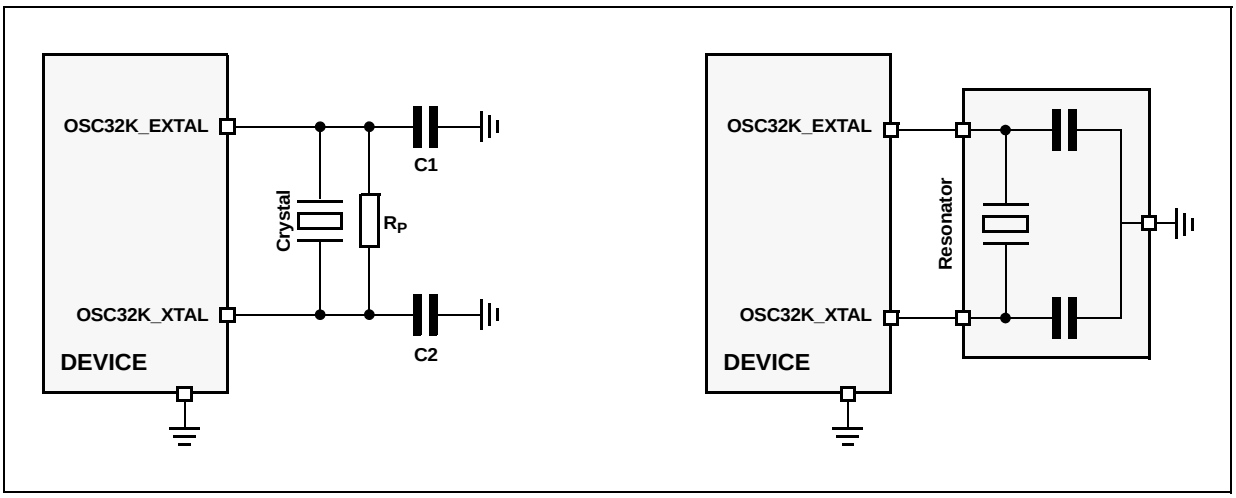
Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD\_HV\_A}$	—	$V_{DD\_HV\_A}$ + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	–0.3	—	$0.35V_{DD\_HV\_A}$	V

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Based on ATE Cz
4. Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

3.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

Figure 12. Crystal oscillator and resonator connection scheme



Note: OSC32K_XTAL/OSC32K_EXTAL must not be directly used to drive external circuits.

Table 40. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
$I_{FIRCRUN}$[3]	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed		—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C		—	—	100	nA
		D		T_A = 55 °C		—	—	200	nA
		D		T_A = 125 °C		—	—	1	µA
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
T_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	T_A = 55 °C	V_{DD} = 5.0 V ± 10%	—	—	2.0	µs
		—			V_{DD} = 3.3 V ± 10%	—	—	5	
		—		T_A = 125 °C	V_{DD} = 5.0 V ± 10%	—	—	2.0	
		—			V_{DD} = 3.3 V ± 10%	—	—	5	
$\Delta_{FIRCPRE}$	CC	C	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C		–1	—	+1	%
$\Delta_{FIRCTRIM}$	CC	C	Fast internal RC oscillator trimming step	T_A = 25 °C		—	1.6		%
$\Delta_{FIRCVAR}$	CC	C	Fast internal RC oscillator variation over temperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	—		–5	—	+5	%

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

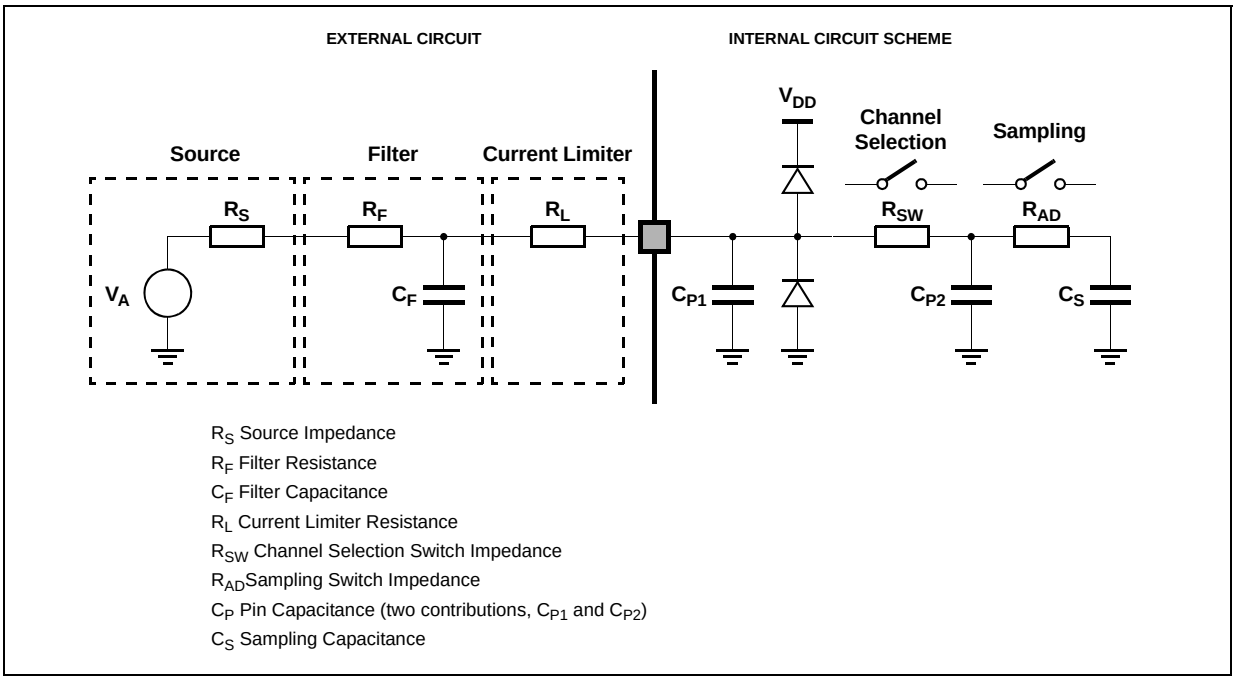
In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being CS and Cp_2 substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1MHz, with CS+Cp_2 equal to 3pF, a resistance of 330KΩ is obtained (Reqiv = 1 / (fc*(CS+Cp_2)), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on CS+Cp_2) and the sum of R_S + R_F, the external circuit must be designed to respect the following relation

Equation 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

The formula above provides a constraint for external network design, in particular on resistive path.

Figure 16. Input equivalent circuit (precise channels)



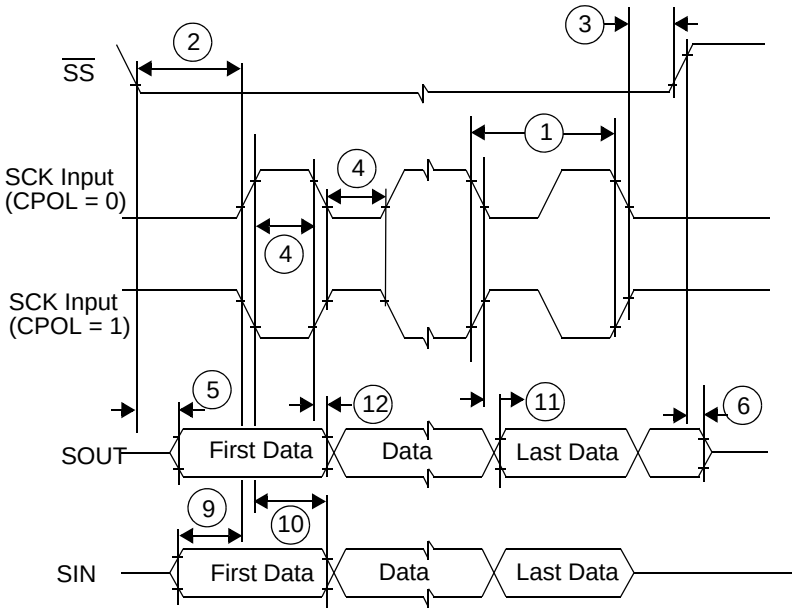
R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW} Channel Selection Switch Impedance
R_{AD}Sampling Switch Impedance
C_P Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S Sampling Capacitance

Table 50. DSPI timing (continued)

Spec	Characteristic	Symbol	Value		Unit
			Min	Max	
—	Slave Setup Time ($\overline{SS}$ active to SCK setup time)	t_{SUSS}	5	—	ns
—	Slave Hold Time ($\overline{SS}$ active to SCK hold time)	t_{HSS}	10	—	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)(4)	t_A	—	42	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	CSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns
9	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)(5) Master (MTFE = 1, CPHA = 1)	t_{SUI}	 36 5 36 36	 — — — —	 ns ns ns ns
10	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)(5) Master (MTFE = 1, CPHA = 1)	t_{HI}	 0 4 0 0	 — — — —	 ns ns ns ns
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{SUO}	 — — — —	 12 37 12 12	 ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{HO}	 0(6) 9.5 0(7) 0(8)	 — — — —	 ns ns ns ns

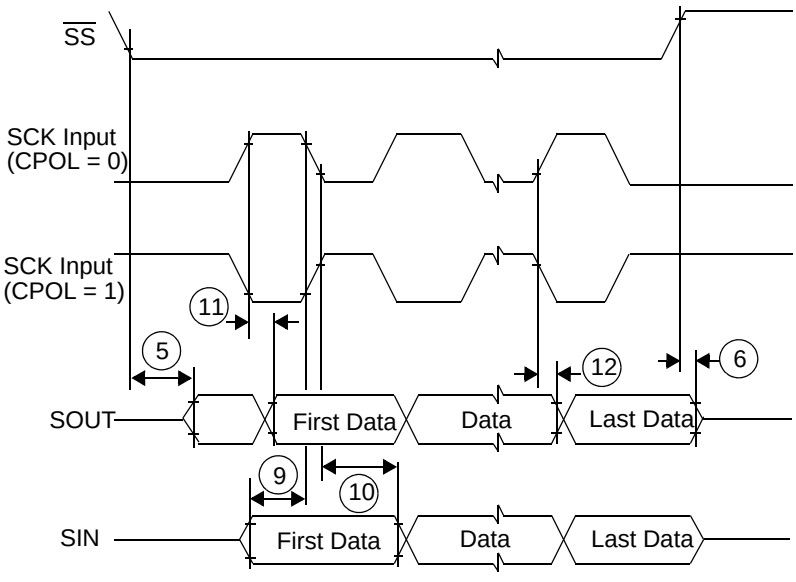
1. This value of this parameter is dependent upon the external device delays and the other parameters mentioned in this table.
2. The maximum value is programmable in DSPI_CTAR*n* [PSSCK] and DSPI_CTAR*n* [CSSCK]. For SPC564B74 and SPC56EC74, the spec value of t_{CSC} will be attained only if T_{DSPI} x PSSCK x CSSCK > Δt_{CSC}.
3. The maximum value is programmable in DSPI_CTAR*n* [PASC] and DSPI_CTAR*n* [ASC]. For SPC564B74 and SPC56EC74, the spec value of t_{ASC} will be attained only if T_{DSPI} x PASC x ASC > Δt_{ASC}.
4. The parameter value is obtained from t_{SUSS} and t_{SUO} for slave.
5. This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b00.
6. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 0) is –2 ns.
7. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 1, CPHA = 0) is –2 n.
8. For DSPI1, the Data Hold Time for Outputs in Master (MTFE = 1, CPHA = 1) is –2 ns.

Figure 27. DSPI classic SPI timing–slave, CPHA = 0



Note: Numbers shown reference *Table 50*.

Figure 28. DSPI classic SPI timing–slave, CPHA = 1



Note: Numbers shown reference *Table 50*.

Table 57. Revision history (continued)

Date	Revision	Changes
01-Dec-2011	4	– Interchanged the denominator with numerator in Equation 11 of Input impedance and ADC accuracy section – Removed the note (All ADC conversion characteristics described in the table below are applicable only for the precision channels. The data for semi-precision and extended channels is awaited and same will be subsequently updated in later revs.) in the ADC electrical characteristics section. – *Table 49* (On-chip peripherals current consumption). Replaced IDD_HV_ADC with IDD_HV_ADC0 and IDD_HV_ADC1 values as per ADC specs – In *Table 43*, the minimum sample time of ADC0 changed to 500 at 32 MHz – In *Table 43*, removed the entry for sample time at 30 MHz – In *Table 44*, changed TUEX to TUES and INLX to INLS (Extended channels are not supported by the device. So, changed to standard channel.)
04-Mar-2013	5	– Updated the pins 23 and 24 of *Figure 2: 176-pin LQFP configuration*. – Updated unit of measure in *Table 44: Conversion characteristics (12-bit ADC_1)* – Modified the value to typical value in *Table 49: On-chip peripherals current consumption* – Added footnote to t_{ESRT} parameter in *Table 26: Code flash memory—Program and erase specifications* – Added footnote to t_{ESRT} parameter in *Table 27: Data flash memory—Program and erase specifications* – Updated *Table 29: Flash memory read access timing*. – Updated Notes 2 and Notes 3 of *Table 10: Recommended operating conditions (3.3 V)* and *Table 11: Recommended operating conditions (5.0 V)* respectively. – Updated the footnote1 of *Table 10: Recommended operating conditions (3.3 V)* and *Table 11: Recommended operating conditions (5.0 V)* – Updated $V_{DD\_HV\_A}$ to V_{DD_BV} for C_{DEC2} and $I_{DD\_HV\_A}$ in *Table 23: Voltage regulator electrical characteristics* and deleted footnote3 – Updated the dedicated number of channels for 12-bit ADC in family comparison tables – Updated the values of $f_{SIRC,}$ parameters and conditions of $\Delta_{SIRCVAR}$ in *Table 41: Slow internal RC oscillator (128 kHz) electrical characteristics* – Updated second footnote in *Table 11: Recommended operating conditions (5.0 V)*, – Updated the value of t_{ADC0_PU} in *Table 43: ADC conversion characteristics (10-bit ADC_0)* – Updated the IDD values in *Table 25: Low voltage power domain electrical characteristics* – Added footnote to *Table 25: Low voltage power domain electrical characteristics* related to current drawn from $V_{DD\_HV\_A}$ and $V_{DD\_HV\_B}$ – Updated entire *Section 3.17.1.1: Input impedance and ADC accuracy* – Updated the values of VLPREG in *Table 23: Voltage regulator electrical characteristics*. – Updated the values of V_{LPREG} in *Table 23: Voltage regulator electrical characteristics*. – Added T_A = 25 °C, min and max values of V_{MREG} in *Table 23: Voltage regulator electrical characteristics* – Added T_A = 25 °C, min and max values of V_{LPREG} in *Table 23: Voltage regulator electrical characteristics*