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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b74l7b8e0x

Table 1. Device summary

Package	Part number		
	1.5 MByte	2 MByte	3 MByte
LQFP176	SPC564B64L7 SPC56EC64L7	SPC564B70L7 SPC56EC70L7	SPC564B74L7 SPC56EC74L7
LQFP208	SPC564B64L8 SPC56EC64L8	SPC564B70L8 SPC56EC70L8	SPC564B74L8 SPC56EC74L8
LBGA256	SPC56EC64B3	SPC56EC70B3	SPC56EC74B3

Table 2. SPC564Bxx and SPC56ECxx family comparison[1] (continued)

Feature	SPC564B64		SPC56EC64			SPC564B70		SPC56EC70			SPC564B74		SPC56EC74		
Package	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256
FlexRay	Yes														
STCU[11]	Yes														
Ethernet	No		Yes			No		Yes			No		Yes		
I^2C	1														
32 kHz oscillator (SXOSC)	Yes														
GPIO[12]	147	177	147	177	199	147	177	147	177	199	147	177	147	177	199
Debug	JTAG				Nexus 3+	JTAG				Nexus 3+	JTAG				Nexus 3+
Cryptographic Services Engine (CSE)	Optional														

1. Feature set dependent on selected peripheral multiplexing; table shows example.
2. Based on 125 °C ambient operating temperature and subject to full device characterization.
3. The e200z0h can run at speeds up to 80 MHz. However, if system frequency is >80 MHz (e.g., e200z4d running at 120 MHz) the e200z0h needs to run at 1/2 system frequency. There is a configurable e200z0 system clock divider for this purpose.
4. DMAMUX also included that allows for software selection of 32 out of a possible 57 sources.
5. Not shared with 12-bit ADC, but possibly shared with other alternate functions.
6. There are 23 dedicated ANS plus 4 dedicated ANX channels on LQPF176. For higher pin count packages, there are 29 dedicated ANS plus 4 dedicated ANX channels.
7. 16x precision channels (ANP) and 3x standard (ANS).
8. Not shared with 10-bit ADC, but possibly shared with other alternate functions.
9. As a minimum, all timer channels can function as PWM or Input Capture and Output Control. Refer to the eMIOS section of the device reference manual for information on the channel configuration and functions.
10. CAN Sampler also included that allows ID of CAN message to be captured when in low power mode.
11. STCU controls MBIST activation and reporting.
12. Estimated I/O count for proposed packages based on multiplexing with peripherals.

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ADC0_S[9]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	64	80	T6
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ADC0_S[10]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	65	81	R6
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	66	82	R7
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	67	83	R8
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	S	Tristate	68	84	P8
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	S	Tristate	69	85	N8
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	S	Tristate	70	86	P9

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PG[10]	PCR[106]	AF0 AF1 AF2 AF3 —	GPIO[106] E0UC[24] E1UC[31] — SIN_4	SIUL eMIOS_0 eMIOS_1 — DSPI_4	I/O I/O I/O — I	S	Tristate	138	162	B13
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] CS0_4 CS0_6	SIUL eMIOS_0 DSPI_4 DSPI_6	I/O I/O I/O I/O	M/S	Tristate	139	163	A16
PG[12]	PCR[108]	AF0 AF1 AF2 AF3 ALT4	GPIO[108] E0UC[26] SOUT_4 — TXD[2]	SIUL eMIOS_0 DSPI_4 — FEC	I/O I/O O — O	M/S	Tristate	116	140	F15
PG[13]	PCR[109]	AF0 AF1 AF2 AF3 ALT4	GPIO[109] E0UC[27] SCK_4 — TXD[3]	SIUL eMIOS_0 DSPI_4 — FEC	I/O I/O I/O — O	M/S	Tristate	115	139	F16
PG[14]	PCR[110]	AF0 AF1 AF2 AF3 —	GPIO[110] E1UC[0] LIN8TX — SIN_6	SIUL eMIOS_1 LINFlexD_8 — DSPI_6	I/O I/O O — I	S	Tristate	134	158	C13
PG[15]	PCR[111]	AF0 AF1 AF2 AF3 —	GPIO[111] E1UC[1] SOUT_6 — LIN8RX	SIUL eMIOS_1 DSPI_6 — LINFlexD_8	I/O I/O O — I	M/S	Tristate	135	159	D13
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[112] E1UC[2] — — TXD[1] SIN_1	SIUL eMIOS_1 — — FEC DSPI_1	I/O I/O — — O I	M/S	Tristate	117	141	E15

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PH[1]	PCR[113]	AF0 AF1 AF2 AF3 ALT4	GPIO[113] E1UC[3] SOUT_1 — TXD[0]	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O O — O	M/S	Tristate	118	142	F13
PH[2]	PCR[114]	AF0 AF1 AF2 AF3 ALT4	GPIO[114] E1UC[4] SCK_1 — TX_EN	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O I/O — O	M/S	Tristate	119	143	D16
PH[3]	PCR[115]	AF0 AF1 AF2 AF3 ALT4	GPIO[115] E1UC[5] CS0_1 — TX_ER	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O I/O — O	M/S	Tristate	120	144	F14
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] SOUT_7 —	SIUL eMIOS_1 DSPI_7 —	I/O I/O O —	M/S	Tristate	162	186	D7
PH[5]	PCR[117]	AF0 AF1 AF2 AF3 —	GPIO[117] E1UC[7] — — SIN_7	SIUL eMIOS_1 — — DSPI_7	I/O I/O — — I	S	Tristate	163	187	B7
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] SCK_7 MA[2]	SIUL eMIOS_1 DSPI_7 ADC_0	I/O I/O I/O O	M/S	Tristate	164	188	C7
PH[7]	PCR[119]	AF0 AF1 AF2 AF3 ALT4	GPIO[119] E1UC[9] CS3_2 MA[1] CS0_7	SIUL eMIOS_1 DSPI_2 ADC_0 DSPI_7	I/O I/O O O I/O	M/S	Tristate	165	189	C6

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PK[7]	PCR[167]	AF0 AF1 AF2 AF3 — —	GPIO[167] — — — CAN3RX LIN3RX	SIUL — — — FlexCAN_3 LINFlexD_3	I/O — — — I I	M/S	Tristate	—	47	M7
PK[8]	PCR[168]	AF0 AF1 AF2 AF3	GPIO[168] CAN3TX LIN3TX —	SIUL FlexCAN_3 LINFlexD_3 —	I/O O O —	M/S	Tristate	—	48	M8
PK[9]	PCR[169]	AF0 AF1 AF2 AF3 —	GPIO[169] — — — SIN_4	SIUL — — — DSPI_4	I/O — — — I	M/S	Tristate	—	197	E8
PK[10]	PCR[170]	AF0 AF1 AF2 AF3	GPIO[170] SOUT_4 — —	SIUL DSPI_4 — —	I/O O — —	M/S	Tristate	—	198	E7
PK[11]	PCR[171]	AF0 AF1 AF2 AF3	GPIO[171] SCK_4 — —	SIUL DSPI_4 — —	I/O I/O — —	M/S	Tristate	—	199	F8
PK[12]	PCR[172]	AF0 AF1 AF2 AF3	GPIO[172] CS0_4 — —	SIUL DSPI_4 — —	I/O I/O — —	M/S	Tristate	—	200	G12
PK[13]	PCR[173]	AF0 AF1 AF2 AF3 —	GPIO[173] CS3_6 CS2_7 SCK_1 CAN3RX	SIUL DSPI_6 DSPI_7 DSPI_1 FlexCAN_3	I/O O O I/O I	M/S	Tristate	—	201	H12

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PL[6]	PCR[182]	AF0 AF1 AF2 AF3	GPIO[182] — MDO4 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	K5
PL[7]	PCR[183]	AF0 AF1 AF2 AF3	GPIO[183] — MDO5 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	L5
PL[8]	PCR[184]	AF0 AF1 AF2 AF3 —	GPIO[184] — — — EVTI	SIUL — — — Nexus	I/O — — — I	S	Pull-up	—	—	M9
PL[9]	PCR[185]	AF0 AF1 AF2 AF3	GPIO[185] — MSEO —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	M10
PL[10]	PCR[186]	AF0 AF1 AF2 AF3	GPIO[186] — MCKO —	SIUL — Nexus —	I/O — O —	F/S	Tristate	—	—	M11
PL[11]	PCR[187]	AF0 AF1 AF2 AF3	GPIO[187] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	M12
PL[12]	PCR[188]	AF0 AF1 AF2 AF3	GPIO[188] — EVTO —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F11
PL[13]	PCR[189]	AF0 AF1 AF2 AF3	GPIO[189] — MDO6 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F10

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PL[14]	PCR[190]	AF0 AF1 AF2 AF3	GPIO[190] — MDO7 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E12
PL[15]	PCR[191]	AF0 AF1 AF2 AF3	GPIO[191] — MDO8 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E11
PM[0]	PCR[192]	AF0 AF1 AF2 AF3	GPIO[192] — MDO9 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E10
PM[1]	PCR[193]	AF0 AF1 AF2 AF3	GPIO[193] — MDO10 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	E9
PM[2]	PCR[194]	AF0 AF1 AF2 AF3	GPIO[194] — MDO11 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F12
PM[3]	PCR[195]	AF0 AF1 AF2 AF3	GPIO[195] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	K12
PM[4]	PCR[196]	AF0 AF1 AF2 AF3	GPIO[196] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	L12

8. Guaranteed by device validation.

Note: SRAM retention guaranteed to LVD levels.

3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 12. LQFP thermal characteristics(1)

Symbol		C	Parameter	Conditions(2)	Pin count	Value(3)			Unit
						Min	Typ	Max	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	176	—	—	44.4(4)	°C/W
					208	—	—	43	°C/W
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection	Four-layer board—2s2p(5)	176	—	—	36.1	°C/W
					208	—	—	33.9	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C.
3. All values need to be confirmed during device validation.
4. 1s board as per standard JEDEC (JESD51-7) in natural convection.
5. 2s2p board as per standard JEDEC (JESD51-7) in natural convection.

Table 13. LBGA256 thermal characteristics(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	—	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	44.3	°C/W
				Four-layer board—2s2p	31	

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.

9. Subject to change, Configuration: 1 × e200z4d + 4 kbit/s Cache, 1 × e200z0h (1/2 system frequency), CSE, 1 × eDMA (10 ch.), 6 × FlexCAN (4 × 500 kbit/s, 2 × 125 kbit/s), 4 × LINFlexD (20 kbit/s), 6 × DSPI (2 × 2 Mbit/s, 3 × 4 Mbit/s, 1 × 10 Mbit/s), 16 × Timed I/O, 16 × ADC Input, 1 × FlexRay (2 ch., 10 Mbit/s), 1 × FEC (100 Mbit/s), 1 × RTC, 4 PIT channels, 1 × SWT, 1 × STM. For lower pin count packages reduce the amount of timed I/O's and ADC channels. RUN current measured with typical application with accesses on both code flash and RAM.
10. This value is obtained from limited sample set.
11. Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz ON. 16 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but no reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3-9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]-PA[11] and PC[12]-PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication, instance: 1-7 clocks gated). RTC/API ON. PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.
12. Only for the "P" classification: No clock, FIRC 16 MHz OFF, SIRC128 kHz ON, PLL OFF, HPvreg OFF, LPVreg ON. All possible peripherals off and clock gated. Flash in power down mode.
13. Only for the "P" classification: LPreg ON, HPVreg OFF, 96 KB RAM ON, device configured for minimum consumption, all possible modules switched-off. Measurement condition assumes T_j = Ta.
14. LPreg ON, HPVreg OFF, 64 KB RAM ON, device configured for minimum consumption, all possible modules switched-off. Measurement condition assumes T_j = Ta.
15. LPreg ON, HPVreg OFF, 8 KB RAM ON, device configured for minimum consumption, all possible modules switched OFF. Measurement condition assumes T_j = Ta.

3.10 Flash memory electrical characteristics

3.10.1 Program/Erase characteristics

Table 26 shows the code flash memory program and erase characteristics.

Table 26. Code flash memory—Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ(1)	Initial max(2)	Max(3)	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time(4)	—	18	50	500	µs
$T_{16Kpperase}$			16 KB block pre-program and erase time	—	200	500	5000	ms
$T_{32Kpperase}$			32 KB block pre-program and erase time	—	300	600	5000	ms
$T_{128Kpperase}$			128 KB block pre-program and erase time	—	600	1300	5000	ms
T_{eslat}		D	Erase Suspend Latency	—	—	30	30	µs
t_{ESRT}(5)		C	Erase Suspend Request Rate	20	—	—	—	ms
t_{PABT}		D	Program Abort Latency	—	—	10	10	µs
t_{EAPT}		D	Erase Abort Latency	—	—	30	30	µs

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. It is Time between erase suspend resume and the next erase suspend request.

Table 27 shows the data flash memory program and erase characteristics.

Figure 11. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

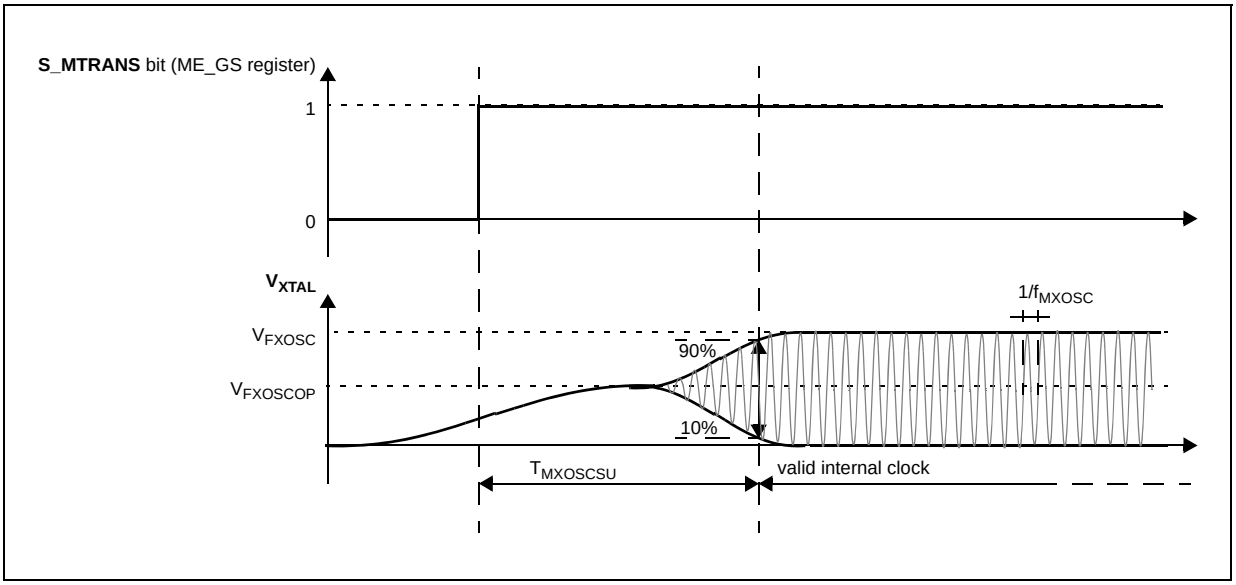


Table 36. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	40.0	MHz
g_{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%	4[3]	—	20[3]	mA/V
				V_{DD} = 5.0 V ± 10%	6.5[3]	—	25[3]	
V_{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f_{OSC} = 40 MHz For both V_{DD} = 3.3 V ± 10%, V_{DD} = 5.0 V ± 10%	—	0.95	—	V
$V_{FXOSCOP}$	CC	P	Oscillation operating point	—	—	1.8		V
I_{FXOSC}[4]	CC	T	Fast external crystal oscillator consumption	V_{DD} = 3.3 V ± 10%, f_{OSC} = 40 MHz	—	2	2.2	mA
				V_{DD} = 5.0 V ± 10%, f_{OSC} = 40 MHz	—	2.3	2.5	
				V_{DD} = 3.3 V ± 10%, f_{OSC} = 16 MHz	—	1.3	1.5	
				V_{DD} = 5.0 V ± 10%, f_{OSC} = 16 MHz	—	1.6	1.8	
$T_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 40 MHz For both V_{DD} = 3.3 V ± 10%, V_{DD} = 5.0 V ± 10%	—	—	5	ms

Figure 13. Equivalent circuit of a quartz crystal

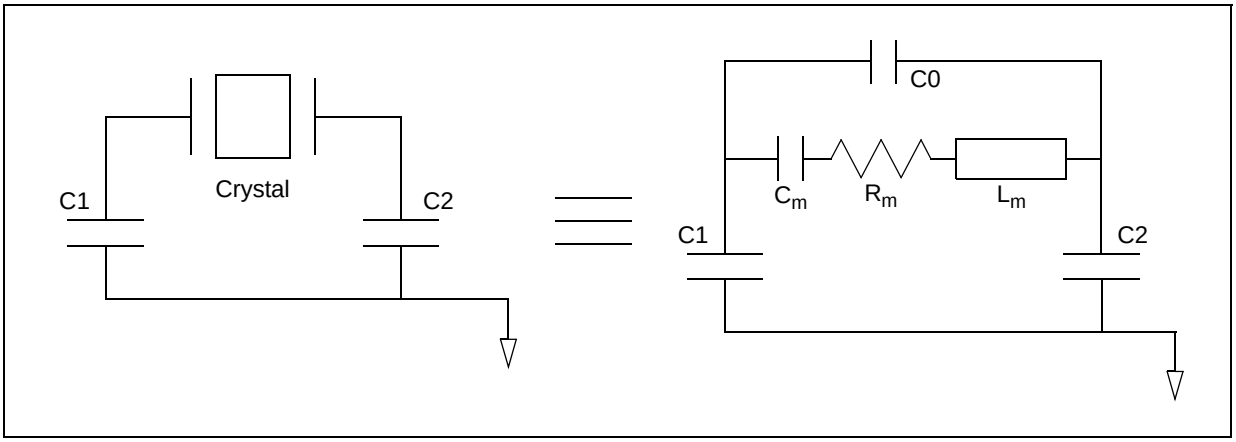


Table 37. Crystal motional characteristics(1)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground(2)	—	18	—	28	pF
R_m(3)	Motional resistance	AC coupled @ C0 = 2.85 pF(4)	—	—	65	kW
		AC coupled @ C0 = 4.9 pF(4)	—	—	50	
		AC coupled @ C0 = 7.0 pF(4)	—	—	35	
		AC coupled @ C0 = 9.0 pF(4)	—	—	30	

1. The crystal used is Epson Toyocom MC306.
2. This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.
3. Maximum ESR (R_m) of the crystal is 50 kΩ.
4. C0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

3.14 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 39. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[3]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[3]	—	40	—	60	%
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	120	MHz
f_{CPU}	SR	—	System clock frequency	—	—	—	120 + 2%[4]	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 40 MHz (resonator), f_{PLLCLK} @ 120 MHz, 4000 cycles	—	—	6 (for < 1ppm)	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	3	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. PLLIN clock retrieved directly from 4-40 MHz XOSC or 16 MIRC. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
4. f_{CPU} 120 + 2% MHz can be achieved at 125 °C.

3.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device and can also be used as input to PLL.

Table 40. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	

Table 49. On-chip peripherals current consumption(1)

Symbol		C	Parameter	Conditions		Value(2) Typ	Unit
IDD_HV_ADC0	CC	D	ADC_0 supply current on $V_{DD\_HV\_ADC0}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	200	µA
					Analog dynamic consumption (continuous conversion)	4	mA
IDD_HV_ADC1	CC	D	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300	µA
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	6	mA
$I_{DD\_HV(FLASH)}$	CC	D	CFlash + DFlash supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	—	13.25	mA
$I_{DD\_HV(PLL)}$	CC	D	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	0.0031 × f_{periph}	

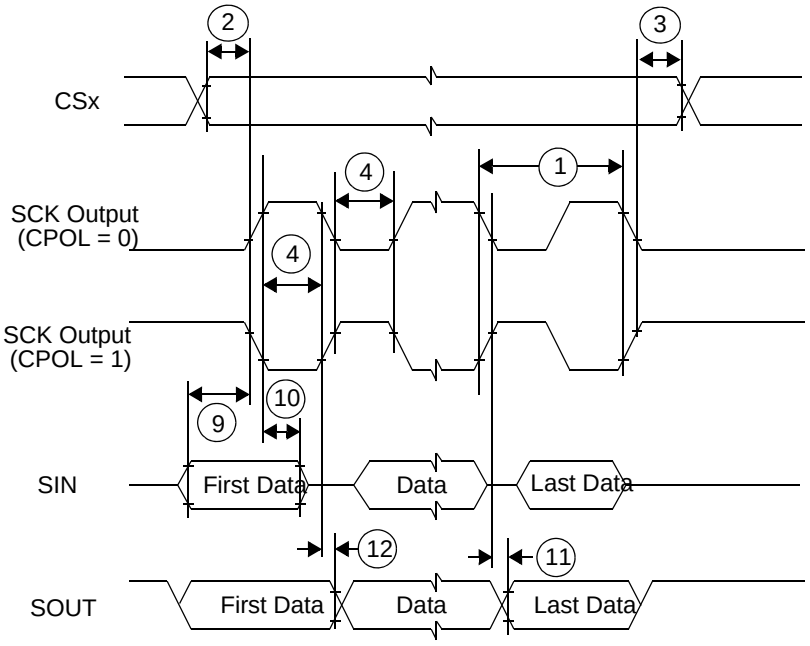
1. Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 120 MHz.
2. f_{periph} is in absolute value.

3.19.2 DSPI characteristics

Table 50. DSPI timing

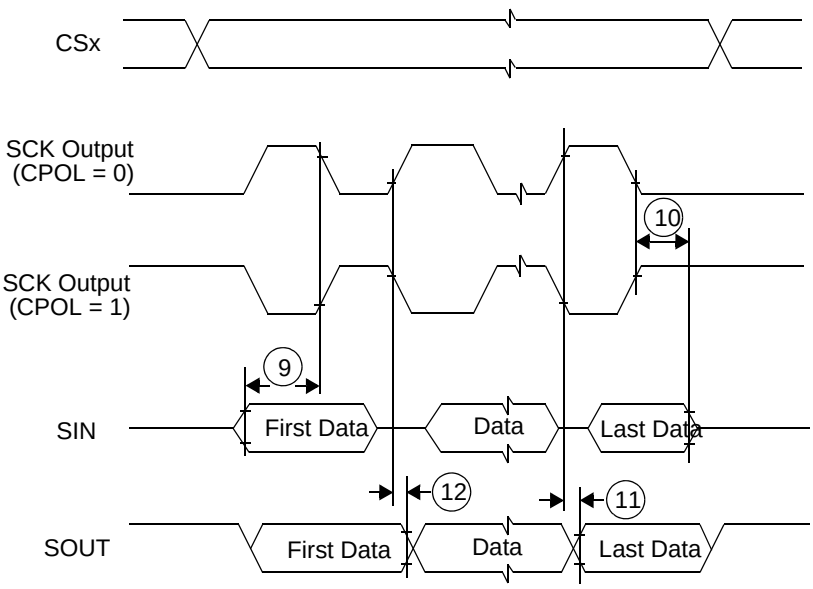
Spec	Characteristic	Symbol	Value Min	Value Max	Unit
1	DSPI Cycle Time	t_{SCK}	Refer note(1)	—	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Δt_{CSC}	—	115	ns
—	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Δt_{ASC}	15	—	ns
2	CS to SCK Delay(2)	t_{CSC}	7	—	ns
3	After SCK Delay(3)	t_{ASC}	15	—	ns
4	SCK Duty Cycle	t_{SDC}	0.4 × t_{SCK}	0.6 × t_{SCK}	ns

Figure 25. DSPI classic SPI timing–master, CPHA = 0



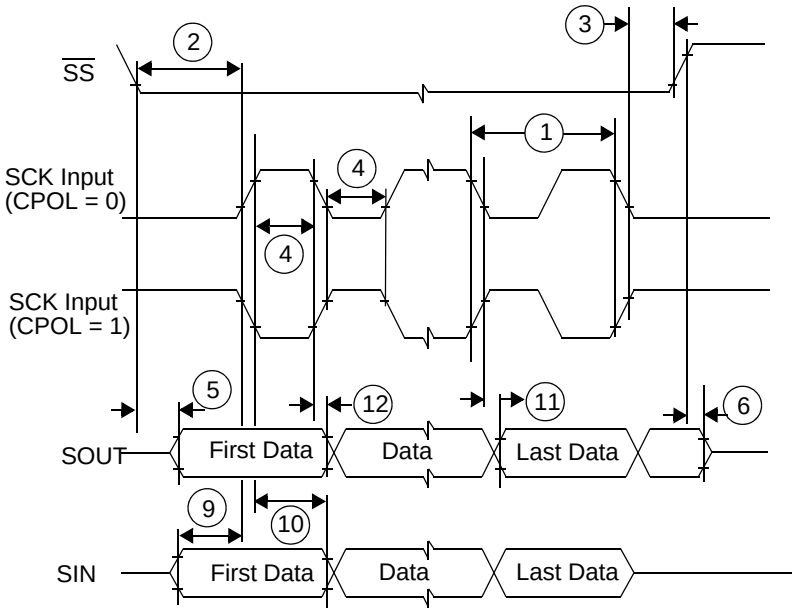
Note: Numbers shown reference *Table 50*.

Figure 26. DSPI classic SPI timing–master, CPHA = 1



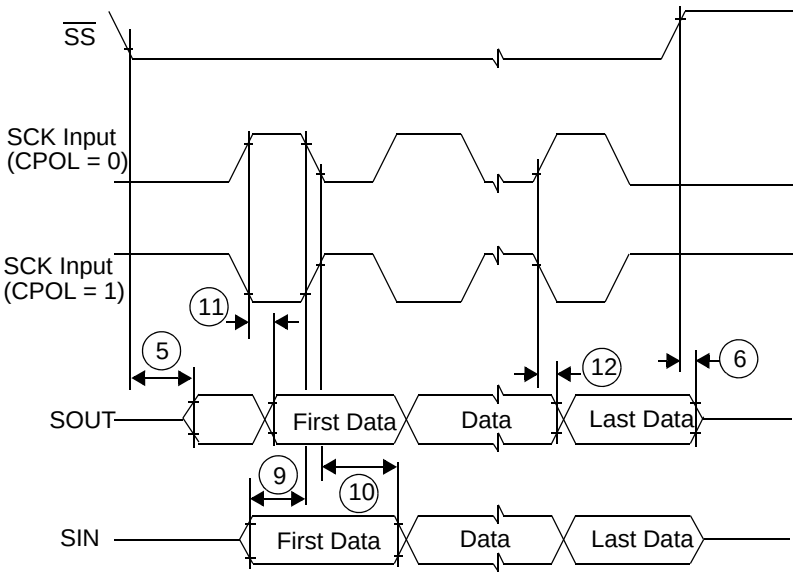
Note: Numbers shown reference *Table 50*.

Figure 27. DSPI classic SPI timing–slave, CPHA = 0



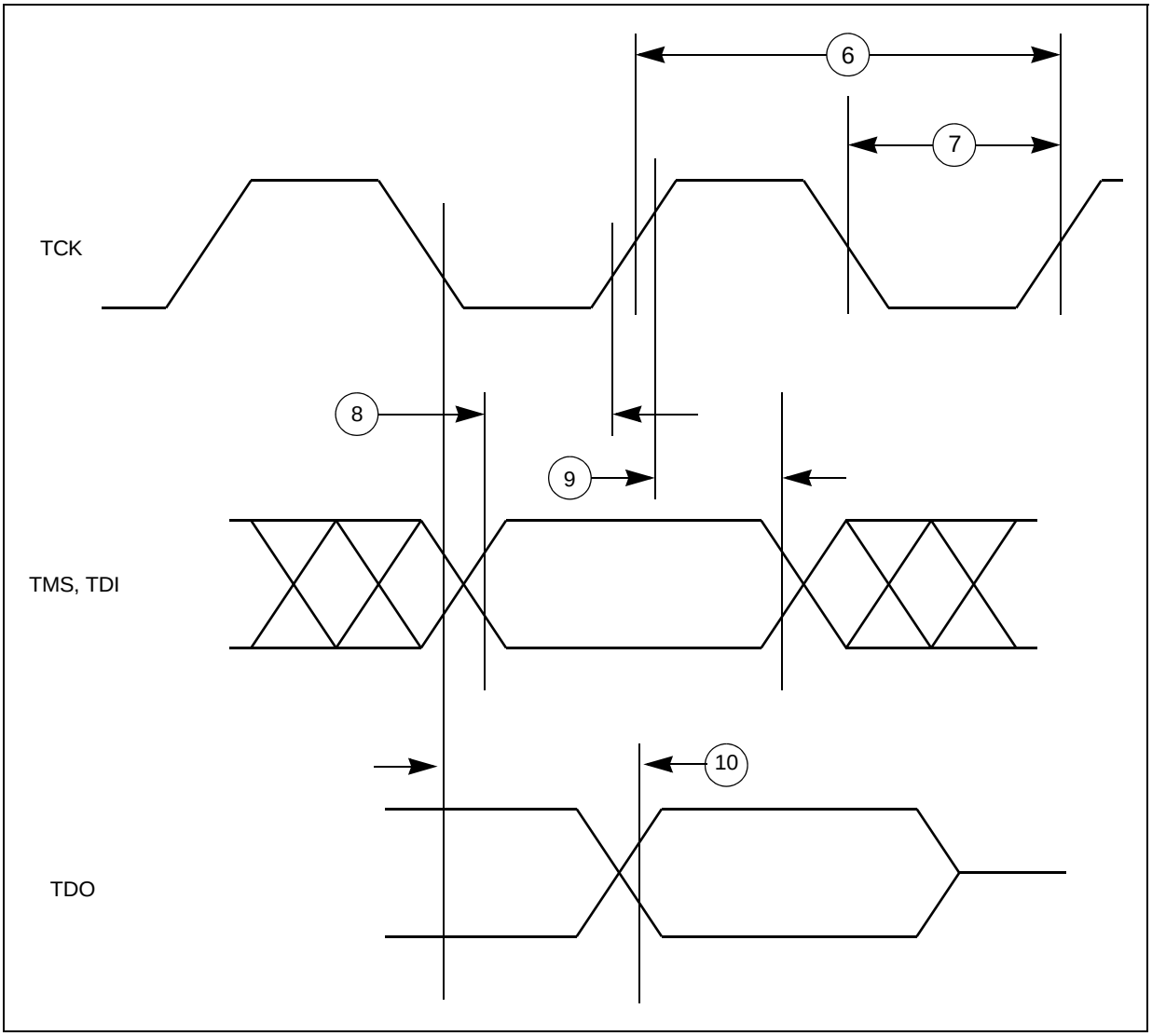
Note: Numbers shown reference *Table 50*.

Figure 28. DSPI classic SPI timing–slave, CPHA = 1



Note: Numbers shown reference *Table 50*.

Figure 35. Nexus TDI, TMS, TDO timing



3.19.4 JTAG characteristics

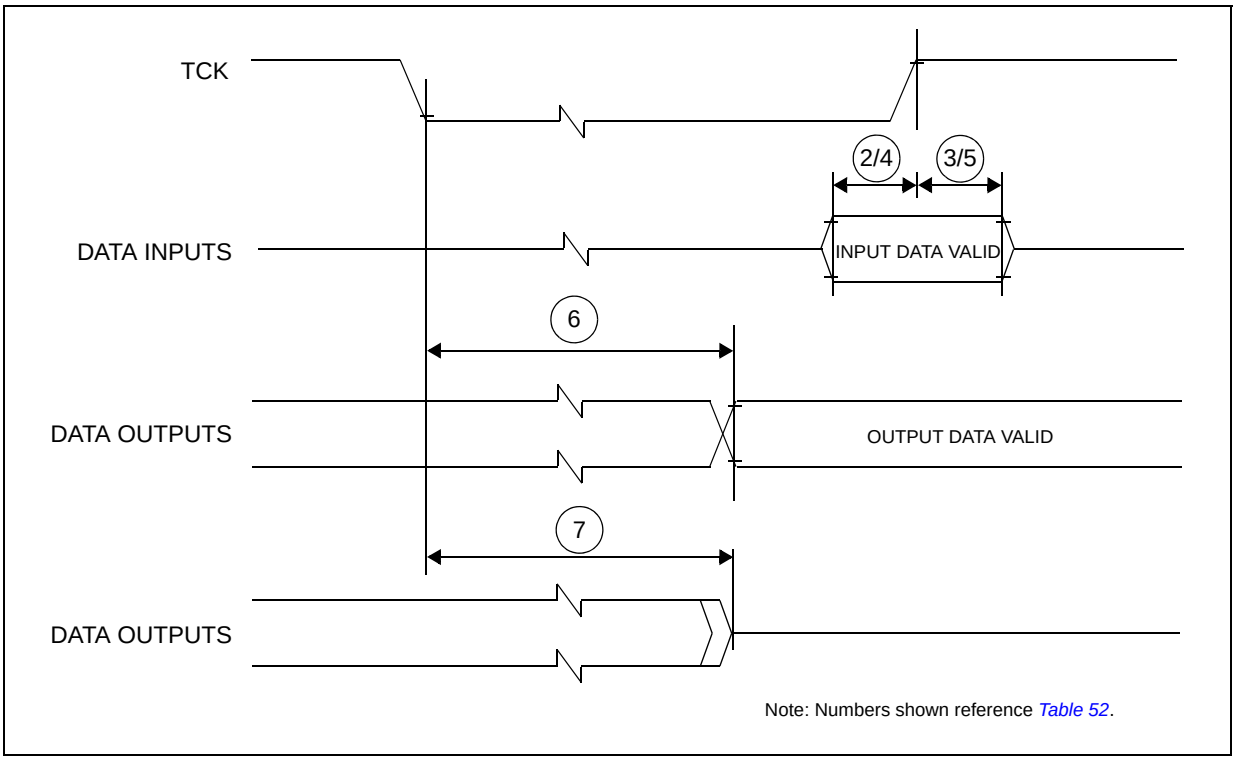
Table 52. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	10	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns
4	t_{TMSS}	CC	D	TMS setup time	10	—	—	ns
5	t_{TMSH}	CC	D	TMS hold time	5	—	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns

Table 52. JTAG characteristics (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns
—	t_{TDC}	CC	D	TCK Duty Cycle	40	—	60	%
—	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times	—	—	3	ns

Figure 36. Timing diagram - JTAG boundary scan



Note: Numbers shown reference *Table 52*.

4.2.3 LBGA256 package mechanical drawing

Figure 39. LBGA256 mechanical drawing