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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b74l7c8e0x

Table 2. SPC564Bxx and SPC56ECxx family comparison⁽¹⁾

Feature		SPC564B64		SPC56EC64			SPC564B70		SPC56EC70			SPC564B74		SPC56EC74		
Package		LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	LBGA 256
CPU		e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h		
Execution speed ⁽²⁾		Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h) ⁽³⁾			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h) ⁽³⁾			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h) ⁽³⁾		
Code flash memory		1.5 MB					2 MB					3 MB				
Data flash memory		4 x16 KB														
SRAM		128 KB		192 KB			160 KB		256 KB			192 KB		256 KB		
MPU		16-entry														
eDMA ⁽⁴⁾		32 ch														
10-bit ADC																
	dedicated ^{(5), (6)}	27 ch	33 ch	27 ch	33 ch		27 ch	33 ch	27 ch	33 ch		27 ch	33 ch	27 ch	33 ch	
	shared with 12-bit ADC ⁽⁷⁾	19 ch														
12-bit ADC																
	dedicated ⁽⁸⁾	5 ch	10 ch	5 ch	10 ch		5 ch	10 ch	5 ch	10 ch		5 ch	10 ch	5 ch	10 ch	
	shared with 10-bit ADC ⁽⁷⁾	19 ch														
CTU		64 ch														
Total timer I/O ⁽⁹⁾ eMIOS		64 ch, 16-bit														
SCI (LINFlexD)		10														
SPI (DSPI)		8														
CAN (FlexCAN) ⁽¹⁰⁾		6														

2.1 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow^(a)

M = Medium^{(a),(b)}

F = Fast^{(a),(b)}

I = Input only with analog feature^(a)

A = Analog

2.2 System pins

The system pins are listed in [Table 4](#).

Table 4. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET config.	Pin number		
					LQFP 176	LQFP 208	LBGA 256
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	29	29	K1
EXTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	A ⁽¹⁾	—	58	74	T8
XTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	A ⁽¹⁾	—	56	72	T7

- For analog pads, it is not recommended to enable IBE if APC is enabled to avoid extra current in middle range voltage.

a. See the I/O pad electrical characteristics in the device datasheet for details.

b. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium. For example, Fast/Medium pad will be Medium by default at reset. Similarly, Slow/Medium pad will be Slow by default. Only exception is PC[1] which is in medium configuration by default (refer to PCR.SRC in the reference manual, Pad Configuration Registers (PCR0—PCR198)).

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlexD_2 eMIOS_0 —	I/O O I/O —	S	Tristate	175	207	B3
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13]	SIUL — eMIOS_0 — LINFlexD_2 WKPU	I/O — I/O — I I	S	Tristate	2	2	C3
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M/S	Tristate	36	36	L1
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] CAN1RX CAN4RX WKPU[5]	SIUL — — ADC_0 FlexCAN_1 FlexCAN_4 WKPU	I/O — — O I I I	S	Tristate	35	35	K4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[44] E0UC[12] — — FR_DBG[0] SIN_2 EIRQ[19]	SIUL eMIOS_0 — — Flexray DSPI_2 SIUL	I/O I/O — — O I I	M/S	Tristate	173	205	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3 ALT4	GPIO[45] E0UC[13] SOUT_2 — FR_DBG[1]	SIUL eMIOS_0 DSPI_2 — Flexray	I/O I/O O — O	M/S	Tristate	174	206	A3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PC[14]	PCR[46]	AF0	GPIO[46]	SIUL	I/O	M/S	Tristate	3	3	B2
		AF1	E0UC[14]	eMIOS_0	I/O					
		AF2	SCK_2	DSPI_2	I/O					
		AF3	—	—	—					
		ALT4	FR_DBG[2]	Flexray	O					
		—	EIRQ[8]	SIUL	I					
PC[15]	PCR[47]	AF0	GPIO[47]	SIUL	I/O	M/S	Tristate	4	4	A1
		AF1	E0UC[15]	eMIOS_0	I/O					
		AF2	CS0_2	DSPI_2	I/O					
		AF3	—	—	—					
		ALT4	FR_DBG[3]	Flexray	O					
		—	EIRQ[20]	SIUL	I					
PD[0]	PCR[48]	AF0	GPI[48]	SIUL	I	I	Tristate	77	93	R12
		AF1	—	—	—					
		AF2	—	—	—					
		AF3	—	—	—					
		—	ADC0_P[4]	ADC_0	I					
		—	ADC1_P[4]	ADC_1	I					
PD[1]	PCR[49]	—	WKPU[27]	WKPU	I					
		AF0	GPI[49]	SIUL	I	I	Tristate	78	94	T13
		AF1	—	—	—					
		AF2	—	—	—					
		AF3	—	—	—					
		—	ADC0_P[5]	ADC_0	I					
PD[2]	PCR[50]	—	ADC1_P[5]	ADC_1	I					
		—	WKPU[28]	WKPU	I					
		AF0	GPI[50]	SIUL	I	I	Tristate	79	95	N11
		AF1	—	—	—					
		AF2	—	—	—					
		AF3	—	—	—					
		—	ADC0_P[6]	ADC_0	I					
		—	ADC1_P[6]	ADC_1	I					

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[63] CS2_1 E0UC[27] — FR_DBG[1] ADC0_S[7]	SIUL DSPI_1 eMIOS_0 — Flexray ADC_0	I/O O I/O — O I	S	Tristate	106	128	J13
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — CAN5RX WKPU[6]	SIUL eMIOS_0 — — FlexCAN_5 WKPU	I/O I/O — — I I	S	Tristate	18	18	G2
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] CAN5TX —	SIUL eMIOS_0 FlexCAN_5 —	I/O I/O O —	M/S	Tristate	20	20	F4
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 ALT4 — —	GPIO[66] E0UC[18] — — FR_A_TX_EN SIN_1 EIRQ[21]	SIUL eMIOS_0 — — Flexray DSPI_1 SIUL	I/O I/O — — O I I	M/S	Tristate	156	180	A7
PE[3]	PCR[67]	AF0 AF1 AF2 AF3 — —	GPIO[67] E0UC[19] SOUT_1 — FR_A_RX WKPU[29]	SIUL eMIOS_0 DSPI_1 — Flexray WKPU	I/O I/O O — I I	M/S	Tristate	157	181	A10
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 ALT4 —	GPIO[68] E0UC[20] SCK_1 — FR_B_TX EIRQ[9]	SIUL eMIOS_0 DSPI_1 — Flexray SIUL	I/O I/O I/O — O I	M/S	Tristate	160	184	A8

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PH[1]	PCR[113]	AF0 AF1 AF2 AF3 ALT4	GPIO[113] E1UC[3] SOUT_1 — TXD[0]	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O O — O	M/S	Tristate	118	142	F13
PH[2]	PCR[114]	AF0 AF1 AF2 AF3 ALT4	GPIO[114] E1UC[4] SCK_1 — TX_EN	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O I/O — O	M/S	Tristate	119	143	D16
PH[3]	PCR[115]	AF0 AF1 AF2 AF3 ALT4	GPIO[115] E1UC[5] CS0_1 — TX_ER	SIUL eMIOS_1 DSPI_1 — FEC	I/O I/O I/O — O	M/S	Tristate	120	144	F14
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] SOUT_7 —	SIUL eMIOS_1 DSPI_7 —	I/O I/O O —	M/S	Tristate	162	186	D7
PH[5]	PCR[117]	AF0 AF1 AF2 AF3 —	GPIO[117] E1UC[7] — — SIN_7	SIUL eMIOS_1 — — DSPI_7	I/O I/O — — I	S	Tristate	163	187	B7
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] SCK_7 MA[2]	SIUL eMIOS_1 DSPI_7 ADC_0	I/O I/O I/O O	M/S	Tristate	164	188	C7
PH[7]	PCR[119]	AF0 AF1 AF2 AF3 ALT4	GPIO[119] E1UC[9] CS3_2 MA[1] CS0_7	SIUL eMIOS_1 DSPI_2 ADC_0 DSPI_7	I/O I/O O O I/O	M/S	Tristate	165	189	C6

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX —	SIUL eMIOS_0 LINFlexD_8 —	I/O I/O O —	S	Tristate	172	196	C5
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKPU[24] LIN8RX	SIUL eMIOS_0 — — WKPU LINFlexD_8	I/O I/O — — I I	S	Tristate	171	195	A4
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX —	SIUL eMIOS_0 LINFlexD_9 —	I/O I/O O —	S	Tristate	170	194	D6
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKPU[23] LIN9RX	SIUL eMIOS_0 — — WKPU LINFlexD_9	I/O I/O — — I I	S	Tristate	169	193	B5
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	M/S	Tristate	143	167	A12
PI[5]	PCR[133]	AF0 AF1 AF2 AF3 ALT4	GPIO[133] E1UC[29] SCK_4 CS2_5 CS2_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O O O	M/S	Tristate	142	166	D12
PI[6]	PCR[134]	AF0 AF1 AF2 AF3 ALT4	GPIO[134] E1UC[30] CS0_4 CS0_5 CS0_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O I/O I/O I/O	S	Tristate	11	11	D2

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PI[7]	PCR[135]	AF0 AF1 AF2 AF3 ALT4	GPIO[135] E1UC[31] CS1_4 CS1_5 CS1_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O O O O	S	Tristate	12	12	E2
PI[8]	PCR[136]	AF0 AF1 AF2 AF3 —	GPIO[136] — — — ADC0_S[16]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	108	130	J14
PI[9]	PCR[137]	AF0 AF1 AF2 AF3 —	GPIO[137] — — — ADC0_S[17]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	131	J15
PI[10]	PCR[138]	AF0 AF1 AF2 AF3 —	GPIO[138] — — — ADC0_S[18]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	134	J16
PI[11]	PCR[139]	AF0 AF1 AF2 AF3 — —	GPIO[139] — — — ADC0_S[19] SIN_3	SIUL — — — ADC_0 DSPI_3	I/O — — — I I	S	Tristate	111	135	H16
PI[12]	PCR[140]	AF0 AF1 AF2 AF3 —	GPIO[140] CS0_3 CS0_2 — ADC0_S[20]	SIUL DSPI_3 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	112	136	G15

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PL[6]	PCR[182]	AF0 AF1 AF2 AF3	GPIO[182] — MDO4 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	K5
PL[7]	PCR[183]	AF0 AF1 AF2 AF3	GPIO[183] — MDO5 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	L5
PL[8]	PCR[184]	AF0 AF1 AF2 AF3 —	GPIO[184] — — — EVTI	SIUL — — — Nexus	I/O — — — I	S	Pull-up	—	—	M9
PL[9]	PCR[185]	AF0 AF1 AF2 AF3	GPIO[185] — MSEO —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	M10
PL[10]	PCR[186]	AF0 AF1 AF2 AF3	GPIO[186] — MCKO —	SIUL — Nexus —	I/O — O —	F/S	Tristate	—	—	M11
PL[11]	PCR[187]	AF0 AF1 AF2 AF3	GPIO[187] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	M12
PL[12]	PCR[188]	AF0 AF1 AF2 AF3	GPIO[188] — EVTO —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F11
PL[13]	PCR[189]	AF0 AF1 AF2 AF3	GPIO[189] — MDO6 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F10

3 Electrical Characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS_HV}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol "SR" for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in [Table 6](#) are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled "C" in the parameter tables where appropriate.

3.2 NVUSRO register

Portions of the device configuration, such as high voltage supply is controlled via bit values in the Non-Volatile User Options Register (NVUSRO). For a detailed description of the NVUSRO register, see SPC564Bxx and SPC56ECxx Reference Manual.

Table 9. Absolute maximum ratings (continued)

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
$V_{RC_CTRL}^{(2)}$	Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	$V_{DD_LV} + 1$	V
V_{SS_ADC}	S R Voltage on $V_{SS_HV_ADC0}$, $V_{SS_HV_ADC1}$ (ADC reference) pin with respect to ground (V_{SS_HV})	—	$V_{SS_HV} - 0.1$	$V_{SS_HV} + 0.1$	V
$V_{DD_HV_ADC0}$	S R Voltage on $V_{DD_HV_ADC0}$ with respect to ground (V_{SS_HV})	—	-0.3	6.0	V
		Relative to $V_{DD_HV_A}^{(3)}$	$V_{DD_HV_A} - 0.3$	$V_{DD_HV_A} + 0.3$	
$V_{DD_HV_ADC1}^{(4)}$	S R Voltage on $V_{DD_HV_ADC1}$ with respect to ground (V_{SS_HV})	—	-0.3	6.0	V
		Relative to $V_{DD_HV_A}^{(2)}$	$V_{DD_HV_A} - 0.3$	$V_{DD_HV_A} + 0.3$	
V_{IN}	S R Voltage on any GPIO pin with respect to ground (V_{SS_HV})	Relative to $V_{DD_HV_A/HV_B}$	$V_{DD_HV_A/HV_B} - 0.3$	$V_{DD_HV_A/HV_B} + 0.3$	V
I_{INJPAD}	S R Injected input current on any pin during overload condition	—	-10	10	mA
I_{INJSUM}	S R Absolute sum of all injected input currents during overload condition	—	-50	50	
$I_{AVGSEG}^{(5)}$	S R Sum of all the static I/O current within a supply segment ($V_{DD_HV_A}$ or $V_{DD_HV_B}$)	$V_{DD} = 5.0\text{ V} \pm 10\%$, $PAD3V5V = 0$		70	mA
		$V_{DD} = 3.3\text{ V} \pm 10\%$, $PAD3V5V = 1$		64	
$T_{STORAGE}$	S R Storage temperature	—	-55 ⁽⁶⁾	150	°C

- $V_{DD_HV_B}$ can be independently controlled from $V_{DD_HV_A}$. These can ramp up or ramp down in any order. Design is robust against any supply order.
- This voltage is internally generated by the device and no external voltage should be supplied.
- Both the relative and the fixed conditions must be met. For instance: If $V_{DD_HV_A}$ is 5.9 V, $V_{DD_HV_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD_HV_A} + 0.3 = 6.2\text{ V}$.
- PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD_HV_B}$ domain hence $V_{DD_HV_ADC1}$ should be within $\pm 300\text{ mV}$ of $V_{DD_HV_B}$ when these channels are used for ADC_1.
- Any temperature beyond 125 °C should limit the current to 50 mA (max).
- This is the storage temperature for the flash memory.

Note: Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD_HV_A/HV_B}$ or $V_{IN} < V_{SS_HV}$), the voltage on pins with respect to ground (V_{SS_HV}) must not exceed the recommended values.

Table 10. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
T_A	SR	Ambient temperature under bias	f_{CPU} up to 120 MHz + 2%	-40	125	°C
T_J	SR	Junction temperature under bias	—	-40	150	

- 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
- 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 μ F bulk capacitance needs to be provided as CREG on each VDD_LV pin. For details refer to the Power Management chapter of the MPC5646C Reference Manual.
- This voltage is internally generated by the device and no external voltage should be supplied.
- 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
- Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
- Both the relative and the fixed conditions must be met. For instance: If V_{DD_HV_A} is 5.9 V, V_{DD_HV_ADC0} maximum value is 6.0 V then, despite the relative condition, the max value is V_{DD_HV_A} + 0.3 = 6.2 V.
- PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from V_{DD_HV_B} domain hence V_{DD_HV_ADC1} should be within ± 100 mV of V_{DD_HV_B} when these channels are used for ADC_1.
- Guaranteed by the device validation.

Table 11. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V _{SS_HV}	S R	Digital ground on VSS_HV pins	—	0	0	V
V _{DD_HV_A} ⁽¹⁾	S R	Voltage on VDD_HV_A pins with respect to ground (V _{SS_HV})	—	4.5	5.5	V
			Voltage drop ⁽²⁾	3.0	5.5	
V _{DD_HV_B}	S R	Generic GPIO functionality	—	3.0	5.5	V
		Ethernet/3.3 V functionality (See the notes in all figures in Section 2: Package pinouts and signal descriptions for the list of channels operating in V _{DD_HV_B} domain)	—	3.0	3.6	V
V _{SS_LV} ⁽³⁾	S R	Voltage on VSS_LV (Low voltage digital supply) pins with respect to ground (V _{SS_HV})	—	V _{SS_HV} - 0.1	V _{SS_HV} + 0.1	V
V _{RC_CTRL} ⁽⁴⁾		Base control voltage for external BCP68 NPN device	Relative to V _{DD_LV}	0	V _{DD_LV} + 1	V
V _{SS_ADC}	S R	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V _{SS_HV})	—	V _{SS_HV} - 0.1	V _{SS_HV} + 0.1	V

4. The width of input pulse in between 40 ns to 1000 ns is indeterminate. It may pass the noise or may not depending on silicon sample to sample variation.

3.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- [Table 15](#) provides weak pull figures. Both pull-up and pull-down resistances are supported.
- [Table 16](#) provides output driver characteristics for I/O pads when in SLOW configuration.
- [Table 17](#) provides output driver characteristics for I/O pads when in MEDIUM configuration.
- [Table 18](#) provides output driver characteristics for I/O pads when in FAST configuration.

Table 15. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions ^{(1),(2)}		Value			Unit
						Min	Typ	Max	
I _{WPUL}	CC	P	Weak pull-up current absolute value	V _{IN} = V _{IL} , V _{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	μA
		PAD3V5V = 1 ⁽³⁾			10	—	250		
		P		V _{IN} = V _{IL} , V _{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
I _{WPD}	CC	P	Weak pull-down current absolute value	V _{IN} = V _{IH} , V _{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	μA
		PAD3V5V = 1			10	—	250		
		P		V _{IN} = V _{IH} , V _{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = -40 to 125 °C, unless otherwise specified.

2. V_{DD} as mentioned in the table is V_{DD_HV_A}/V_{DD_HV_B}.

3. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 16. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions ^{(1),(2)}		Value			Unit
						Min	Typ	Max	
V _{OH}	CC	P	Output high level SLOW configuration	Push Pull	I _{OH} = -3 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V _{DD}	—	—	V
		C			I _{OH} = -3 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ⁽³⁾	0.8V _{DD}	—	—	
		P			I _{OH} = -1.5 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	V _{DD} - 0.8	—	—	

Figure 11. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

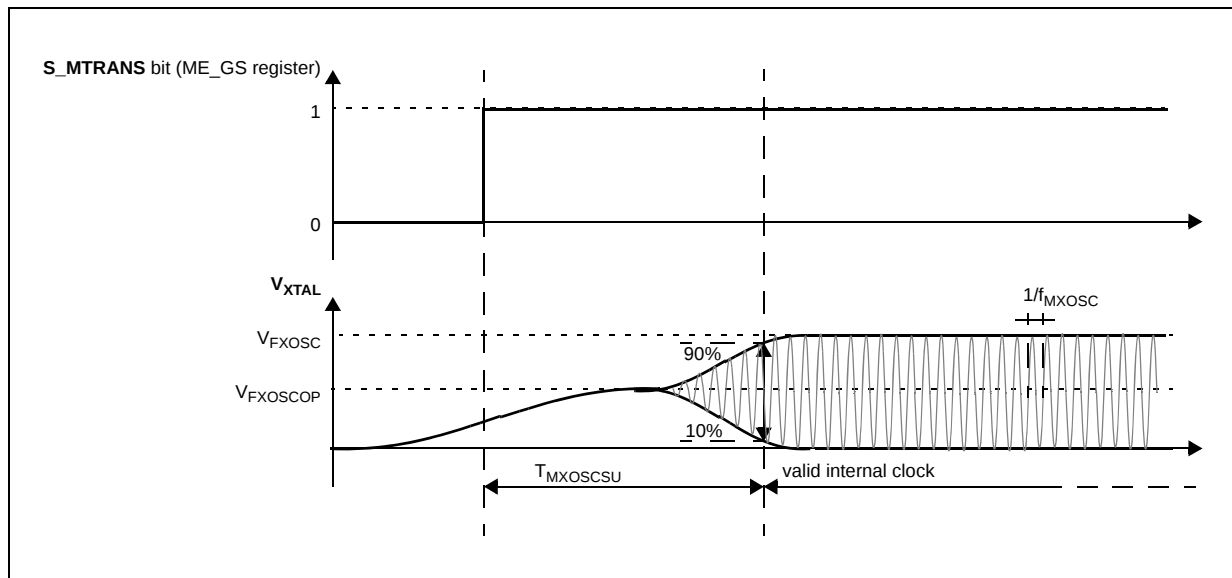


Table 36. Fast external crystal oscillator (4 to 40 MHz) electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value ⁽²⁾			Unit
				Min	Typ	Max	
f_{FXOSC}	SR	Fast external crystal oscillator frequency	—	4.0	—	40.0	MHz
g_{mFXOSC}	CC	Fast external crystal oscillator transconductance	$V_{DD} = 3.3 \text{ V} \pm 10\%$	4 ⁽³⁾	—	20 ⁽³⁾	mA/V
			$V_{DD} = 5.0 \text{ V} \pm 10\%$	6.5 ⁽³⁾	—	25 ⁽³⁾	
V_{FXOSC}	CC	Oscillation amplitude at EXTAL	$f_{OSC} = 40 \text{ MHz}$ For both $V_{DD} = 3.3 \text{ V} \pm 10\%$, $V_{DD} = 5.0 \text{ V} \pm 10\%$	—	0.95	—	V
$V_{FXOSCOPE}$	CC	Oscillation operating point	—	—	1.8	—	V
$I_{FXOSC}^{(4)}$	CC	Fast external crystal oscillator consumption	$V_{DD} = 3.3 \text{ V} \pm 10\%$, $f_{OSC} = 40 \text{ MHz}$	—	2	2.2	mA
			$V_{DD} = 5.0 \text{ V} \pm 10\%$, $f_{OSC} = 40 \text{ MHz}$	—	2.3	2.5	
			$V_{DD} = 3.3 \text{ V} \pm 10\%$, $f_{OSC} = 16 \text{ MHz}$	—	1.3	1.5	
			$V_{DD} = 5.0 \text{ V} \pm 10\%$, $f_{OSC} = 16 \text{ MHz}$	—	1.6	1.8	
$T_{FXOSCSU}$	CC	Fast external crystal oscillator start-up time	$f_{OSC} = 40 \text{ MHz}$ For both $V_{DD} = 3.3 \text{ V} \pm 10\%$, $V_{DD} = 5.0 \text{ V} \pm 10\%$	—	—	5	ms

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{P2} substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1MHz, with $C_S + C_{P2}$ equal to 3pF, a resistance of 330K Ω is obtained ($R_{eqv} = 1 / (f_c * (C_S + C_{P2}))$), where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $C_S + C_{P2}$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the following relation

Equation 4

$$V_A \cdot \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} \text{LSB}$$

The formula above provides a constraint for external network design, in particular on resistive path.

Figure 16. Input equivalent circuit (precise channels)

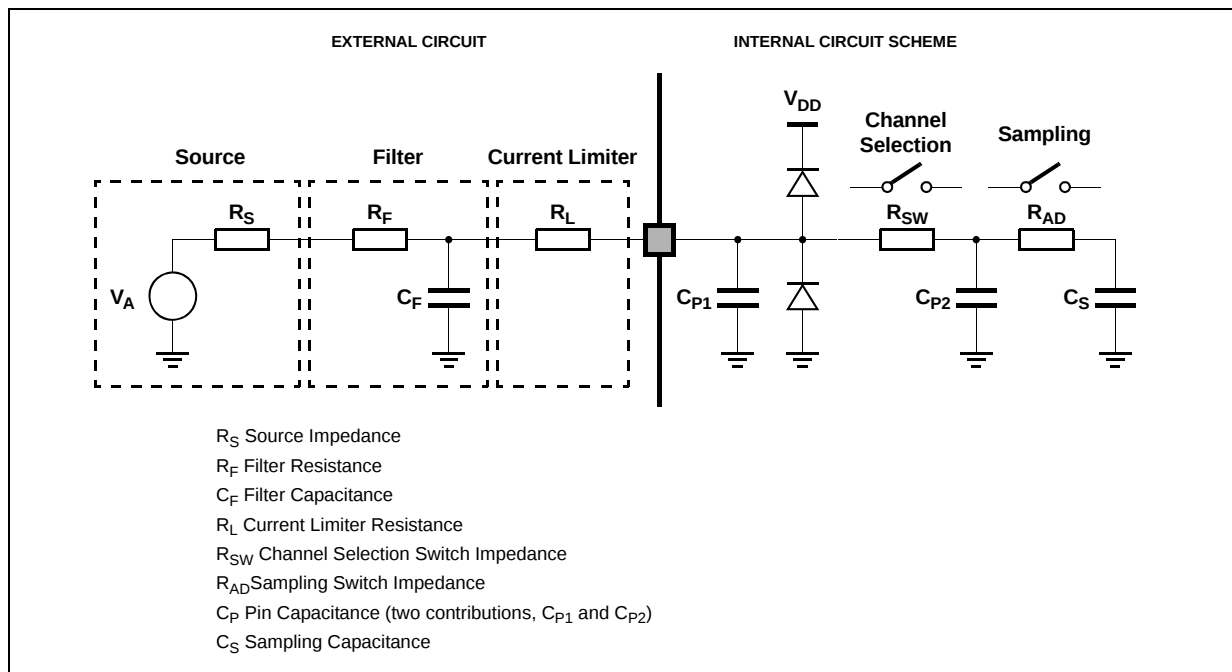
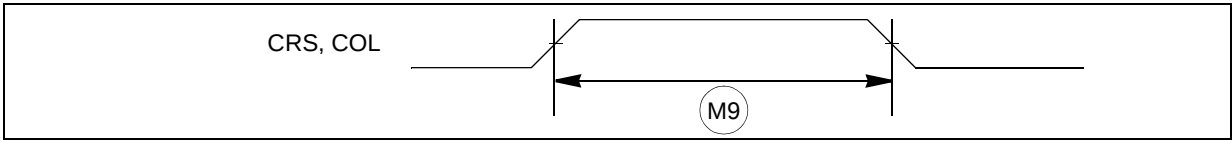


Figure 23. MII async inputs timing diagram



3.18.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 48. MII serial management channel timing⁽¹⁾

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	28	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1. Output pads configured with SRE = 0b11.

Figure 24. MII serial management channel timing diagram

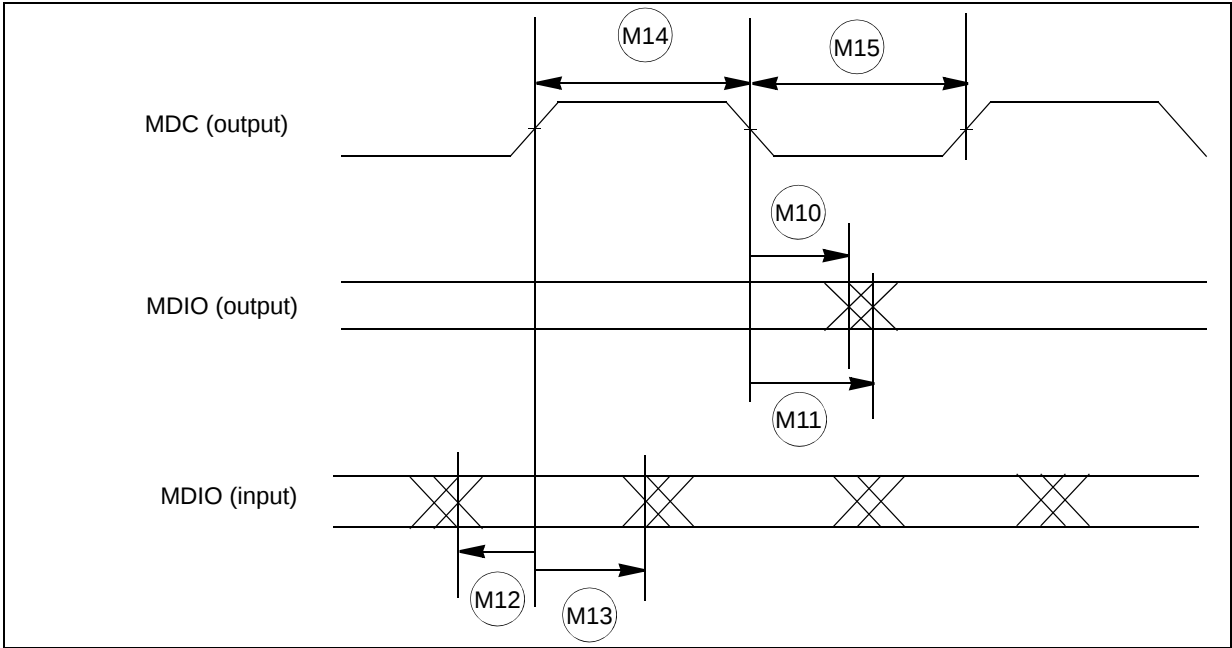


Figure 29. DSPI modified transfer format timing-master, CPHA = 0

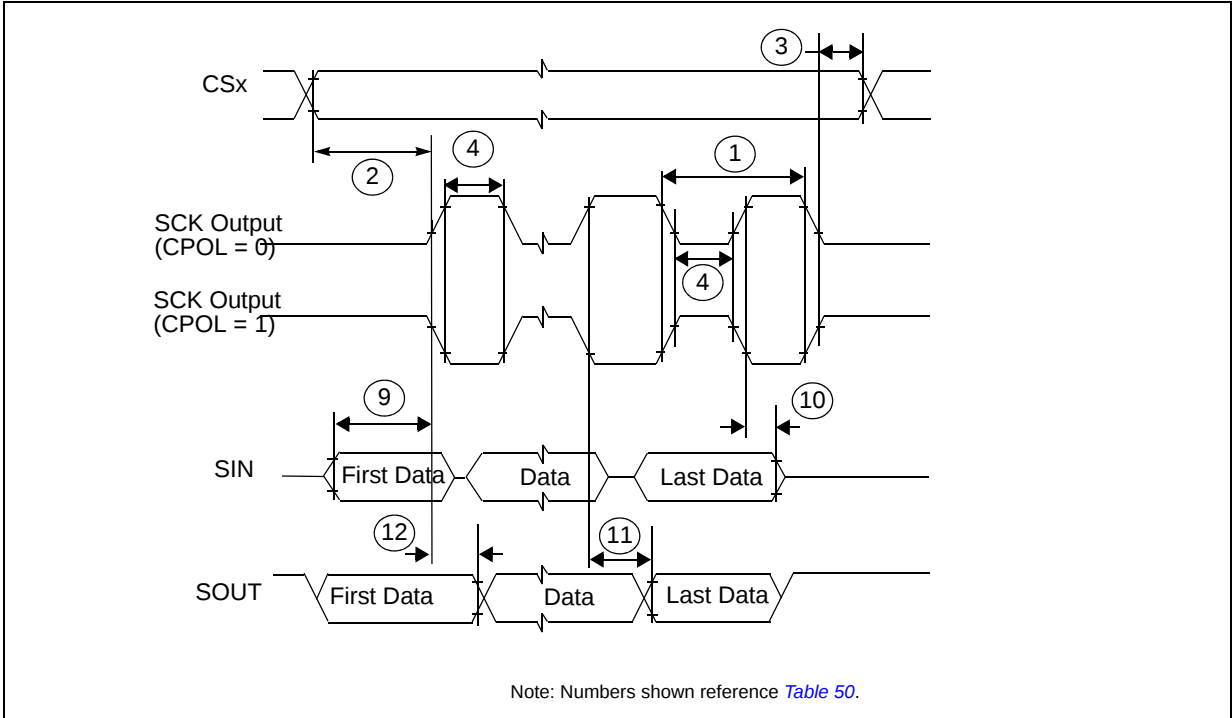


Figure 30. DSPI modified transfer format timing-master, CPHA = 1

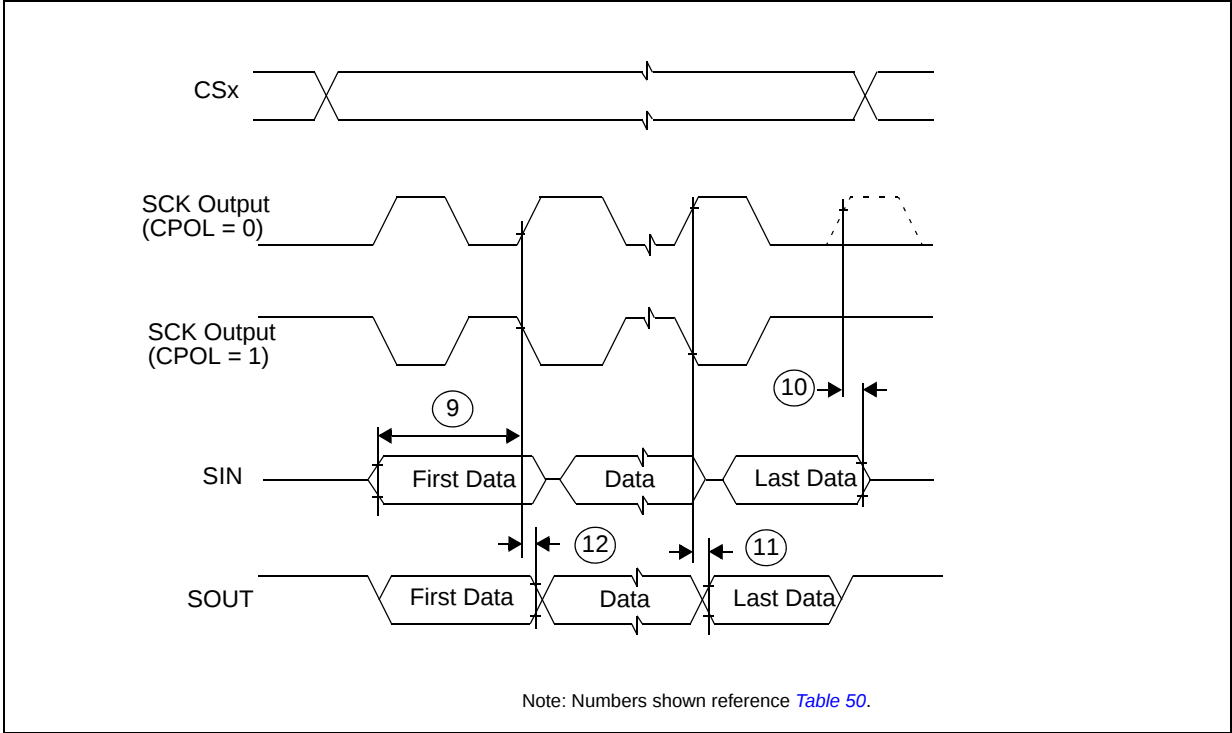


Table 52. JTAG characteristics (continued)

No.	Symbol	C	D	Parameter	Value			Unit
					Min	Typ	Max	
7	t_{TDOl}	CC	D	TCK low to TDO invalid	6	—	—	ns
—	t_{TDC}	CC	D	TCK Duty Cycle	40	—	60	%
—	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times	—	—	3	ns

Figure 36. Timing diagram - JTAG boundary scan

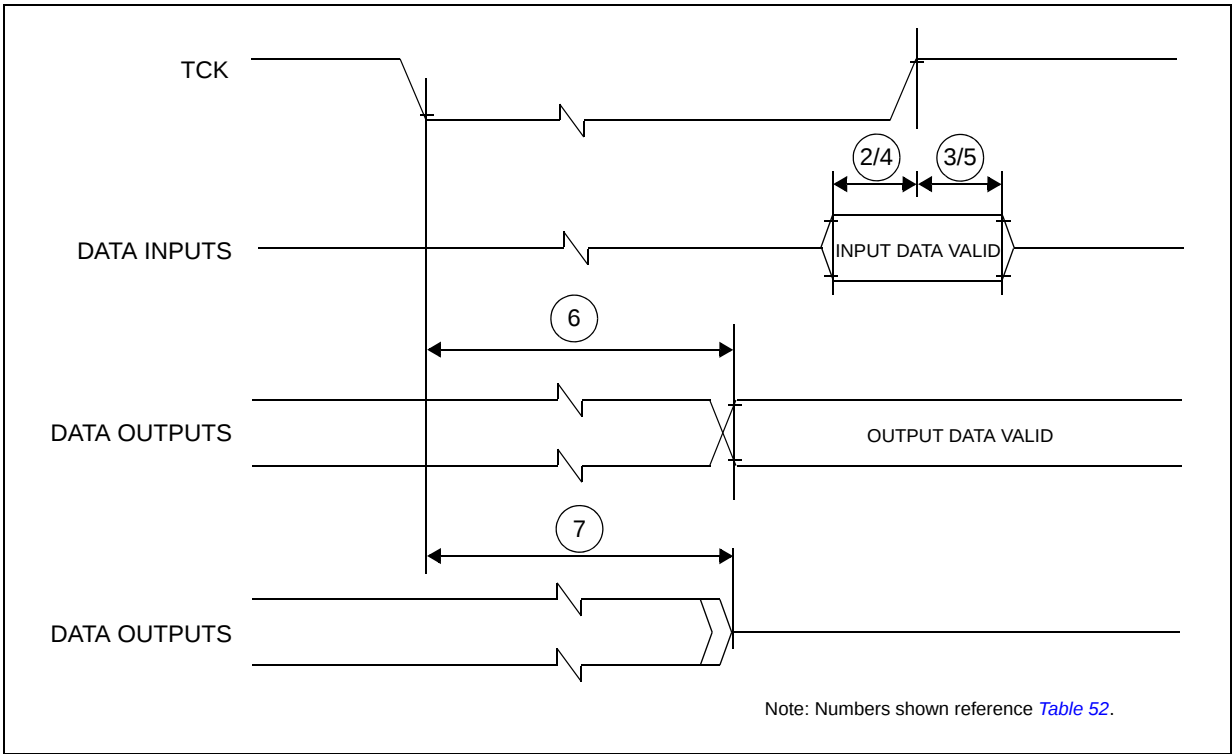


Table 55. LBGA256 mechanical data

Ref	mm		
	Min	Typ	Max
A	1.210		1.700
A1	0.300		
A2		0.300	
A4			0.800
b	0.400	0.500	0.600
D	16.800	17.000	17.200
D1		15.000	
E	16.800	17.000	17.200
E1		15.000	
e	0.900	1.000	1.100
Z	0.750	1.000	1.250
ddd			0.200

Note: The package is designed according to the JEDEC standard No 95-1 Section 14 dedicated to Ball Grid Array Package Design Guide.

Appendix A Abbreviations

[Table 56](#) lists abbreviations used but not defined elsewhere in this document.

Table 56. Abbreviations

Abbreviation	Meaning
CS	Chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select