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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	147
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564b74l7c9ecy

2.3 Functional ports

The functional port pins are listed in *Table 5*.

Table 5. Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 — —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKPU[19] CAN1RX	SIUL eMIOS_0 MC_CGM eMIOS_0 WKPU FlexCAN_1	I/O I/O O I/O I I	M/S	Tristate	24	24	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — — —	GPIO[1] E0UC[1] — — WKPU[2] CAN3RX NMI[0][3]	SIUL eMIOS_0 — — WKPU FlexCAN_3 WKPU	I/O I/O — — I I I	S	Tristate	19	19	F3
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 — —	GPIO[2] E0UC[2] — MA[2] WKPU[3] NMI[1][3]	SIUL eMIOS_0 — ADC_0 WKPU WKPU	I/O I/O — O I I	S	Tristate	17	17	F1
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — — —	GPIO[3] E0UC[3] LIN5TX CS4_1 RX_ER_CLK EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlexD_5 DSPI_1 FEC SIUL ADC_1	I/O I/O O O I I I	M/S	Tristate	114	138	G16
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 — —	GPIO[4] E0UC[4] — CS0_1 LIN5RX WKPU[9]	SIUL eMIOS_0 — DSPI_1 LINFlexD_5 WKPU	I/O I/O — I/O I I	S	Tristate	51	61	T2

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX CS4_0 CAN2TX	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M/S	Tristate	42	50	N2
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — — —	GPIO[89] E1UC[1] CS5_0 — CAN2RX CAN3RX WKPU[22]	SIUL eMIOS_1 DSPI_0 — FlexCAN_2 FlexCAN_3 WKPU	I/O I/O O — I I I	S	Tristate	41	49	M4
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] CS1_0 LIN4TX E1UC[2]	SIUL DSPI_0 LINFlexD_4 eMIOS_1	I/O O O I/O	M/S	Tristate	46	54	P2
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 — —	GPIO[91] CS2_0 E1UC[3] — LIN4RX WKPU[15]	SIUL DSPI_0 eMIOS_1 — LINFlexD_4 WKPU	I/O O I/O — I I	S	Tristate	47	55	R1
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] LIN5TX —	SIUL eMIOS_1 LINFlexD_5 —	I/O I/O O —	M/S	Tristate	43	51	P1
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] — — LIN5RX WKPU[16]	SIUL eMIOS_1 — — LINFlexD_5 WKPU	I/O I/O — — I I	S	Tristate	49	57	P3

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PI[7]	PCR[135]	AF0 AF1 AF2 AF3 ALT4	GPIO[135] E1UC[31] CS1_4 CS1_5 CS1_6	SIUL eMIOS_1 DSPI_4 DSPI_5 DSPI_6	I/O I/O O O O	S	Tristate	12	12	E2
PI[8]	PCR[136]	AF0 AF1 AF2 AF3 —	GPIO[136] — — — ADC0_S[16]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	108	130	J14
PI[9]	PCR[137]	AF0 AF1 AF2 AF3 —	GPIO[137] — — — ADC0_S[17]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	131	J15
PI[10]	PCR[138]	AF0 AF1 AF2 AF3 —	GPIO[138] — — — ADC0_S[18]	SIUL — — — ADC_0	I/O — — — I	S	Tristate	—	134	J16
PI[11]	PCR[139]	AF0 AF1 AF2 AF3 — —	GPIO[139] — — — ADC0_S[19] SIN_3	SIUL — — — ADC_0 DSPI_3	I/O — — — I I	S	Tristate	111	135	H16
PI[12]	PCR[140]	AF0 AF1 AF2 AF3 —	GPIO[140] CS0_3 CS0_2 — ADC0_S[20]	SIUL DSPI_3 DSPI_2 — ADC_0	I/O I/O I/O — I	S	Tristate	112	136	G15

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PJ[10]	PCR[154]	AF0 AF1 AF2 AF3 —	GPIO[154] — — — ADC1_S[9]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	67	T5
PJ[11]	PCR[155]	AF0 AF1 AF2 AF3 —	GPIO[155] — — — ADC1_S[10]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	60	R3
PJ[12]	PCR[156]	AF0 AF1 AF2 AF3 —	GPIO[156] — — — ADC1_S[11]	SIUL — — — ADC_1	I/O — — — I	S	Tristate	—	59	T1
PJ[13]	PCR[157]	AF0 AF1 AF2 AF3 — — — —	GPIO[157] — CS1_7 — CAN4RX ADC1_S[12] CAN1RX WKPU[31]	SIUL — DSPI_7 — FlexCAN_4 ADC_1 FlexCAN_1 WKPU	I/O — O — I I I I	S	Tristate	—	65	N5
PJ[14]	PCR[158]	AF0 AF1 AF2 AF3	GPIO[158] CAN1TX CAN4TX CS2_7	SIUL FlexCAN_1 FlexCAN_4 DSPI_7	I/O O O O	M/S	Tristate	—	64	T4
PJ[15]	PCR[159]	AF0 AF1 AF2 AF3 —	GPIO[159] — CS1_6 — CAN1RX	SIUL — DSPI_6 — FlexCAN_1	I/O — O — I	M/S	Tristate	—	63	R4

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin number		
								LQFP 176	LQFP 208	LBGA256
PK[14]	PCR[174]	AF0 AF1 AF2 AF3	GPIO[174] CAN3TX CS3_7 CS0_1	SIUL FlexCAN_3 DSPI_7 DSPI_1	I/O O O I/O	M/S	Tristate	—	202	J12
PK[15]	PCR[175]	AF0 AF1 AF2 AF3 — —	GPIO[175] — — — SIN_1 SIN_7	SIUL — — — DSPI_1 DSPI_7	I/O — — — I I	M/S	Tristate	—	203	D5
PL[0]	PCR[176]	AF0 AF1 AF2 AF3	GPIO[176] SOUT_1 SOUT_7 —	SIUL DSPI_1 DSPI_7 —	I/O O O —	M/S	Tristate	—	204	C4
PL[1]	PCR[177]	AF0 AF1 AF2 AF3	GPIO[177] — — —	SIUL — — —	I/O — — —	M/S	Tristate	—	—	F7
PL[2]	PCR[178][7]	AF0 AF1 AF2 AF3	GPIO[178] — MDO0[8] —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	F5
PL[3]	PCR[179]	AF0 AF1 AF2 AF3	GPIO[179] — MDO1 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	G5
PL[4]	PCR[180]	AF0 AF1 AF2 AF3	GPIO[180] — MDO2 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	H5
PL[5]	PCR[181]	AF0 AF1 AF2 AF3	GPIO[181] — MDO3 —	SIUL — Nexus —	I/O — O —	M/S	Tristate	—	—	J5

3.2.1 NVUSRO [PAD3V5V(0)] field description

Table 7 shows how NVUSRO [PAD3V5V(0)] controls the device configuration for $V_{DD\_HV\_A}$ domain.

Table 7. PAD3V5V(0) field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

3.2.2 NVUSRO [PAD3V5V(1)] field description

Table 8 shows how NVUSRO [PAD3V5V(1)] controls the device configuration the device configuration for $V_{DD\_HV\_B}$ domain.

Table 8. PAD3V5V(1) field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. '1' is delivery value. It is part of shadow flash memory, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V(0,1) bit value.

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$	SR	Voltage on VDD_HV_A pins with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
$V_{DD\_HV\_B}$[1]	SR	Voltage on VDD_HV_B pins with respect to common ground (V_{SS_HV})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	$V_{SS\_HV} - 0.1$	$V_{SS\_HV} + 0.1$	V

Table 9. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{RC_CTRL} (2)		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	S R	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
$V_{DD\_HV\_ADC0}$	S R	Voltage on VDD_HV_ADC0 with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_A}$ (3)	$V_{DD\_HV\_A}$ – 0.3	$V_{DD\_HV\_A}$+0.3	
$V_{DD\_HV\_ADC1}$ (4)	S R	Voltage on VDD_HV_ADC1 with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_A}$ 2	$V_{DD\_HV\_A}$–0.3	$V_{DD\_HV\_A}$+0.3	
V_{IN}	S R	Voltage on any GPIO pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A/HV\_B}$	$V_{DD\_HV\_A/HV\_B}$– 0.3	$V_{DD\_HV\_A/HV\_B}$+ 0.3	V
I_{INJPAD}	S R	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	S R	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG} (5)	S R	Sum of all the static I/O current within a supply segment ($V_{DD\_HV\_A}$ or $V_{DD\_HV\_B}$)	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		64	
$T_{STORAGE}$	S R	Storage temperature	—	–55 (6)	150	°C

1. $V_{DD\_HV\_B}$ can be independently controlled from $V_{DD\_HV\_A}$. These can ramp up or ramp down in any order. Design is robust against any supply order.
2. This voltage is internally generated by the device and no external voltage should be supplied.
3. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.
4. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±300 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.
5. Any temperature beyond 125 °C should limit the current to 50 mA (max).
6. This is the storage temperature for the flash memory.

Note: Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN} > $V_{DD\_HV\_A/HV\_B}$ or V_{IN} < V_{SS_HV}), the voltage on pins with respect to ground (V_{SS_HV}) must not exceed the recommended values.

Table 10. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
T_A	SR	Ambient temperature under bias	f_{CPU} up to 120 MHz + 2%	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	

1. 100 nF EMI capacitance need to be provided between each VDD/VSS_HV pair.
2. 100 nF EMI capacitance needs to be provided between each VDD_LV/VSS_LV supply pair. 10 µF bulk capacitance needs to be provided as CREG on each VDD_LV pin. For details refer to the Power Management chapter of the MPC5646C Reference Manual.
3. This voltage is internally generated by the device and no external voltage should be supplied.
4. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
6. Both the relative and the fixed conditions must be met. For instance: If $V_{DD\_HV\_A}$ is 5.9 V, $V_{DD\_HV\_ADC0}$ maximum value is 6.0 V then, despite the relative condition, the max value is $V_{DD\_HV\_A}$ + 0.3 = 6.2 V.
7. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1.
8. Guaranteed by the device validation.

Table 11. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_HV}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD\_HV\_A}$(1)	SR	Voltage on VDD_HV_A pins with respect to ground (V_{SS_HV})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
$V_{DD\_HV\_B}$	SR	Generic GPIO functionality	—	3.0	5.5	V
		Ethernet/3.3 V functionality (See the notes in all figures in *Section 2: Package pinouts and signal descriptions* for the list of channels operating in $V_{DD\_HV\_B}$ domain)	—	3.0	3.6	V
V_{SS_LV}(3)	SR	Voltage on VSS_LV (Low voltage digital supply) pins with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V
V_{RC_CTRL}(4)		Base control voltage for external BCP68 NPN device	Relative to V_{DD_LV}	0	V_{DD_LV} + 1	V
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS_HV})	—	V_{SS_HV} – 0.1	V_{SS_HV} + 0.1	V

8. Guaranteed by device validation.

Note: SRAM retention guaranteed to LVD levels.

3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 12. LQFP thermal characteristics(1)

Symbol		C	Parameter	Conditions(2)	Pin count	Value(3)			Unit
						Min	Typ	Max	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	176	—	—	44.4(4)	°C/W
					208	—	—	43	°C/W
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection	Four-layer board—2s2p(5)	176	—	—	36.1	°C/W
					208	—	—	33.9	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C.
3. All values need to be confirmed during device validation.
4. 1s board as per standard JEDEC (JESD51-7) in natural convection.
5. 2s2p board as per standard JEDEC (JESD51-7) in natural convection.

Table 13. LBGA256 thermal characteristics(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	—	Thermal resistance, junction-to-ambient natural convection	Single-layer board—1s	44.3	°C/W
				Four-layer board—2s2p	31	

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.

The internal voltage regulator requires external bulk capacitance (C_{REGn}) to be connected to the device to provide a stable low voltage digital supply to the device. Also required for stability is the C_{DEC2} capacitor at ballast collector. This is needed to minimize sharp injection current when ballast is turning ON. Apart from the bulk capacitance, user should connect EMI/decoupling cap (C_{REGP}) at each V_{DD_LV}/V_{SS_LV} pin pair.

3.8.1.1 Recommendations

- The external NPN driver must be BCP68 type.
- V_{DD_LV} should be implemented as a power plane from the emitter of the ballast transistor.
- 10 µF capacitors should be connected to the 4 pins closest to the outside of the package and should be evenly distributed around the package. For BGA packages, the balls should be used are D8, H14, R9, J3–one cap on each side of package.
  - There should be a track direct from the capacitor to this pin (pin also connects to V_{DD_LV} plane). The tracks ESR should be less than 100 mΩ.
  - The remaining V_{DD_LV} pins (exact number will vary with package) should be decoupled with 0.1 µF caps, connected to the pin as per 10 µF.

(see *Section 3.4: Recommended operating conditions*).

3.8.2 V_{DD_BV} options

- Option 1: V_{DD_BV} shared with $V_{DD\_HV\_A}$

  V_{DD_BV} must be star routed from $V_{DD\_HV\_A}$ from the common source. This is to eliminate ballast noise injection on the MCU.
- Option 2: V_{DD_BV} independent of the MCU supply

  V_{DD_BV} > 2.6 V for correct functionality. The device is not monitoring this supply hence the external component must meet the 2.6 V criteria through external monitoring if required.

Table 23. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	External ballast stability capacitance	—	40	—	60	µF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	—	—	—	0.2	W
C_{REGP}	SR	—	Decoupling capacitance (Close to the pin)	$V_{DD\_HV\_A/HV\_B}/V_{SS\_HV}$ pair		100	—	nF
				V_{DD_LV}/V_{SS_LV} pair		100	—	nF
C_{DEC2}	SR	—	Stability capacitance regulator supply (Close to the ballast collector)	V_{DD_BV}/V_{SS_HV}	10	—	40	µF
V_{MREG}	CC	P	Main regulator output voltage	After trimming T_A = 25 °C	1.20	1.28	1.32	V

Table 27. Data flash memory—Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ(1)	Initial max(2)	Max(3)	
$T_{wprogram}$	CC	C	Word (32 bits) program time(4)	—	30	70	500	µs
$T_{16Kpperase}$			16 KB block pre-program and erase time	—	700	800	5000	ms
T_{eslat}		D	Erase Suspend Latency	—	—	30	30	µs
t_{ESRT}(5)		C	Erase Suspend Request Rate	10	—	—	—	ms
t_{PABT}		D	Program Abort Latency	—	—	12	12	µs
t_{EAPT}		D	Erase Abort Latency	—	—	30	30	µs

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. It is time between erase suspend resume and next erase suspend.

Table 28. Flash memory module life

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Typ	
P/E	CC	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100000	100000	cycles
			Number of program/erase cycles per block for 32 Kbyte blocks over the operating temperature range (T_J)	—	10000	100000	cycles
			Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0–1000 P/E cycles	20	—	years
				Blocks with 10000 P/E cycles	10	—	years
				Blocks with 100000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 29. Flash memory read access timing(1)

Symbol		C	Parameter	Conditions(2)		Frequency range	Unit
				Code flash memory	Data flash memory		
f_{READ}	CC	P	Maximum frequency for Flash reading	5 wait states	13 wait states	120 —100	MHz
		C		4 wait states	11 wait states	100—80	
		D		3 wait states	9 wait states	80—64	
		C		2 wait states	7 wait states	64—40	
		C		1 wait states	4 wait states	40—20	
		C		0 wait states	2 wait states	20—0	

1. Max speed is the maximum speed allowed including PLL frequency modulation (FM).
2. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.

3.10.2 Flash memory power supply DC characteristics

Table 30 shows the flash memory power supply DC characteristics on external supply.

Table 30. Flash memory power supply DC electrical characteristics

Symbol		Parameter	Conditions(1)		Value(2)			Unit
					Min	Typ	Max	
I_{CFREAD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ on read access	Flash memory module read f_{CPU} = 120 MHz + 2%(4)	Code flash memory			33	mA
I_{DFREAD}(3)				Data flash memory			13	
I_{CFMOD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ (program/erase)	Program/Erase on-going while reading flash memory registers f_{CPU} = 120 MHz + 2% (4)	Code flash memory			52	mA
I_{DFMOD}(3)				Data flash memory			13	
I_{CFLPW}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ during flash memory low power mode		Code flash memory			1.1	mA
I_{CFPWD}(3)	CC	Sum of the current consumption on $V_{DD\_HV\_A}$ during flash memory power down mode		Code flash memory			150	µA
I_{DFPWD}(3)				Data flash memory			150	

1. V_{DD} = 3.3 V ± 10 % / 5.0 V ± 10 %, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Data based on characterization results, not tested in production.
4. f_{CPU} 120 MHz + 2 % can be achieved over full temperature 125 °C ambient, 150 °C junction temperature.

Figure 14. Slow external crystal oscillator (32 kHz) electrical characteristics

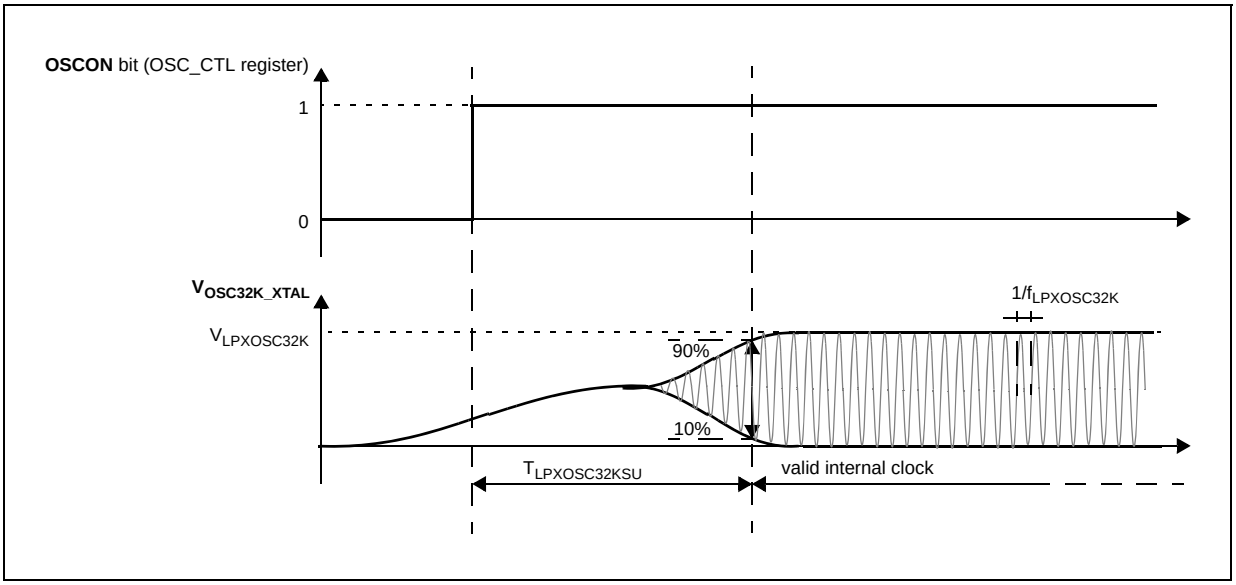


Table 38. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
g_{mSXOSC}	CC	—	Slow external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%,	13[3]	—	33[3]	µA/V
				V_{DD} = 5.0 V ± 10%	15[3]	—	35[3]	
V_{SXOSC}	CC	T	Oscillation amplitude	—	1.2	1.4	1.7	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—	1.2	—	4.4	µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	7	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[4]	s

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Based on ATE CZ
4. Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

3.17.1.2 ADC electrical characteristics

Table 42. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 43. ADC conversion characteristics (10-bit ADC_0)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC0}	SR	—	Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V_{SS_HV})[2]	—	–0.1	—	0.1	V
V_{DD_ADC0}	SR	—	Voltage on VDD_HV_ADC0 pin (ADC_0 reference) with respect to ground (V_{SS_HV})	—	$V_{DD\_HV\_A}$ – 0.1	—	$V_{DD\_HV\_A}$ + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC0} – 0.1	—	V_{DD_ADC0} + 0.1	V
f_{ADC0}	SR	—	ADC_0 analog frequency	—	6	—	32 + 2%	MHz
t_{ADC0_PU}	SR	—	ADC_0 power up delay	—	—	—	1.5	µs
t_{ADC0_S}	CC	T	Sample time[4]	f_{ADC} = 32 MHz	500	—		ns
t_{ADC0_C}	CC	P	Conversion time[5],[6]	f_{ADC} = 32 MHz	0.625	—		µs
				f_{ADC} = 30 MHz	0.700	—		
C_S	CC	D	ADC_0 input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC_0 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_0 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_0 input pin capacitance 3	—	—	—	1	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	3	kΩ

Table 43. ADC conversion characteristics (10-bit ADC_0) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
R_{SW2}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
I_{INJ}[7]	SR	—	Input current Injection	Current injection on one ADC_0 input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
| INL |	CC	T	Absolute value for integral non-linearity	No overload		—	0.5	1.5	LSB
| DNL |	CC	T	Absolute differential non-linearity	No overload		—	0.5	1.0	LSB
| OFS |	CC	T	Absolute offset error	—		—	0.5	—	LSB
| GNE |	CC	T	Absolute gain error	—		—	0.6	—	LSB
TUEP	CC	P	Total unadjusted error[8] for precise channels, input only pins	Without current injection		–2	0.6	2	LSB
		T		With current injection		–3		3	
TUEX	CC	T	Total unadjusted error[8] for extended channel	Without current injection		–3	1	3	LSB
		T		With current injection		–4		4	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS_HV} must be common (to be tied together externally).
3. V_{AINx} may exceed V_{SS_ADC0} and V_{DD_ADC0} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
4. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC0_S}. After the end of the sample time t_{ADC0_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC0_S} depend on programming.
5. This parameter does not include the sample time t_{ADC0_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.
6. Refer to ADC conversion table for detailed calculations.
7. PB10 should not have any current injected. It can disturb accuracy on other ADC_0 pins.
8. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

Table 44. Conversion characteristics (12-bit ADC_1)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC1}	SR	—	Voltage on VSS_HV_ADC1 (ADC_1 reference) pin with respect to ground (V_{SS_HV})[2]	—	–0.1		0.1	V
V_{DD_ADC1}	SR	—	Voltage on VDD_HV_ADC1 pin (ADC_1 reference) with respect to ground (V_{SS_HV})	—	$V_{DD\_HV\_A}$ – 0.1		$V_{DD\_HV\_A}$ + 0.1	V
V_{AINx}[3], [4]	SR	—	Analog input voltage[5]	—	V_{SS_ADC1} – 0.1		V_{DD_ADC1} + 0.1	V
f_{ADC1}	SR	—	ADC_1 analog frequency	—	8 + 2%		32 + 2%	MHz
t_{ADC1_PU}	SR	—	ADC_1 power up delay	—	1.5			µs
t_{ADC1_S}	CC	T	Sample time[6] VDD=5.0 V	—	440			ns
			Sample time[6] VDD=3.3 V	—	530			
t_{ADC1_C}	CC	P	Conversion time[7], [8] VDD=5.0 V	f_{ADC1} = 32 MHz	2			µs
			Conversion time[7], [6] VDD =5.0 V	$f_{ADC\ 1}$= 30 MHz	2.1			
			Conversion time[7], [6] VDD=3.3 V	$f_{ADC\ 1}$= 20 MHz	3			
			Conversion time[7], [6] VDD =3.3 V	f_{ADC1} = 15 MHz	3.01			
C_S	CC	D	ADC_1 input sampling capacitance	—	5			pF
C_{P1}	CC	D	ADC_1 input pin capacitance 1	—	3			pF
C_{P2}	CC	D	ADC_1 input pin capacitance 2	—	1			pF

3.18.2 MII Transmit Signal Timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency in 2:1 mode and two times the TX_CLK frequency in 1:1 mode.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

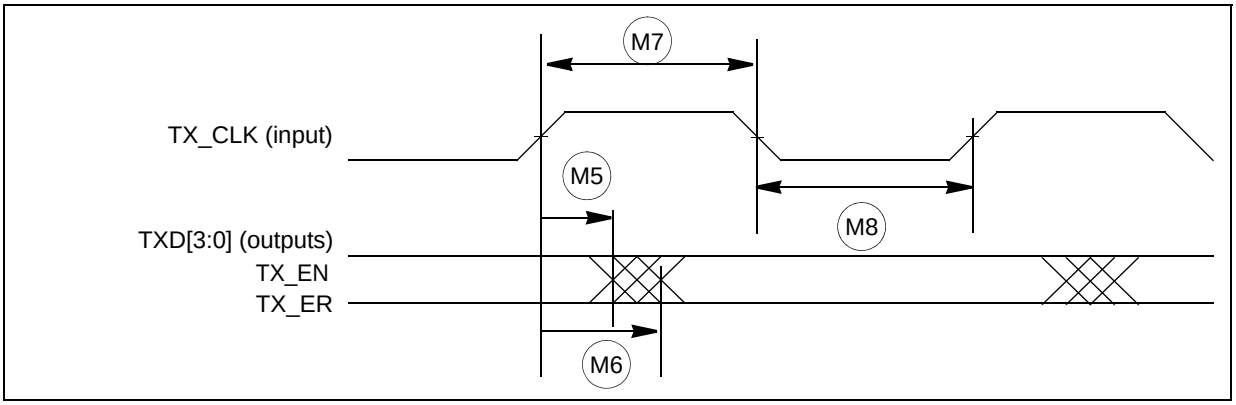
Refer to the Fast Ethernet Controller (FEC) chapter of the SPC564B74 and SPC56EC74 Reference Manual for details of this option and how to enable it.

Table 46. MII transmit signal timing(1)

Spec	Characteristic	Min	Max	Unit
M5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1. Output pads configured with SRE = 0b11.

Figure 22. MII transmit signal timing diagram



3.18.3 MII Async Inputs Signal Timing (CRS and COL)

Table 47. MII Async Inputs Signal Timing(1)

Spec	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

1. Output pads configured with SRE = 0b11.

Appendix A Abbreviations

Table 56 lists abbreviations used but not defined elsewhere in this document.

Table 56. Abbreviations

Abbreviation	Meaning
CS	Chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

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