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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x5b, 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1765t-i-sl

PIC16(L)F1764/5/8/9

14/20-Pin, 8-Bit Flash Microcontroller Product Brief

Description:

PIC16(L)F176X microcontrollers combine intelligent analog integration with digital peripherals to suit a variety of functions and end equipment. These 14/20-pin devices provide features like 10-bit A/D, op amps, zero-cross detect, high current IOs, communication, peripheral pin select and other key peripherals that make this family appealing in applications looking for design flexibility.

Core Features:

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-Bit Timers
- Up to Three 16-Bit Timers
- Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR) with Selectable Trip Point
- Extended Watchdog Timer (EWDT):
  - Low-power 31 kHz WDT
  - Software-selectable prescaler
  - Software-selectable enable

Memory:

- Up to 14 KB Flash Program Memory
- Up to 1024 Bytes Data RAM Memory
- Direct, Indirect and Relative Addressing modes
- High Endurance Flash (HEF)
  - 128B of nonvolatile data storage
  - 100K Erase/Write cycles

Operating Characteristics:

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF176X)
  - 2.3V to 5.5V (PIC16F176X)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

eXtreme Low-Power (XLP) Features:

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical
- Low-Power BOR (LPBOR):
  - 200 nA in Sleep

Digital Peripherals:

- Configurable Logic Cell (CLC):
  - Up to three CLCs; up to four selected inputs
  - Integrated combinational and state logic
- Up to Two Complementary Output Generators (COG):
  - Push-Pull, Full-Bridge and Steering modes
- Up to Two Capture/Compare/PWM (CCP) modules
- Pulse-Width Modulators (PWM):
  - Up to two 10-bit PWMs
  - Up to two 16-bit PWMs
- Peripheral Pin Select (PPS):
  - Configure any digital pin to output
- Serial Communications:
  - Enhanced USART (EUSART)
  - SPI, I^2C™, RS-232, RS-485, LIN compatible
  - Auto-Baud Detect, auto-wake-up on start
- Up to 18 I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
- Up to Two Data Signal Modulators (DSM)

Intelligent Analog Peripherals:

- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 12 external channels
  - Conversion available during Sleep
- Up to Two Operational Amplifiers (OPA):
  - Selectable internal and external channels
  - High and low GBWP operating modes
- Up to Four Fast Comparators (COMP):
  - Low-Power/High-Speed mode
  - Up to five external inverting inputs
  - Up to eight external non-inverting inputs
  - Fixed Voltage Reference at non-inverting input(s)
  - Comparator outputs externally accessible
- Digital-to-Analog Converters (DAC):
  - Up to two 10-bit resolution DACs
  - Up to two 5-bit resolution DACs

- Voltage Reference:
  - Fixed Voltage Reference (FVR): 1.024V, 2.048V and 4.096V output levels
- Zero-Cross Detector (ZCD):
  - Detect high voltage AC signal
- Programmable Ramp Generator (PRG)
  - Slope compensation
  - Ramp generation
- High Current Drive I/Os:
  - 100 mA capacity
  - Low voltage

Clocking Structure:

- 16 MHz Internal Oscillator:
  - ±1% at calibration
  - Selectable frequency range 32 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- 4x Phase-Locked Loop (PLL):
  - For up to 32 MHz internal operation
- External Oscillator Block with:
  - Three external clock modes up to 32 MHz

TABLE 1: PIC16(L)F1764/5/8/9 FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (words)	High-Endurance Flash (B)	Data SRAM (bytes)	I/O Pins	8/16-bit Timer	Comparator	10-bit ADC (ch)	5/10-bit DAC	CCP	10/16-bit PWM	COG	DSM	CLC	Op Amp	Zero-Cross Detect	Programmable Ramp Gen	High Current I/Os	Peripheral Pin Select	EUSART	I²C™/SPI	Debug(1)
PIC16(L)F1764	**(A)**	4096	128	512	12	4/3	2	8	1/1	1	1/1	1	1	3	1	1	1	2	Y	1	1	I/H
PIC16(L)F1765	**(A)**	8192	128	1024	12	4/3	2	8	1/1	1	1/1	1	1	3	1	1	1	2	Y	1	1	I/H
PIC16(L)F1768	**(B)**	4096	128	512	18	4/3	4	12	2/2	2	2/2	2	2	3	2	1	2	2	Y	1	1	I/H
PIC16(L)F1769	**(B)**	8192	128	1024	18	4/3	4	12	2/2	2	2/2	2	2	3	2	1	2	2	Y	1	1	I/H

Note 1: Debugging Methods: (I) – Integrated on Chip; (H) – via ICD header; E – Emulation Product.

Data Sheet Index:

A. Future Release PIC16(L)F1764/5 Data Sheet, 14-Pin, 8-bit Flash Microcontrollers.

B. Future Release PIC16(L)F1768/9 Data Sheet, 20-Pin, 8-bit Flash Microcontrollers.

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

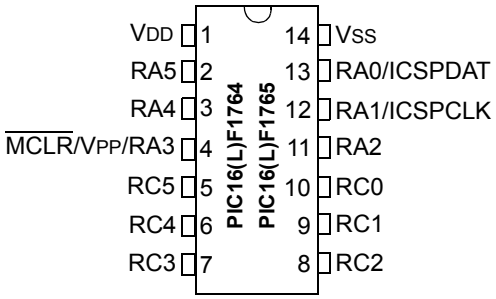
TABLE 2: PACKAGES

Packages	PDIP	SOIC	TSSOP	QFN	SSOP
PIC16(L)F1764	X	X	X	X	
PIC16(L)F1765	X	X	X	X	
PIC16(L)F1768	X	X		X	X
PIC16(L)F1769	X	X		X	X

Note: Pin details are subject to change.

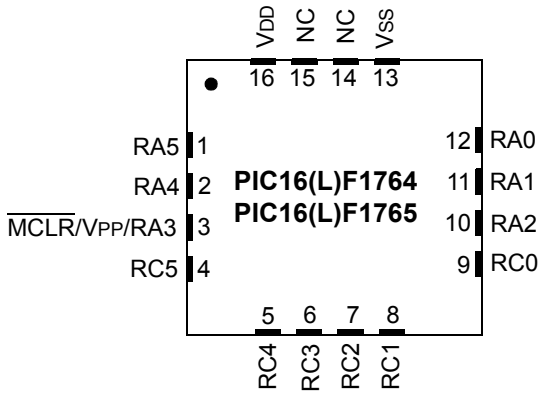
PIN DIAGRAMS

FIGURE 1: 14-PIN PDIP, SOIC, TSSOP



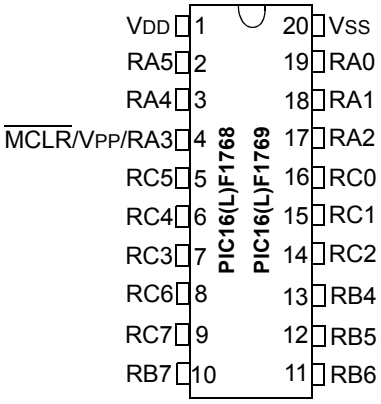
Note: See Table 3 for location of all peripheral functions.

FIGURE 2: 16-PIN QFN (4x4)



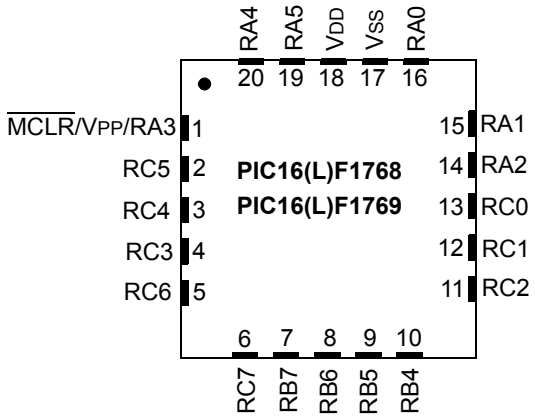
Note: See Table 3 for location of all peripheral functions.

FIGURE 3: 20-PIN PDIP, SOIC, SSOP



Note: See Table 4 for location of all peripheral functions.

FIGURE 4: 20-PIN QFN (4x4)



Note: See Table 4 for location of all peripheral functions.

PIN ALLOCATION TABLES

TABLE 3: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16(L)F1764 AND PIC16(L)F1765)

I/O	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN	ADC	Reference	DAC	Op Amp	Comparator	Zero Cross	Ramp Generator	Timers	PWM	CCP	COG	CLC	DSM	EUSART	MSSP	Interrupts	Pull-ups	Hi Current	Basic
RA0	13	12	AN0	VREF- DAC1REF- DAC2REF-	DAC1OUT1 DAC2OUT1	—	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	ICSPDAT
RA1	12	11	AN1	VREF+ DAC1REF+ DAC2REF+	—	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	ICSPCLK
RA2	11	10	AN2	—	—	—	—	ZCD	—	T0CKI(1)	—	—	COG1IN(1)	—	—	—	—	INT(1) IOC	Y	—	—
RA3	4	3	—	—	—	—	—	—	—	T6CKI(1)	—	—	—	—	DSM1CH(1)	—	—	IOC	Y	—	VPP MCLR ICD
RA4	3	2	AN3	—	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	DSM1CL(1)	—	—	IOC	Y	—	OSC2 CLKOUT
RA5	2	1	—	—	—	—	—	—	—	T1CKI(1) T2CKI(1) SOSCI	—	—	—	CLCIN3(1)	DSM1MOD(1)	—	—	IOC	Y	—	OSC1 CLKIN
RC0	10	9	AN4	—	—	OPA1IN+	C2IN0+	—	—	T5CKI(1)	—	—	—	—	—	—	SCL(1) SCK(1,3)	IOC	Y	—	—
RC1	9	8	AN5	—	—	OPA1IN-	C1IN1- C2IN1-	—	—	T4CKI(1)	—	—	—	CLCIN2(1)	—	—	SDI(1) SDA(1,3)	IOC	Y	—	—
RC2	8	7	AN6	—	—	OPA1OUT	C1IN2- C2IN2-	—	RG1IN0	—	—	—	—	—	—	—	—	IOC	Y	—	—
RC3	7	6	AN7	—	—	—	C1IN3- C2IN3-	—	—	T5G(1)	—	—	—	CLCIN0(1)	—	—	$\overline{SS}$(1)	IOC	Y	—	—
RC4	6	5	—	—	—	—	—	—	RG1R(1)	T3G(1)	—	—	—	CLCIN1(1)	—	CK(1)	—	IOC	Y	Y	—
RC5	5	4	—	—	—	—	—	—	RG1F(1)	T3CKI(1)	—	CCP1(1)	—	—	—	RX(1,3)	—	IOC	Y	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	—	—	C1OUT	—	—	—	PWM3OUT	CCP1	COG1A	CLC1OUT	DSM1OUT	DT(3)	SDO	INT	—	—	—
	—	—	—	—	—	—	C2OUT	—	—	—	PWM5OUT	—	COG1B	CLC2OUT	—	TX	SDA(3)	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG1C	CLC3OUT	—	CK	SCK(3)	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG1D	—	—	—	SCL	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1768 AND PIC16(L)F1769)

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	ADC	Reference	DAC	Op Amp	Comparator	Zero Cross	Ramp Generator	Timers	PWM	CCP	COG	CLC	DSM	EUSART	MSSP	Interrupts	Pull-ups	Hi Current	Basic
RA0	19	16	AN0	VREF- DAC1REF- DAC2REF- DAC3REF- DAC4REF-	DAC1OUT1 DAC2OUT1 DAC3OUT1 DAC4OUT1	—	C1IN0+ C3IN0+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	ICSPDAT
RA1	18	15	AN1	VREF+ DAC1REF+ DAC2REF+ DAC3REF+ DAC4REF+	—	—	C1IN0- C2IN0- C3IN0- C4IN0-	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	ICSPCLK
RA2	17	14	AN2	—	—	—	—	ZCD	—	T0CKI(1)	—	—	COG1IN(1) COG2IN(1)	—	—	—	—	INT(1) IOC	Y	—	—
RA3	4	1	—	—	—	—	—	—	—	T6CKI(1)	—	—	—	—	DSM1CH(1) DSM2CH(1)	—	—	IOC	Y	—	$\overline{VPP}$ $\overline{MCLR}$ $\overline{ICD}$
RA4	3	20	AN3	—	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	DSM1CL(1) DSM2CL(1)	—	—	IOC	Y	—	OSC2 CLKOUT
RA5	2	19	—	—	—	—	—	—	—	T1CKI(1) T2CKI(1) SOSCI	—	—	—	CLCIN3(1)	DSM1MOD(1) DSM2MOD(1)	—	—	IOC	Y	—	OSC1 CLKIN
RB4	13	10	AN10	—	—	OPA1IN0-	—	—	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3)	IOC	Y	—	—
RB5	12	9	AN11	—	—	OPA1IN0+	—	—	—	—	—	—	—	—	—	RX(1,3)	—	IOC	Y	—	—
RB6	11	8	—	—	—	—	C1IN1+ C3IN1+	—	—	—	—	—	—	—	—	—	SCL(1) SCK(1,3)	IOC	Y	—	—
RB7	10	7	—	—	—	—	C2IN1- C4IN1+	—	—	—	—	—	—	—	—	CK(1)	—	IOC	Y	—	—
RC0	16	13	AN4	—	—	—	C2IN0- C4IN0+	—	—	T5CKI(1)	—	—	—	—	—	—	—	IOC	Y	—	—
RC1	15	12	AN5	—	—	—	C1IN1- C2IN1- C3IN1- C4IN1-	—	—	T4CKI(1)	—	—	—	CLCIN2(1)	—	—	—	IOC	Y	—	—
RC2	14	11	AN6	—	—	OPA1OUT OPA2IN1- OPA2IN1+	C1IN2- C2IN2-	—	RG1IN0 RG2IN1	—	—	—	—	—	—	—	—	IOC	Y	—	—

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RC3	7	4	AN7	—	—	OPA2OUT OPA1IN1- OPA1IN1+	C1IN3- C2IN3- C3IN3- C4IN3-	—	RG2IN0 RG1IN1	T5G(1)	—	CCP2(1)	—	CLCIN0(1)	—	—	—	IOC	Y	—	—
RC4	6	3	—	—	—	—	—	—	RG1R(1) RG2R(1)	T3G(1)	—	—	—	CLCIN1(1)	—	—	—	IOC	Y	Y	—
RC5	5	2	—	—	—	—	—	—	RG1F(1) RG2F(1)	T3CKI(1)	—	CCP1(1)	—	—	—	—	—	IOC	Y	Y	—
RC6	8	5	AN8	—	—	OPA2IN0-	—	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	IOC	Y	—	—
RC7	9	6	AN9	—	—	OPA2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
OUT(2)	—	—	—	—	—	—	C1OUT	—	—	—	PWM3OUT	CCP1	COG1A	CLC1OUT	DSM1OUT	DT(3)	SDO	—	—	—	—
	—	—	—	—	—	—	C2OUT	—	—	—	PWM4OUT	CCP2	COG1B	CLC2OUT	DSM2OUT	TX	SDA(3)	—	—	—	—
	—	—	—	—	—	—	C3OUT	—	—	—	PWM5OUT	—	COG1C	CLC3OUT	—	CK	SCK(3)	—	—	—	—
	—	—	—	—	—	—	C4OUT	—	—	—	PWM6OUT	—	COG1D	—	—	—	SCL	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2A	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2B	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2C	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2D	—	—	—	—	—	—	—	—

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