



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

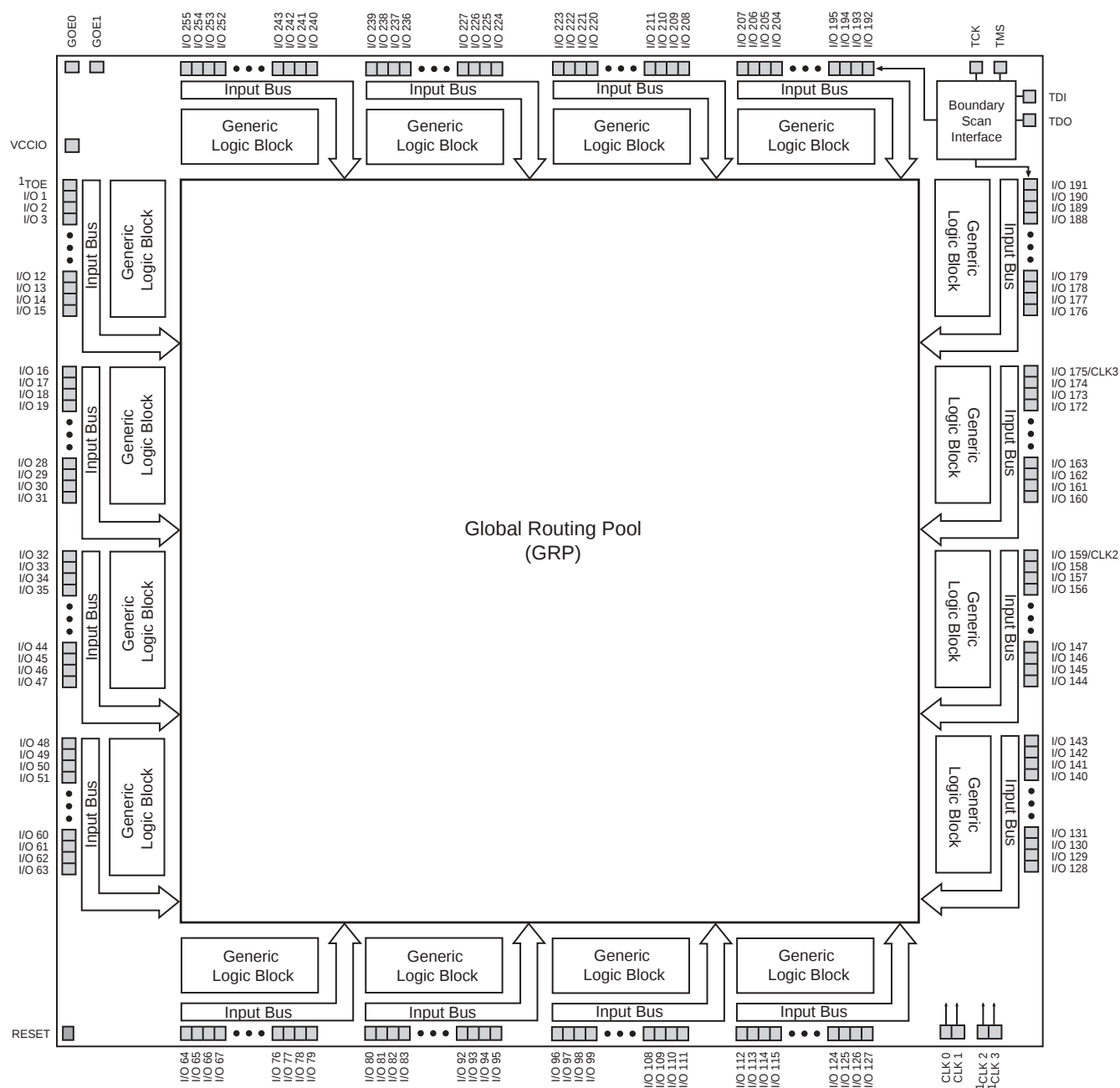
Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	24000
Number of I/O	192
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	272-BBGA
Supplier Device Package	272-BGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/isplsi-5512ve-125lb272

Functional Block Diagram

Figure 1. ispLSI 5512VE Functional Block Diagram (256-I/O Option)



1. CLK2, CLK3 and TOE signals are multiplexed with I/O signals. Use the table below to determine which I/O is shared by package type.

Package Type	Multiplexed Signals		
256 fpBGA	I/O 119 / CLK2	I/O 131 / CLK3	I/O 0 / TOE
272 BGA	I/O 119 / CLK2	I/O 131 / CLK 3	I/O 0 / TOE
388 fpBGA	I/O 179 / CLK2	I/O 197 / CLK 3	I/O 0 / TOE
388 BGA	I/O 179 / CLK2	I/O 197 / CLK 3	I/O 0 / TOE

ispLSI 5000VE Description (Continued)

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch and the necessary clocks and control logic to allow combinatorial or registered operation. The macrocells each have two outputs, combinatorial and registered. This dual output capability from the macrocell allows efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O pad facilitates efficient use of this feature to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also available to each register, eliminating the need to gate the clock to the macrocell registers. Reset for the macrocell register is provided from the global signal, its polarity is user-selectable. The macrocell register can be programmed to operate as a D-type register or a D-type latch.

The 32 outputs from the GLB can drive both the Global Routing Pool and the device I/O cells. The Global Routing Pool contains one input from each macrocell output and one input from each I/O pin.

The input buffer threshold has programmable TTL/3.3V/2.5V compatible levels. The output driver can source 4mA and sink 8mA in 3.3V mode. The output drivers have a separate VCCIO reference input which is independent of the main VCC supply for the device. This feature allows individual output drivers to drive either 3.3V (from the device VCC) or 2.5V (from the VCCIO pin) output levels while the device logic and the output current drive are powered from device supply (VCC). The output drivers also provide individually programmable edge rates and open drain capability. A programmable pullup resistor is provided to tie off unused inputs. Additionally, a programmable bus-hold latch is available to hold tristate outputs in their last valid state until the bus is driven again by some device.

The ispLSI 5000VE Family features 3.3V, non-volatile in-system programmability for both the logic and the interconnect structures, providing the means to develop truly reconfigurable systems. Programming is achieved through the industry standard IEEE 1149.1-compliant Boundary Scan interface. Boundary Scan test is also supported through the same interface.

An enhanced, multiple cell security scheme is provided that prevents reading of the JEDEC programming file when secured. After the device has been secured using this mechanism, the only way to clear the security is to execute a bulk-erase instruction.

ispLSI 5000VE Family Members

The ispLSI 5000VE Family ranges from 128 macrocells to 512 macrocells and operates from a 3.3V power supply. All family members will be available with multiple package options. The ispLSI 5000VE Family device matrix showing the various bondout options is shown in the table below.

The interconnect structure (GRP) is very similar to Lattice's existing ispLSI 1000, 2000 and 3000 families, but with an enhanced interconnect structure for optimal pin locking and logic routing. This eliminates the need for registered I/O cells or an Output Routing Pool.

The ispLSI 5000VE encompasses the innovative features of the ispLSI 5000VA family with several enhancements. The macrocell is optimized and the T-type flip flop option is removed. To improve the efficiency of design fits, the Product Term Reset Logic is simplified and the polarity option as well as the Global Preset function are removed. The programmable output-delay feature (skew option) is also removed. As a result, the ispLSI 5000VE is not JEDEC compatible with the ispLSI 5000VA. ispLSI 5000VA and 5000VE pinouts may differ in the same package, however all programming and power/ground pins are located in the same locations.

Table 1. ispLSI 5000VE Family

Device	GLBs	Macrocells	Package Type					
			100 TQFP	128 TQFP	256 fpBGA	272 BGA	388 fpBGA	388 BGA
ispLSI 5128VE	4	128	—	96 I/O	—	—	—	—
ispLSI 5256VE	8	256	72 I/O	96 I/O	144 I/O	144 I/O	—	—
ispLSI 5384VE	12	384	—	—	192 I/O	192 I/O	—	—
ispLSI 5512VE	16	512	—	—	192 I/O	192 I/O	256 I/O	256 I/O

Figure 2. ispLSI 5512VE Block Diagram (256 I/O Version)

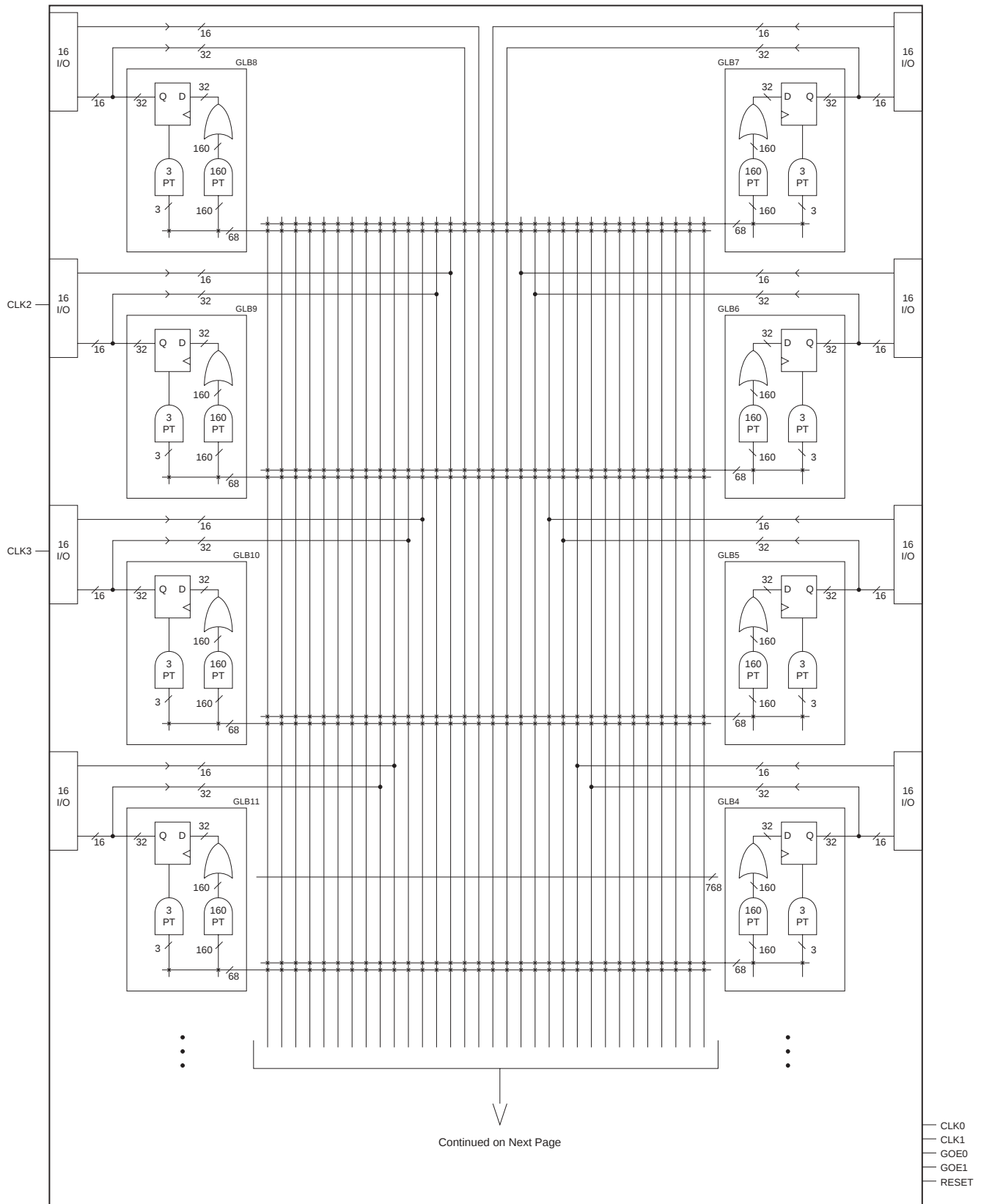


Figure 2. ispLSI 5512VE Block Diagram (256 I/O Version) -- Continued

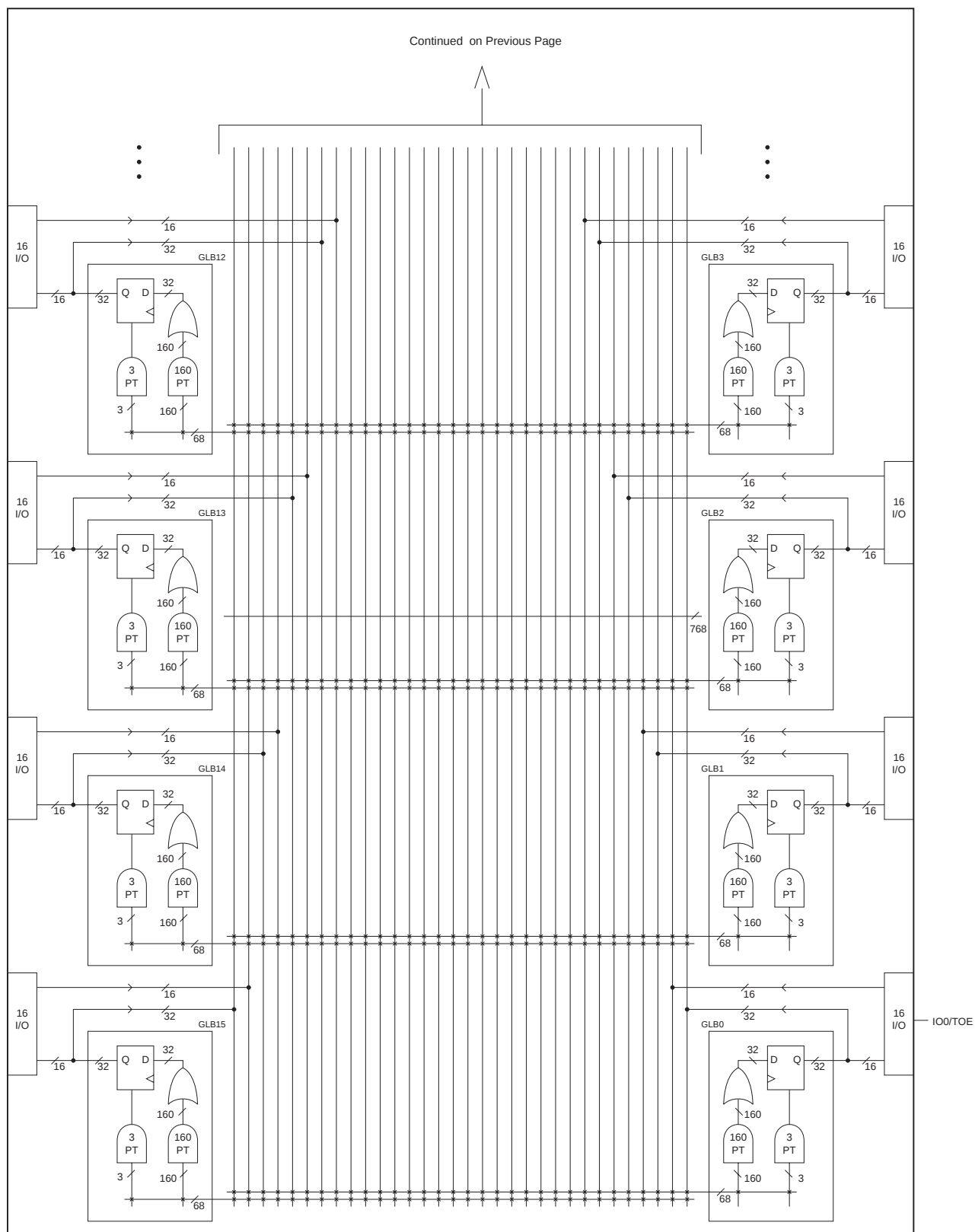


Figure 3. ispLSI 5000VE Generic Logic Block (GLB)

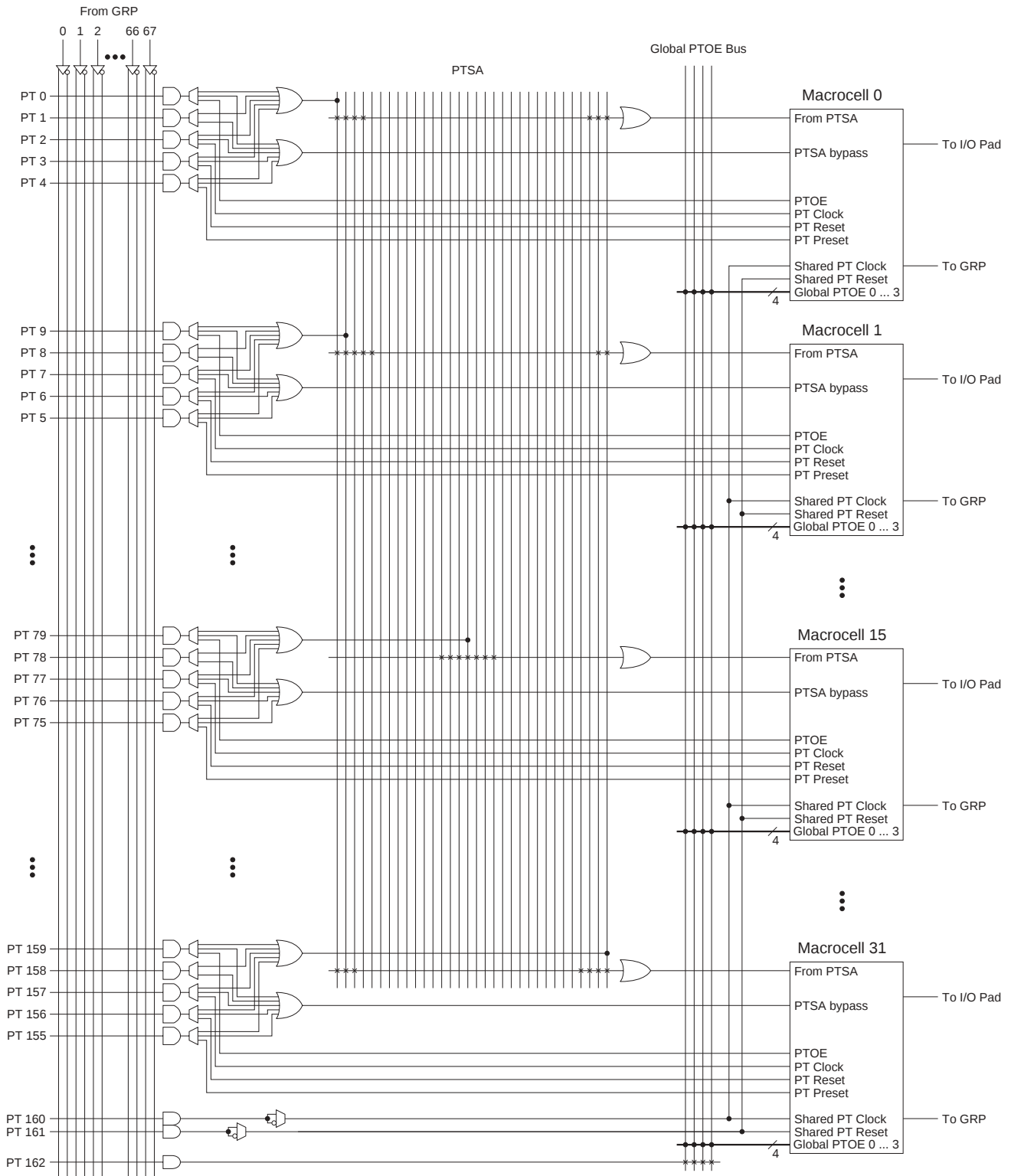
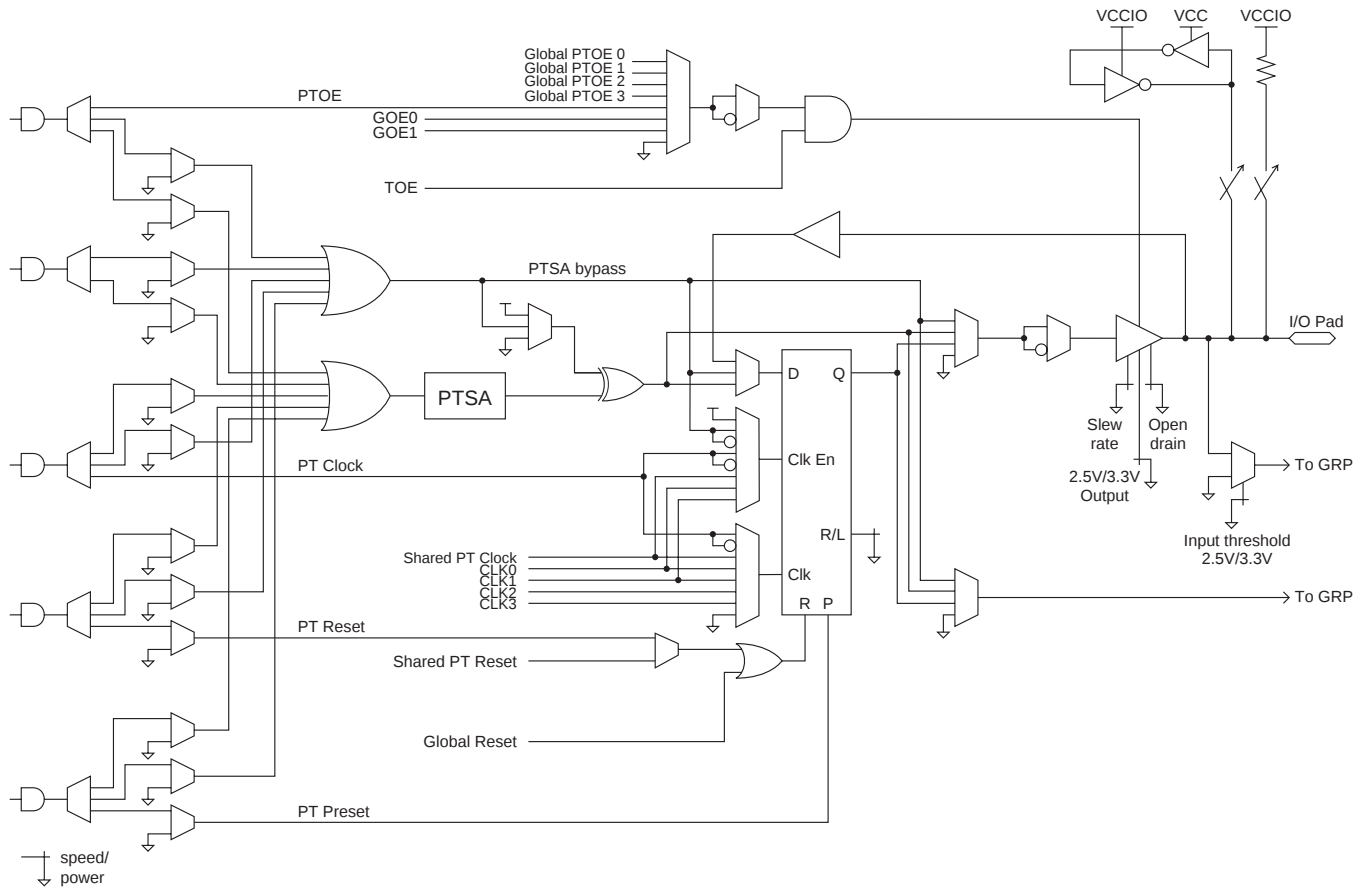


Figure 4. ispLSI 5000VE Macrocell



Note: Not all macrocells have I/O pads.

Global Clock Distribution

The ispLSI 5000VE Family has four dedicated clock input pins: CLK0 - CLK3. CLK0 input is used as the dedicated master clock that has the lowest internal clock skew with no clock inversion to maintain the fastest internal clock

speed. The clock inversion is available on the remaining CLK1 - CLK3 signals. By sharing the pins with the I/O pins, CLK2 and CLK3 can not only be inverted but are also available for logic implementation through GRP signal routing. Figure 5 shows these different clock distribution options.

Figure 5. ispLSI 5000VE Global Clock Structure

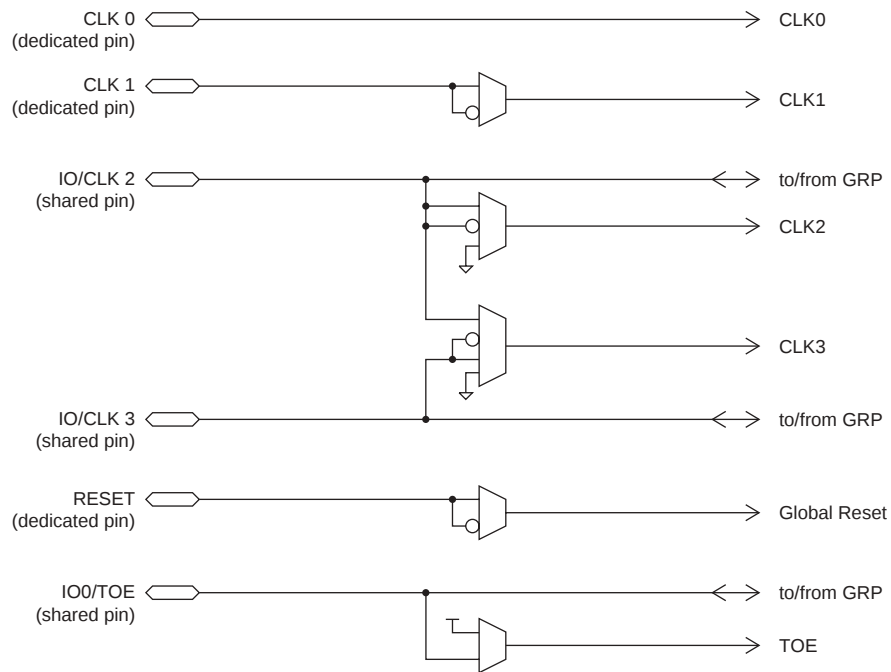


Figure 8. Boundary Scan Waveforms and Timing Specifications



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{btcp}	TCK [BSCAN test] clock pulse width	125	–	ns
t_{btch}	TCK [BSCAN test] pulse width high	62.5	–	ns
t_{btcl}	TCK [BSCAN test] pulse width low	62.5	–	ns
t_{btsu}	TCK [BSCAN test] setup time	25	–	ns
t_{bth}	TCK [BSCAN test] hold time	25	–	ns
t_{rf}	TCK [BSCAN test] rise and fall time	50	–	mV/ns
t_{btco}	TAP controller falling edge of clock to valid output	–	25	ns
t_{btoz}	TAP controller falling edge of clock to data output disable	–	25	ns
t_{btvo}	TAP controller falling edge of clock to data output enable	–	25	ns
$t_{btcp su}$	BSCAN test Capture register setup time	25	–	ns
$t_{btcp h}$	BSCAN test Capture register hold time	25	–	ns
t_{btuco}	BSCAN test Update reg, falling edge of clock to valid output	–	50	ns
$t_{btuo z}$	BSCAN test Update reg, falling edge of clock to output disable	–	50	ns
t_{btuov}	BSCAN test Update reg, falling edge of clock to output enable	–	50	ns

Switching Test Conditions

Input Pulse Levels	GND to $V_{CCIO_{min}}$
Input Rise and Fall Time	$\leq 1.5\text{ns}$ 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 9

3-state levels are measured 0.5V from steady-state active level.

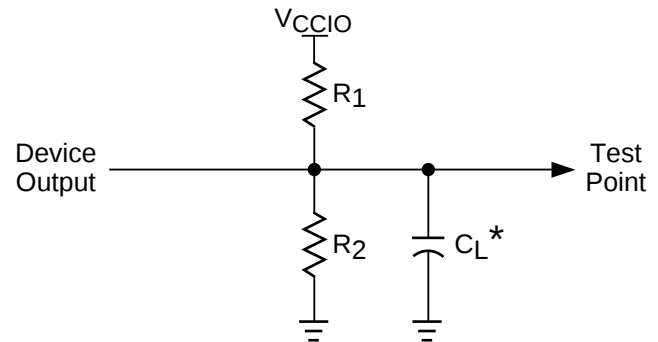
Table 2-0003/5KVE

Output Load Conditions (See Figure 9)

		3.3V		2.5V		
TEST CONDITION		R1	R2	R1	R2	CL
A		316 Ω	348 Ω	511 Ω	475 Ω	35pF
B	Active High	∞	348 Ω	∞	475 Ω	35pF
	Active Low	316 Ω	∞	511 Ω	∞	35pF
C	Active High to Z at $V_{OH}-0.5\text{V}$	∞	348 Ω	∞	475 Ω	5pF
	Active Low to Z at $V_{OL}+0.5\text{V}$	316 Ω	∞	511 Ω	∞	5pF
D	Slow Slew	∞	∞	∞	∞	35pF

Table 2-0004A/5KVE

Figure 9. Test Load



* C_L includes Test Fixture and Probe Capacitance.

0213D

DC Electrical Characteristics for 3.3V Range¹

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCIO}	I/O Reference Voltage		3.0	—	3.6	V
V_{IL}	Input Low Voltage		-0.3	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
V_{OL}	Output Low Voltage	$V_{CCIO} = \text{min}, I_{OL} = 8 \text{ mA}$	—	—	0.4	V
V_{OH}	Output High Voltage	$V_{CCIO} = \text{min}, I_{OH} = -4 \text{ mA}$	2.4	—	—	V

Table 2-0007/5KVE

1. I/O voltage configuration must be set to VCC.

DC Electrical Characteristics for 2.5V Range¹

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V _{CCIO}	I/O Reference Voltage		2.3	–	2.7	V
V _{IL}	Input Low Voltage		-0.3	–	0.7	V
V _{IH}	Input High Voltage		1.7	–	5.25	V
V _{OL}	Output Low Voltage	V _{CCIO} =min, I _{OL} = 100μA	–	–	0.2	V
		V _{CCIO} =min, I _{OL} = 2mA	–	–	0.6	V
V _{OH}	Output High Voltage	V _{CCIO} =min, I _{OH} = -100μA	2.1	–	–	V
		V _{CCIO} =min, I _{OH} = -2mA	1.8	–	–	V

1. I/O voltage configuration must be set to V_{CCIO}.

2.5V/5512VE

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
I _{IL}	Input or I/O Low Leakage Current	0V ≤ V _{IN} ≤ V _{IL} (Max.)	–	–	-10	μA
I _{IH}	Input or I/O High Leakage Current	(V _{CCIO} -0.2)V ≤ V _{IN} ≤ V _{CCIO}	–	–	10	μA
		V _{CCIO} ≤ V _{IN} ≤ 5.25V	–	–	50	μA
I _{PU} ¹	I/O Active Pullup Current	0V ≤ V _{IN} ≤ V _{IL}	–	–	-200	μA
I _{BHL}	Bus Hold Low Sustaining Current	V _{IN} = V _{IL} (max)	40	–	–	μA
I _{BHH}	Bus Hold High Sustaining Current	V _{IN} = V _{IH} (min)	-40	–	–	μA
I _{BHLO}	Bus Hold Low Overdrive Current	0V ≤ V _{IN} ≤ V _{CCIO}	–	–	550	μA
I _{BHLH}	Bus Hold High Overdrive Current	0V ≤ V _{IN} ≤ V _{CCIO}	–	–	-550	μA
I _{BHT}	Bus Hold Trip Points		V _{IL}	–	V _{IH}	V
I _{VCCIO}	Current Needed for V _{CCIO} Pin	All I/Os Pulled-up, (Total I/Os * I _{PU} max)	–	–	30	mA

1. Pullup is capable of pulling to a minimum voltage of V_{OH} under no-load conditions.

DC Char_5KVE

External Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST ³ COND.	DESCRIPTION ^{4,5}	-155		-125		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd1 ⁶	A	Data Prop. Delay, 5PT Bypass	—	6.5	—	7.5	ns
tpd2 ⁶	A	Data Propagation Delay	—	8.0	—	9.5	ns
fmax	A	Clock Frequency with Internal Feedback ¹	155	—	125	—	MHz
fmax (Ext.)	—	Clock Freq. with Ext. Feedback, 1/(tsu2 + tco1)	105	—	87	—	MHz
fmax (Tog.)	—	Clock Frequency, Max Toggle ²	200	—	167	—	MHz
tsu1	—	GLB Reg. Setup Time before Clk, 5PT bypass	4.5	—	5.0	—	ns
tco1 ⁶	A	GLB Reg. Clock to Output Delay	—	3.5	—	4.5	ns
th1	—	GLB Reg. Hold Time after Clock, 5PT bypass	0.0	—	0.0	—	ns
tsu2	—	GLB Reg. Setup Time before Clock	6.0	—	7.0	—	ns
th2	—	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	ns
tsu3	—	GLB Reg. Setup Time before Clock, Input Reg. Path	3.0	—	3.5	—	ns
th3	—	GLB Reg. Hold Time after Clock, Input Reg. Path	0.5	—	0.5	—	ns
tr1	A	Ext. Reset Pin to Output Delay	—	9.0	—	10.0	ns
trw1 ⁷	—	Ext. Reset Pulse Duration	4.5	—	5.0	—	ns
tpden/dis ⁶	B/C	Local Product Term Output Enable/Disable	—	7.0	—	8.5	ns
tgpten/dis ⁶	B/C	Global Product Term Output Enable/Disable	—	13.0	—	14.0	ns
tgen/dis ⁶	B/C	Global OE Input to Output Enable/Disable	—	4.5	—	5.5	ns
tten/dis ⁶	B/C	Test OE Input to Output Enable/Disable	—	9.5	—	10.5	ns
twh	—	Ext. Sync. Clock Pulse Duration, High	2.5	—	3.0	—	ns
twl	—	Ext. Sync. Clock Pulse Duration, Low	2.5	—	3.0	—	ns

1. Standard 16-bit counter using GRP feedback.

2. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.

3. Reference Switching Test Conditions section.

4. Unless noted otherwise, all timing numbers are taken with worst case PTSA fanout, a GRP load of 1 GLB, CLK0, and high-speed AND array.

5. Timing parameters measured using normal active output driver.

6. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O voltage reference.

7. Pulse widths less than minimum may cause unknown output behavior.

Timing Ext.5512ve1.eps

Timing v.2.0

External Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST ³ COND.	DESCRIPTION ^{4,5}	-100		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd1⁶	A	Data Prop. Delay, 5PT Bypass	—	10.0	—	12.0	ns
tpd2⁶	A	Data Propagation Delay	—	12.0	—	15.0	ns
fmax	A	Clock Frequency with Internal Feedback ¹	100	—	80	—	MHz
fmax (Ext.)	—	Clock Freq. with Ext. Feedback, 1/(tsu2 + tco1)	67	—	56	—	MHz
fmax (Tog.)	—	Clock Frequency, Max Toggle ²	125	—	100	—	MHz
tsu1	—	GLB Reg. Setup Time before Clk, 5PT bypass	7.0	—	8.0	—	ns
tco1⁶	A	GLB Reg. Clock to Output Delay	—	6.0	—	7.0	ns
th1	—	GLB Reg. Hold Time after Clock, 5PT bypass	0.0	—	0.0	—	ns
tsu2	—	GLB Reg. Setup Time before Clock	9.0	—	11.0	—	ns
th2	—	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	ns
tsu3	—	GLB Reg. Setup Time before Clock, Input Reg. Path	4.5	—	5.5	—	ns
th3	—	GLB Reg. Hold Time after Clock, Input Reg. Path	1.0	—	1.0	—	ns
tr1	A	Ext. Reset Pin to Output Delay	—	11.5	—	13.0	ns
trw1⁷	—	Ext. Reset Pulse Duration	6.5	—	8.0	—	ns
tpden/dis⁶	B/C	Local Product Term Output Enable/Disable	—	10.0	—	12.0	ns
tgpten/dis⁶	B/C	Global Product Term Output Enable/Disable	—	15.5	—	17.0	ns
tgen/dis⁶	B/C	Global OE Input to Output Enable/Disable	—	7.5	—	9.0	ns
tten/dis⁶	B/C	Test OE Input to Output Enable/Disable	—	11.5	—	12.5	ns
twh	—	Ext. Sync. Clock Pulse Duration, High	4.0	—	5.0	—	ns
tlw	—	Ext. Sync. Clock Pulse Duration, Low	4.0	—	5.0	—	ns

1. Standard 16-bit counter using GRP feedback.

Timing Ext.5512ve2.eps

2. fmax (Toggle) may be less than 1/(twh + tlw). This is to allow for a clock duty cycle of other than 50%.

Timing v.2.0

3. Reference Switching Test Conditions section.

4. Unless noted otherwise, all timing numbers are taken with worst case PTSA fanout, a GRP load of 1 GLB, CLK0, and high-speed AND array.

5. Timing parameters measured using normal active output driver.

6. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O reference.

7. Pulse widths less than minimum may cause unknown output behavior.

Internal Timing Parameters

Over Recommended Operating Conditions

PARAMETER	DESCRIPTION	-155		-125		-100		-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
In/Out Delays										
tin	Input Buffer Delay	–	1.1	–	1.3	–	2.3	–	2.3	ns
tgclk_in	Global Clock Buffer Input Delay (clk0)	–	0.7	–	1.3	–	1.8	–	1.8	ns
trst	Global Reset Pin Delay	–	5.8	–	6.6	–	7.1	–	7.1	ns
tgoe	Global OE Pin Delay	–	3.2	–	3.9	–	5.9	–	7.4	ns
tbuf	Output Buffer Delay	–	2.0	–	2.2	–	2.7	–	3.7	ns
ten	Output Enable Delay	–	1.3	–	1.6	–	1.6	–	1.6	ns
tdis	Output Disable Delay	–	1.3	–	1.6	–	1.6	–	1.6	ns
Routing/GLB Delays										
troute	GRP and Logic Delay	–	3.1	–	3.6	–	4.0	–	4.5	ns
tpdb	5-pt Bypass Propagation Delay	–	0.3	–	0.4	–	1.0	–	1.5	ns
tpdi	Combinatorial Propagation Delay	–	0.0	–	0.0	–	0.0	–	0.0	ns
tptsa	Product Term Sharing Array	–	1.8	–	2.4	–	3.0	–	4.5	ns
tfbk	Internal Feedback Delay	–	0.0	–	0.0	–	0.0	–	0.5	ns
tinreg	Input Buffer to Macrocell Register Delay	–	1.9	–	2.5	–	2.5	–	3.5	ns
Register/Latch Delays										
ts	Register Setup Time	0.7	–	1.0	–	1.5	–	1.5	–	ns
ts_pt	Register Setup Time (Product Term Clock)	0.7	–	1.0	–	1.5	–	1.5	–	ns
th	Register Hold Time	2.8	–	3.0	–	4.0	–	5.0	–	ns
tcoi	Register Clock to GLB Output Delay	–	0.8	–	1.0	–	1.5	–	1.5	ns
tsl	Latch Setup Time	0.7	–	1.0	–	1.5	–	1.5	–	ns
thl	Latch Hold Time	2.8	–	3.0	–	4.0	–	5.0	–	ns
tgoi	Latch Gate to GLB Output Delay	–	0.8	–	1.0	–	1.5	–	1.5	ns
tpdli	GLB Latch propagation Delay	–	1.0	–	1.5	–	2.0	–	2.5	ns
tces	Clock Enable Setup Time	4.1	–	4.3	–	5.3	–	6.3	–	ns
tceh	Clock Enable Hold Time	0.9	–	1.7	–	2.7	–	3.7	–	ns
tsri	Asynchronous Set/Reset to GLB Output Delay	–	1.2	–	1.2	–	1.7	–	2.2	ns
tsrr	Asynchronous Set/Reset Recovery Time	0.9	–	1.2	–	1.2	–	2.2	–	ns
Control Delays										
tptclk	Macrocell PT Clock Delay	–	0.4	–	0.4	–	0.5	–	0.5	ns
tbclk	Block PT Clock Delay	–	1.4	–	1.9	–	2.5	–	2.5	ns
tptsr	Macrocell PT Set/Reset Delay	–	1.1	–	3.7	–	4.8	–	4.8	ns
tbsr	Block PT Set/Reset Delay	–	2.1	–	5.7	–	6.8	–	6.8	ns
tptoe	Macrocell PT OE Delay	–	1.5	–	2.0	–	2.1	–	3.6	ns
tgptoe	Global PT OE Delay	–	7.5	–	7.5	–	7.6	–	8.6	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further details. Timing v.2.0

ispLSI 5512VE Timing Parameters (continued)

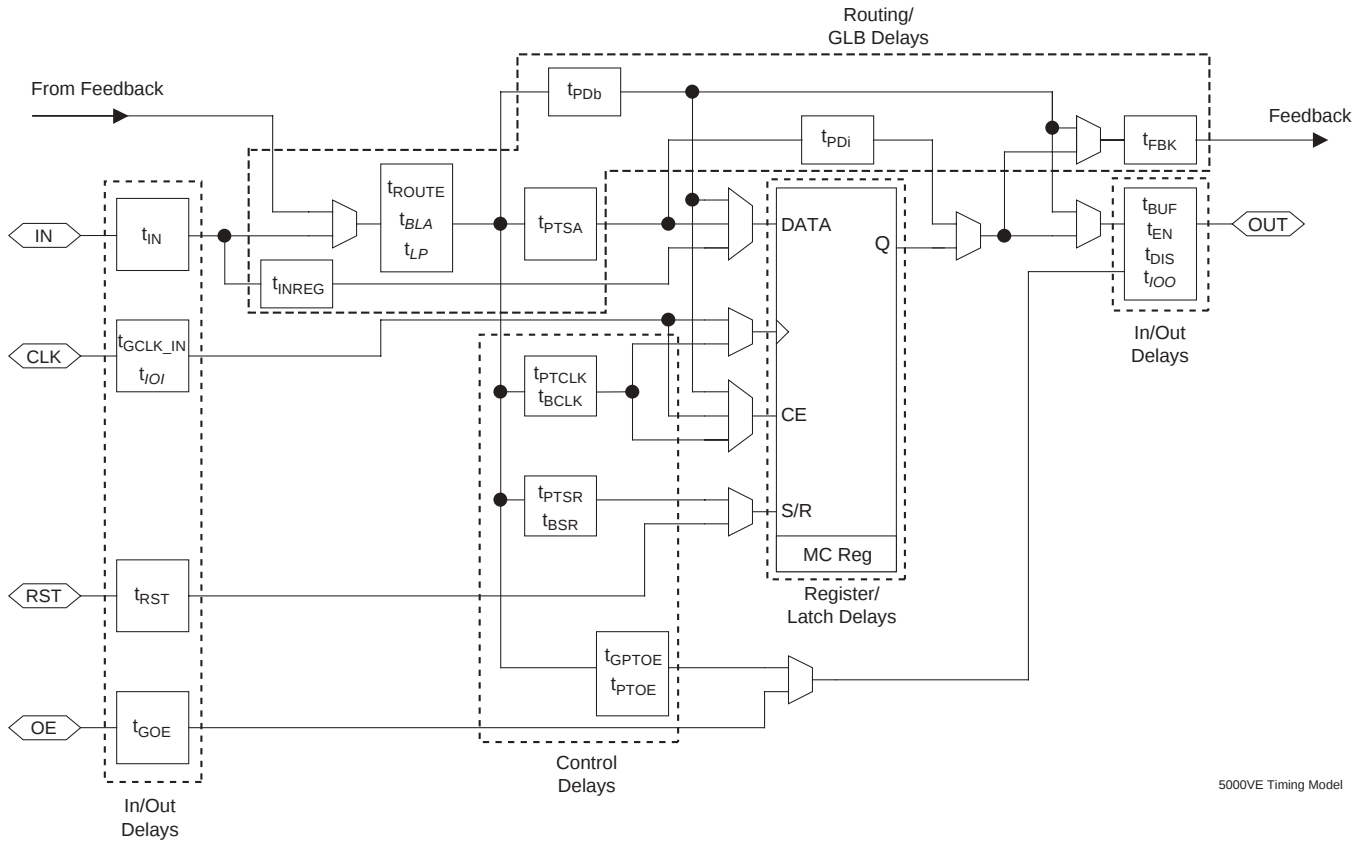
ADDER TYPE	BASE PARAMETER	ADDER				UNITS
		-155	-125	-100	-80	
Routing Adders						
t _{lp}	t _{route}	1.0	1.5	1.5	1.5	ns
Tioi Input Adders						
clk1	t _{gclk_in}	1.5	1.7	1.7	1.7	ns
clk2	t _{gclk_in}	1.5	1.7	1.7	1.7	ns
clk3	t _{gclk_in}	1.5	1.7	1.7	1.7	ns
Tioo Output Adders ¹						
Slow Slew I/O	t _{buf} , t _{en}	4.0	4.0	4.0	4.0	ns
LVTTL_out	t _{buf} , t _{en} , t _{dis}	0.0	0.0	0.0	0.0	ns
LVC MOS25_out	t _{buf} , t _{en} , t _{dis}	0.5	0.5	0.5	0.5	ns
LVC MOS33_out	t _{buf} , t _{en} , t _{dis}	0.0	0.0	0.0	0.0	ns
Tbla Additional Block Loading Adders						
1	t _{route}	0.1	0.1	0.1	0.1	ns
2	t _{route}	0.2	0.2	0.2	0.2	ns
3	t _{route}	0.2	0.3	0.3	0.3	ns
4	t _{route}	0.3	0.4	0.4	0.4	ns
5	t _{route}	0.4	0.5	0.5	0.5	ns
6	t _{route}	0.5	0.6	0.6	0.6	ns
7	t _{route}	0.6	0.7	0.7	0.7	ns
8	t _{route}	0.6	0.8	0.8	0.8	ns
9	t _{route}	0.7	0.9	0.9	0.9	ns
10	t _{route}	0.8	1.0	1.0	1.0	ns
11	t _{route}	0.9	1.1	1.1	1.1	ns
12	t _{route}	1.0	1.2	1.2	1.2	ns
13	t _{route}	1.0	1.3	1.3	1.3	ns
14	t _{route}	1.1	1.4	1.4	1.4	ns
15	t _{route}	1.2	1.5	1.5	1.5	ns

¹Timing for open drain configurations is the same as non-open drain configurations.

Timing Table/5512VE
Timing v.2.0

Note: Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for details.

ispLSI 5512VE Timing Model



5000VE Timing Model

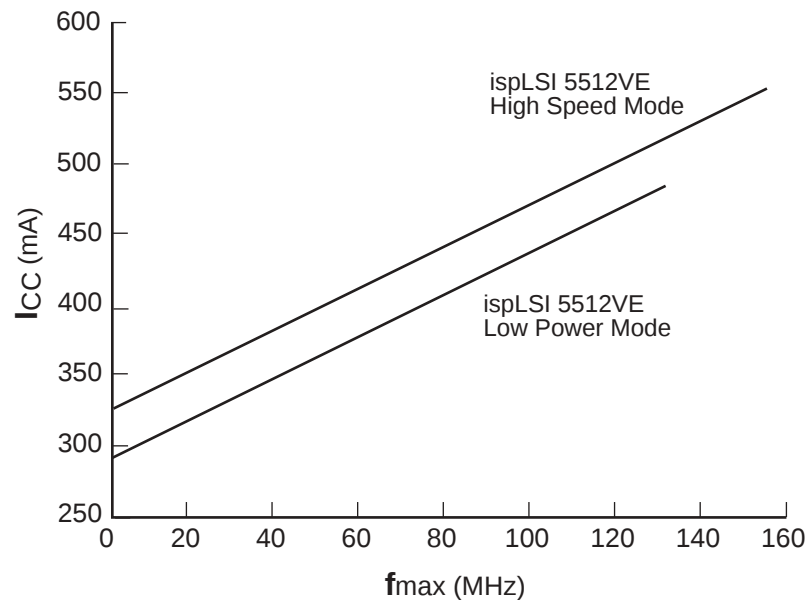
Note: Italicized parameters are delay adders above and beyond default conditions (i.e. GRP load of one GLB, CLK0, high-speed AND Array and VCC I/O option).

Power Consumption

Power consumption in the ispLSI 5512VE device depends on two primary factors: the speed at which the device is operating and the number of product terms used. The product terms have a fuse-selectable speed/power tradeoff setting. Each group of five product terms has a single speed/power tradeoff control fuse that acts on the complete group of five. The fast “high-speed”

setting operates product terms at their normal full power consumption. For portions of the logic that can tolerate longer propagation delays, selecting the slower “low-power” setting will reduce the power dissipation for these product terms. Figure 10 shows the relationship between power and operating frequency.

Figure 10. Typical Device Power Consumption vs fmax



Notes: Configuration of 32 16-bit Counters
Typical Current at 3.3V, 25° C

I_{CC} can be estimated for the ispLSI 5512VE using the following equation:

High Speed Mode: $I_{CC} = 30 + (\# \text{ of PTs} * 0.3030) + (\# \text{ of nets} * F_{max} * 0.00273)$

Low Power Mode: $I_{CC} = 30 + (\# \text{ of PTs} * 0.2676) + (\# \text{ of nets} * F_{max} * 0.00273)$

of PTs = Number of Product Terms used in design

of nets = Number of Signals used in device

Fmax = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions ($V_{CC} = 3.3V$, room temperature) and an assumption of one GLB load on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127/5512VE

Signal Descriptions

Signal Name	Description
TMS	Input - This pin is the Test Mode Select input, which is used to control the JTAG state machine.
TCK	Input - This pin is the Test Clock input pin used to clock through the JTAG state machine.
TDI	Input - This pin is the JTAG Test Data In pin used to load data.
TDO	Output - This pin is the JTAG Test Data Out pin used to shift data out.
TOE / I/O0	Input/Output - This pin functions as either the Test Output Enable pin or an I/O pin based upon customer's design. TOE tristates all I/O pins when a logic low is driven.
GOE0, GOE1	Input - These two pins are the Global Output Enable input pins.
RESET	Dedicated Reset Input - This pin resets all registers in the device. The global polarity (active high or low input) for this pin is selectable.
I/O	Input/Output – These are the general purpose I/O used by the logic array.
GND	Ground
NC ¹	No connect.
VCC	Vcc
CLK0, CLK1	Dedicated clock inputs for all registers. Both clocks are muxed before being used as the clock input to all registers in the device.
CLK2 / I/O, CLK3 / I/O	Input/Output - These pins share functionality. They can be used as dedicated clock inputs for all registers, as well as I/O pins.
VCCIO	Input - This pin is used for optional 2.5V outputs. Every I/O can independently select either 3.3V or the optional voltage as its output level. If the optional output voltage is not required, this pin must be connected to the Vcc supply. Programmable pull-up resistors and bus-hold latches only draw current from this supply.

1. NC pins are not to be connected to any active signals, VCC or GND.

Signal Configuration

ispLSI 5512VE 272-Ball BGA (1.27mm Ball Pitch / 27.0mm x 27.0mm Body Size)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O 114	I/O 115	I/O 119/ CLK2	NC ¹	I/O 122	I/O 126	I/O 129	I/O 132	I/O 136	I/O 139	I/O 140	I/O 142	I/O 146	I/O 149	I/O 151	I/O 154	I/O 158	I/O 160	I/O 164	GND	A
B	NC ¹	NC ¹	NC ¹	I/O 116	I/O 121	I/O 125	I/O 128	I/O 131/ CLK3	I/O 135	I/O 137	I/O 141	I/O 143	I/O 147	I/O 150	I/O 153	I/O 157	I/O 159	NC ¹	I/O 163	I/O 165	B
C	I/O 111	NC ¹	NC ¹	I/O 117	I/O 120	I/O 123	I/O 127	I/O 130	I/O 134	I/O 138	CLK0	I/O 144	I/O 148	I/O 152	I/O 156	NC ¹	I/O 162	NC ¹	I/O 166	I/O 169	C
D	I/O 109	NC ¹	I/O 113	GND	I/O 118	VCC	I/O 124	GND	I/O 133	VCC	CLK1	I/O 145	GND	I/O 155	VCC	I/O 161	GND	NC ¹	I/O 167	I/O 170	D
E	I/O 105	I/O 108	I/O 110	I/O 112	ispLSI 5512VE Bottom View 												I/O 168	I/O 171	NC ¹	I/O 172	E
F	I/O 102	I/O 104	I/O 107	VCC													VCC	I/O 173	I/O 175	I/O 176	F
G	I/O 100	I/O 101	I/O 103	I/O 106													I/O 174	I/O 177	I/O 178	I/O 179	G
H	I/O 97	I/O 98	I/O 99	GND													GND	I/O 180	I/O 181	I/O 182	H
J	TDO	VCCIO	RESET	I/O 96													I/O 183	I/O 184	I/O 185	I/O 186	J
K	I/O 92	I/O 93	I/O 94	I/O 95													VCC	I/O 188	I/O 187	I/O 189	K
L	I/O 91	I/O 89	I/O 90	VCC													TCK	TMS	I/O 191	I/O 190	L
M	I/O 88	I/O 87	I/O 86	I/O 85													I/O 2	I/O 1	I/O 0/ TOE	TDI	M
N	I/O 84	I/O 83	I/O 82	GND													GND	I/O 5	I/O 4	I/O 3	N
P	I/O 81	NC ¹	I/O 80	I/O 77													I/O 12	I/O 9	I/O 7	I/O 6	P
R	I/O 79	I/O 78	I/O 76	VCC													VCC	NC ¹	I/O 10	I/O 8	R
T	NC ¹	I/O 75	I/O 74	NC ¹													NC ¹	I/O 14	I/O 13	I/O 11	T
U	I/O 73	I/O 70	I/O 71	GND	I/O 64	VCC	I/O 58	GND	I/O 48	GOE1	VCC	I/O 37	GND	I/O 28	VCC	I/O 21	GND	NC ¹	NC ¹	NC ¹	U
V	I/O 72	I/O 69	I/O 68	I/O 65	I/O 62	I/O 59	I/O 55	I/O 51	I/O 47	GOE0	I/O 42	I/O 38	I/O 34	I/O 31	I/O 27	I/O 24	I/O 20	I/O 17	I/O 16	I/O 15	V
W	NC ¹	NC ¹	I/O 66	NC ¹	I/O 60	I/O 56	I/O 53	I/O 50	I/O 46	I/O 45	I/O 41	I/O 39	I/O 35	I/O 32	I/O 29	I/O 25	NC ¹	I/O 19	NC ¹	NC ¹	W
Y	NC ¹	I/O 67	I/O 63	I/O 61	I/O 57	I/O 54	I/O 52	I/O 49	NC ¹	I/O 44	I/O 43	I/O 40	I/O 36	I/O 33	I/O 30	I/O 26	I/O 23	I/O 22	NC ¹	I/O 18	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

1. NCs are not to be connected to any active signals, Vcc or GND.

Note: Ball A1 indicator dot on top side of package.

Signal Configuration

ispLSI 5512VE 388-Ball fpBGA (1.0mm Ball Pitch / 23.0mm x 23.0mm Body Size)

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O 170	I/O 174	I/O 178	I/O 181	I/O 184	I/O 189	I/O 192	I/O 196	I/O 201	I/O 202	I/O 207	I/O 211	I/O 215	I/O 218	I/O 223	I/O 226	I/O 231	I/O 234	I/O 237	NC ¹	GND	A
B	I/O 169	GND	I/O 171	I/O 175	I/O179/ CLK2	I/O 182	I/O 187	I/O 191	I/O 195	I/O 200	I/O 204	I/O 208	CLK0	I/O 216	I/O 219	I/O 224	I/O 228	I/O 233	I/O 236	I/O 241	GND	NC ¹	B
C	I/O 164	I/O 165	GND	I/O 172	I/O 177	I/O 180	I/O 186	I/O 190	I/O 193	I/O 199	I/O 205	I/O 209	I/O 213	I/O 217	I/O 221	I/O 227	I/O 232	I/O 235	I/O 240	GND	I/O 242	I/O 245	C
D	I/O 161	I/O 163	I/O 168	GND	I/O 173	VCC	I/O 183	I/O 188	VCC	I/O 198	VCC	I/O 210	I/O 214	VCC	I/O 225	I/O 229	VCC	I/O 238	GND	I/O 243	I/O 246	I/O 249	D
E	I/O 156	I/O 160	I/O 162	I/O 166															I/O 244	I/O 247	I/O 250	I/O 252	E
F	I/O 153	I/O 155	I/O 159	VCC															VCC	I/O 251	I/O 253	I/O 256	F
G	I/O 147	I/O 151	I/O 154	I/O 157															I/O 254	I/O 255	I/O 258	I/O 259	G
H	I/O 145	I/O 146	I/O 148	I/O 152															I/O 260	I/O 261	I/O 262	I/O 263	H
J	VCCIO	RESET	I/O 144	VCC															VCC	I/O 264	I/O 265	I/O 268	J
K	I/O 140	I/O 141	I/O 142	TDO															I/O 269	I/O 270	I/O 271	I/O 272	K
L	I/O 135	I/O 136	I/O 137	I/O 139															VCC	I/O 276	I/O 274	I/O 273	L
M	I/O 131	I/O 132	I/O 134	VCC															I/O 281	I/O 280	I/O 279	I/O 278	M
N	I/O 130	I/O 128	I/O 127	I/O 126															TMS	I/O 285	I/O 283	I/O 282	N
P	I/O 125	I/O 123	I/O 122	VCC															VCC	TCK	TDI	I/O 286	P
R	I/O 121	I/O 119	I/O 118	I/O 116															I/O 7	I/O 4	I/O 1	I/O0/ TOE	R
T	I/O 117	I/O 115	I/O 114	I/O 110															I/O 13	I/O 9	I/O 6	I/O 2	T
U	I/O 113	I/O 112	I/O 108	VCC															VCC	I/O 14	I/O 10	I/O 8	U
V	I/O 109	I/O 107	I/O 105	I/O 101															I/O 23	I/O 17	I/O 15	I/O 11	V
W	I/O 106	I/O 104	I/O 100	GND	I/O 94	VCC	I/O 85	I/O 80	VCC	I/O 69	I/O 65	VCC	I/O 53	VCC	I/O 44	I/O 38	VCC	I/O 28	GND	I/O 24	I/O 18	I/O 16	W
Y	I/O 103	I/O 99	GND	I/O 95	I/O 90	I/O 87	I/O 82	I/O 77	I/O 72	GOE0	I/O 64	I/O 60	I/O 54	I/O 49	I/O 45	I/O 41	I/O 35	I/O 32	I/O 27	GND	I/O 22	I/O 19	Y
AA	I/O 98	GND	I/O 96	I/O 91	I/O 88	I/O 84	I/O 79	I/O 74	I/O 71	I/O 68	I/O 63	I/O 59	I/O 55	I/O 50	I/O 46	I/O 42	I/O 37	I/O 34	I/O 31	I/O 26	GND	I/O 20	AA
AB	GND	I/O 97	I/O 92	I/O 89	I/O 86	I/O 81	I/O 78	I/O 73	I/O 70	I/O 67	I/O 62	I/O 58	I/O 56	I/O 51	I/O 47	I/O 43	I/O 40	I/O 36	I/O 33	I/O 29	I/O 25	GND	AB
	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

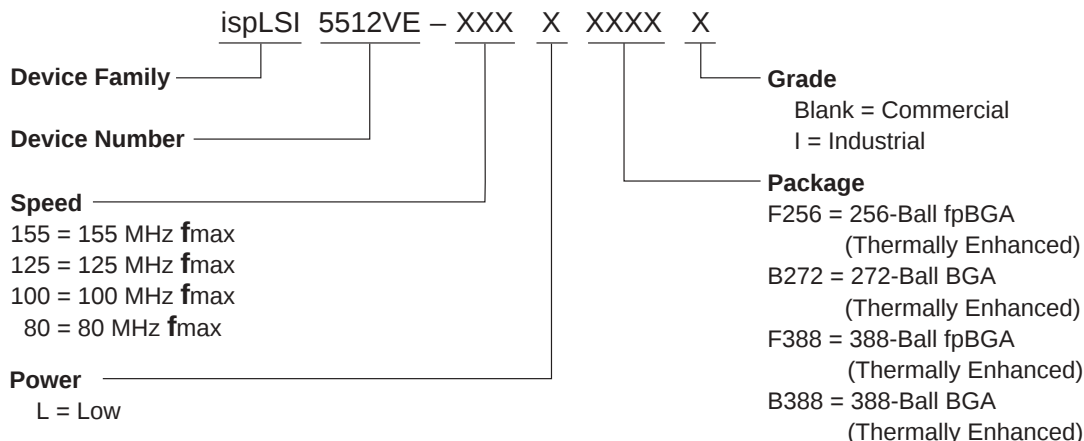
ispLSI 5512VE

Bottom View

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



0212/5512ve

Ordering Information

COMMERCIAL

FAMILY	f_{max} (MHz)	t_{pd} (ns)	ORDERING NUMBER	PACKAGE
ispLSI	155	6.5	ispLSI 5512VE-155LF256	256-Ball fpBGA
	155	6.5	ispLSI 5512VE-155LB272	272-Ball BGA
	155	6.5	ispLSI 5512VE-155LF388	388-Ball fpBGA
	155	6.5	ispLSI 5512VE-155LB388	388-Ball BGA
	125	7.5	ispLSI 5512VE-125LF256	256-Ball fpBGA
	125	7.5	ispLSI 5512VE-125LB272	272-Ball BGA
	125	7.5	ispLSI 5512VE-125LF388	388-Ball fpBGA
	125	7.5	ispLSI 5512VE-125LB388	388-Ball BGA
	100	10	ispLSI 5512VE-100LF256	256-Ball fpBGA
	100	10	ispLSI 5512VE-100LB272	272-Ball BGA
	100	10	ispLSI 5512VE-100LF388	388-Ball fpBGA
	100	10	ispLSI 5512VE-100LB388	388-Ball BGA

Table 2-0041A/5512VE

INDUSTRIAL

FAMILY	f_{max} (MHz)	t_{pd} (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 5512VE-125LF256I	256-Ball fpBGA
	125	7.5	ispLSI 5512VE-125LB272I	272-Ball BGA
	125	7.5	ispLSI 5512VE-125LF388I	388-Ball fpBGA
	125	7.5	ispLSI 5512VE-125LB388I	388-Ball BGA
	100	10	ispLSI 5512VE-100LF256I	256-Ball fpBGA
	100	10	ispLSI 5512VE-100LB272I	272-Ball BGA
	100	10	ispLSI 5512VE-100LF388I	388-Ball fpBGA
	100	10	ispLSI 5512VE-100LB388I	388-Ball BGA
	80	12	ispLSI 5512VE-80LF256I	256-Ball fpBGA
	80	12	ispLSI 5512VE-80LB272I	272-Ball BGA
	80	12	ispLSI 5512VE-80LF388I	388-Ball fpBGA
	80	12	ispLSI 5512VE-80LB388I	388-Ball BGA

The ispLSI 5512VE is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is faster (i.e. ispLSI 5512VE-155LF256) than the Industrial speed grade (i.e. ispLSI 5512VE-125LF256I).

Table 2-0041B/5512VE