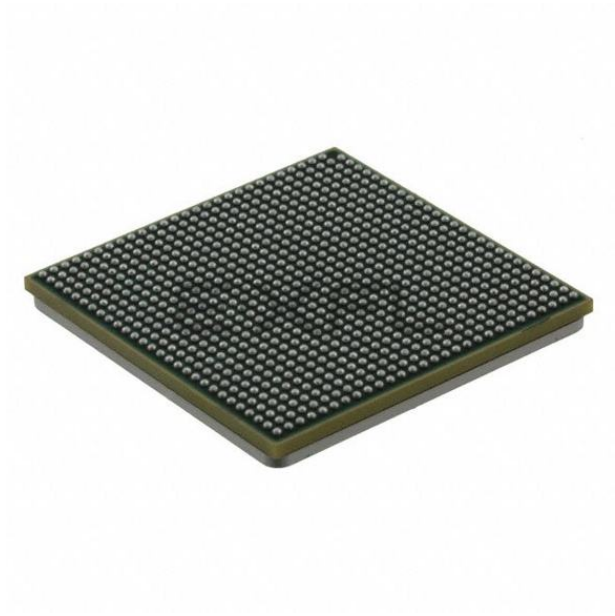

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Quad Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8154esvt1000b

1 Pin Assignment

This section includes diagrams of the MSC8154E package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in Figure 3 with the ball location index numbers.

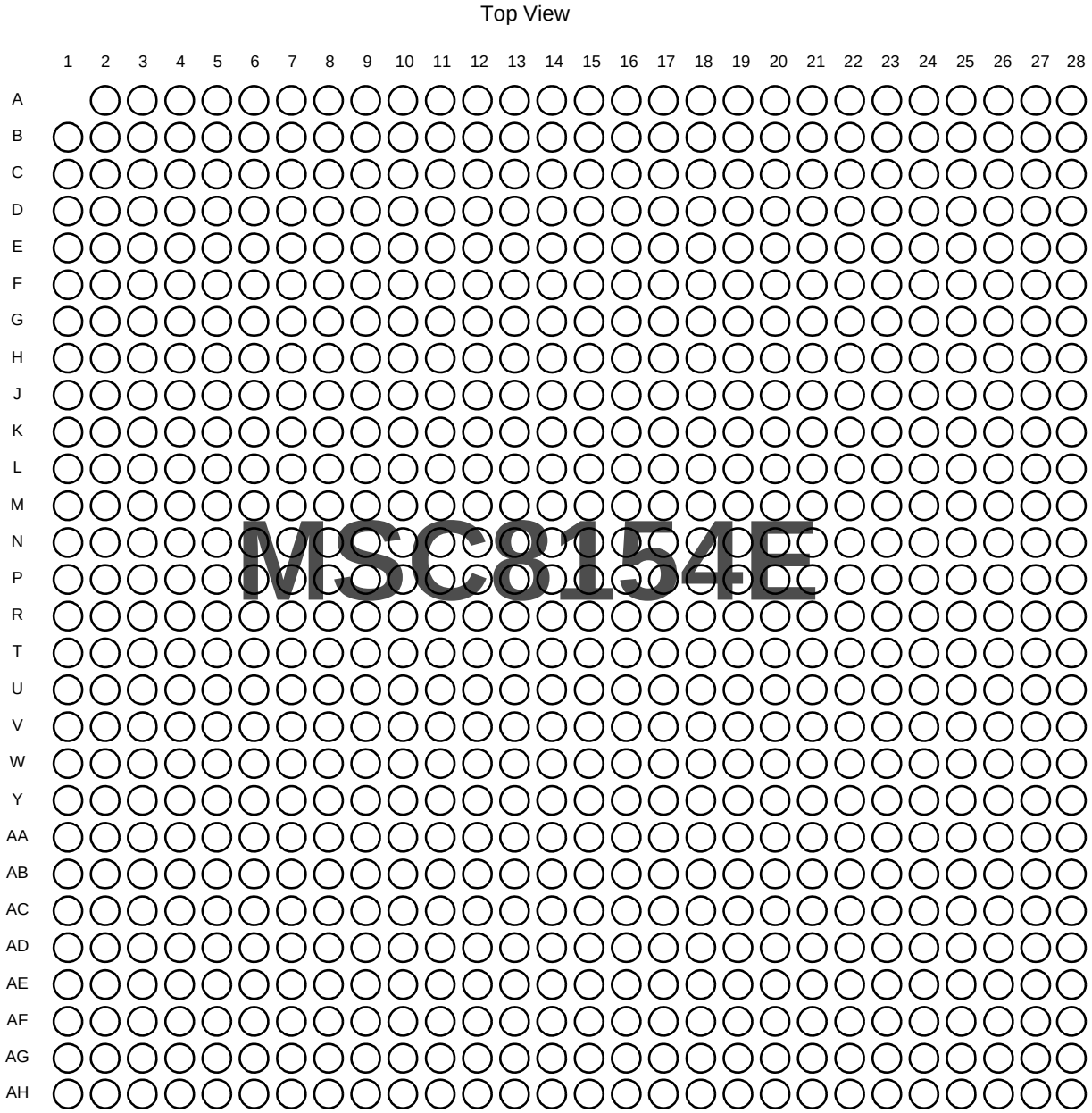

Figure 3. MSC8154E FC-PBGA Package, Top View

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
E17	M2DQ56	I/O	GVDD2
E18	M2DQ57	I/O	GVDD2
E19	$\overline{\text{M2DQS7}}$	I/O	GVDD2
E20	Reserved	NC	—
E21	Reserved	NC	—
E22	Reserved	NC	—
E23	SXPVDD1	Power	N/A
E24	SXPVSS1	Ground	N/A
E25	SR1_PLL_AGND[9]	Ground	SXCVSS1
E26	SR1_PLL_AVDD[9]	Power	SXCVDD1
E27	SXCVSS1	Ground	N/A
E28	SXCVDD1	Power	N/A
F1	VSS	Ground	N/A
F2	GVDD2	Power	N/A
F3	M2DQ16	I/O	GVDD2
F4	VSS	Ground	N/A
F5	GVDD2	Power	N/A
F6	M2DQ17	I/O	GVDD2
F7	VSS	Ground	N/A
F8	GVDD2	Power	N/A
F9	M2BA2	O	GVDD2
F10	VSS	Ground	N/A
F11	GVDD2	Power	N/A
F12	M2A4	O	GVDD2
F13	VSS	Ground	N/A
F14	GVDD2	Power	N/A
F15	M2DQ42	I/O	GVDD2
F16	VSS	Ground	N/A
F17	GVDD2	Power	N/A
F18	M2DQ58	I/O	GVDD2
F19	M2DQS7	I/O	GVDD2
F20	GVDD2	Power	N/A
F21	SXPVDD1	Power	N/A
F22	SXPVSS1	Ground	N/A
F23	SR1_TXD2/SG1_TX[4]	O	SXPVDD1
F24	$\overline{\text{SR1\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD1
F25	SXCVDD1	Power	N/A
F26	SXCVSS1	Ground	N/A
F27	$\overline{\text{SR1\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD1
F28	SR1_RXD2/SG1_RX[4]	I	SXCVDD1
G1	$\overline{\text{M2DQS2}}$	I/O	GVDD2
G2	M2DQS2	I/O	GVDD2
G3	M2DQ19	I/O	GVDD2
G4	M2DM2	O	GVDD2
G5	M2DQ21	I/O	GVDD2
G6	M2DQ22	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N24	$\overline{\text{SR2\_TXD2}}$/$\overline{\text{PE\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	$\overline{\text{SR2\_RXD2}}$/$\overline{\text{PE\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD2
N28	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD[9]	Power	VDD
P9	PLL2_AVDD[9]	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	MVDD	Power	N/A
P16	VSS	Ground	N/A
P17	MVDD	Power	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND[9]	Ground	SXCVSS2
P26	SR2_PLL_AVDD[9]	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	$\overline{\text{NMI}}$	I	QVDD
R3	$\overline{\text{NMI\_OUT}}$[6]	O	QVDD
R4	$\overline{\text{HRESET}}$[6,7]	I/O	QVDD
R5	$\overline{\text{INT\_OUT}}$[6]	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD[9]	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
R13	VSS	Ground	N/A
R14	VDD	Power	N/A
R15	VSS	Ground	N/A
R16	MVDD	Power	N/A
R17	VSS	Ground	N/A
R18	VDD	Power	N/A
R19	VSS	Ground	N/A
R20	VSS	Non-user	N/A
R21	SXPVSS2	Ground	N/A
R22	SXPVDD2	Power	N/A
R23	SR2_TXD1/PE_TXD1[4]	O	SXPVDD2
R24	$\overline{\text{SR2\_TXD1}}$/$\overline{\text{PE\_TXD1}}$[4]	O	SXPVDD2
R25	SXCVSS2	Ground	N/A
R26	SXCVDD2	Power	N/A
R27	$\overline{\text{SR2\_RXD1}}$/$\overline{\text{PE\_RXD1}}$[4]	I	SXCVDD2
R28	SR2_RXD1/PE_RXD1[4]	I	SXCVDD2
T1	VSS	Ground	N/A
T2	TCK	I	QVDD
T3	$\overline{\text{SRESET}}$[6,7]	I/O	QVDD
T4	TDI	I	QVDD
T5	VSS	Ground	N/A
T6	TDO	O	QVDD
T7	VSS	Ground	N/A
T8	VSS	Ground	N/A
T9	QVDD	Power	N/A
T10	VSS	Ground	N/A
T11	VDD	Power	N/A
T12	VSS	Ground	N/A
T13	M3VDD	Power	N/A
T14	VSS	Ground	N/A
T15	VDD	Power	N/A
T16	VSS	Ground	N/A
T17	MVDD	Power	N/A
T18	VSS	Ground	N/A
T19	VDD	Power	N/A
T20	VSS	Ground	N/A
T21	VSS	Non-user	N/A
T22	SR2_IMP_CAL_RX	I	SXCVDD2
T23	SXPVSS2	Ground	N/A
T24	SXPVDD2	Power	N/A
T25	SR2_REF_CLK	I	SXCVDD2
T26	$\overline{\text{SR2\_REF\_CLK}}$	I	SXCVDD2
T27	Reserved	NC	—
T28	Reserved	NC	—
U1	M1DQ8	I/O	GVDD1
U2	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AC19	VSS	Ground	N/A
AC20	GVDD1	Power	N/A
AC21	VSS	Ground	N/A
AC22	NVDD	Power	N/A
AC23	GPIO30/I2C_SCL[5,8]	I/O	NVDD
AC24	GPIO26/TMR3[5,8]	I/O	NVDD
AC25	VSS	Ground	N/A
AC26	NVDD	Power	N/A
AC27	GPIO23/TMR0[5,8]	I/O	NVDD
AC28	GPIO22[5,8]	I/O	NVDD
AD1	M1DQ31	I/O	GVDD1
AD2	M1DQ30	I/O	GVDD1
AD3	M1DQ27	I/O	GVDD1
AD4	M1ECC7	I/O	GVDD1
AD5	M1ECC6	I/O	GVDD1
AD6	M1ECC3	I/O	GVDD1
AD7	M1A9	O	GVDD1
AD8	M1A6	O	GVDD1
AD9	M1A3	O	GVDD1
AD10	M1A10	O	GVDD1
AD11	$\overline{\text{M1RAS}}$	O	GVDD1
AD12	M1A2	O	GVDD1
AD13	M1DQ38	I/O	GVDD1
AD14	$\overline{\text{M1DQS}}$5	I/O	GVDD1
AD15	M1DQS5	I/O	GVDD1
AD16	M1DQ33	I/O	GVDD1
AD17	M1DQ56	I/O	GVDD1
AD18	M1DQ57	I/O	GVDD1
AD19	$\overline{\text{M1DQS7}}$	I/O	GVDD1
AD20	M1DQS7	I/O	GVDD1
AD21	VSS	Ground	N/A
AD22	GE2_TX_CTL	O	NVDD
AD23	GPIO15/DDN0/$\overline{\text{IRQ15}}$/RC15[5,8]	I/O	NVDD
AD24	GPIO13/$\overline{\text{IRQ13}}$/RC13[5,8]	I/O	NVDD
AD25	GE_MDC	O	NVDD
AD26	GE_MDIO	I/O	NVDD
AD27	TDM2TCK/GE1_TD3[3]	I/O	NVDD
AD28	TDM2RCK/GE1_TD0[3]	I/O	NVDD
AE1	GVDD1	Power	N/A
AE2	VSS	Ground	N/A
AE3	M1DQ29	I/O	GVDD1
AE4	GVDD1	Power	N/A
AE5	VSS	Ground	N/A
AE6	M1ECC5	I/O	GVDD1
AE7	GVDD1	Power	N/A
AE8	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AF27	TDM2TDT/GE1_TX_CLK[3]	I/O	NVDD
AF28	TDM3RSN/GE1_RD1[3]	I/O	NVDD
AG1	M1DQ24	I/O	GVDD1
AG2	GVDD1	Power	N/A
AG3	M1DQ25	I/O	GVDD1
AG4	VSS	Ground	N/A
AG5	GVDD1	Power	N/A
AG6	M1ECC1	I/O	GVDD1
AG7	VSS	Ground	N/A
AG8	GVDD1	Power	N/A
AG9	M1A13	O	GVDD1
AG10	VSS	Ground	N/A
AG11	GVDD1	Power	N/A
AG12	$\overline{\text{M1CS1}}$	O	GVDD1
AG13	VSS	Ground	N/A
AG14	GVDD1	Power	N/A
AG15	M1DQ35	I/O	GVDD1
AG16	VSS	Ground	N/A
AG17	GVDD1	Power	N/A
AG18	M1DQ51	I/O	GVDD1
AG19	VSS	Ground	N/A
AG20	GVDD1	Power	N/A
AG21	NVDD	Power	N/A
AG22	TDM1TSN/GE2_TD1[3]	I/O	NVDD
AG23	TDM1RDT/GE2_TX_CLK[3]	I/O	NVDD
AG24	TDM0TCK/GE2_GTX_CLK[3]	I/O	NVDD
AG25	TDM1TDT/GE2_TD0[3]	I/O	NVDD
AG26	VSS	Ground	N/A
AG27	NVDD	Power	N/A
AG28	TDM3RDT/GE1_RD0[3]	I/O	NVDD
AH1	Reserved.	NC	—
AH2	$\overline{\text{M1DQS3}}$	I/O	GVDD1
AH3	M1DQS3	I/O	GVDD1
AH4	M1ECC0	I/O	GVDD1
AH5	$\overline{\text{M1DQS8}}$	I/O	GVDD1
AH6	M1DQS8	I/O	GVDD1
AH7	M1A5	O	GVDD1
AH8	$\overline{\text{M1CK1}}$	O	GVDD1
AH9	M1CK1	O	GVDD1
AH10	$\overline{\text{M1CS0}}$	O	GVDD1
AH11	M1BA0	O	GVDD1
AH12	$\overline{\text{M1CAS}}$	O	GVDD1
AH13	M1DQ34	I/O	GVDD1
AH14	$\overline{\text{M1DQS4}}$	I/O	GVDD1
AH15	M1DQS4	I/O	GVDD1
AH16	M1DQ50	I/O	GVDD1

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8154E Reference Manual*.

2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8154E.

Table 2. Absolute Maximum Ratings

Rating	Power Rail Name	Symbol	Value	Unit
Core supply voltage • Cores 0–3	VDD	V_{DD}	–0.3 to 1.1	V
PLL supply voltage[3]		V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	–0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1	V V V
M3 memory supply voltage	M3VDD	V_{DDM3}	–0.3 to 1.1	V
MAPLE-B supply voltage	MVDD	V_{DDM}	–0.3 to 1.1	V
DDR memory supply voltage • DDR2 mode • DDR3 mode	GVDD1, GVDD2	V_{DDDDR}	 –0.3 to 1.98 –0.3 to 1.65	 V V
DDR reference voltage	MVREF	MV_{REF}	–0.3 to $0.51 \times V_{DDDDR}$	V
Input DDR voltage		V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
I/O voltage excluding DDR and RapidIO lines	NVDD, QVDD	V_{DDIO}	–0.3 to 2.625	V
Input I/O voltage		V_{INIO}	–0.3 to V_{DDIO} + 0.3	V
RapidIO pad voltage	SXPVDD1, SXPVDD2	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O core voltage	SXCVDD1, SXCVDD2	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O PLL voltage[3]		$V_{DDRIOPLL}$	–0.3 to 1.21	V
Input RapidIO I/O voltage		V_{INRIO}	–0.3 to V_{DDSXC} + 0.3	V
Operating temperature		T_J	–40 to 105	°C
Storage temperature range		T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 3**.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8154E (see Figure 37 and Figure 38)

2.5.1.2 DDR3 (1.5V) SDRAM DC Electrical Characteristics

Table 7 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Note: At recommended operating conditions (see Table 3) with V_{DDDDR} = 1.5 V.

Table 7. DDR3 SDRAM Interface DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V	2,3,4
Input high voltage	V_{IH}	MV_{REF} + 0.100	V_{DDDDR}	V	5
Input low voltage	V_{IL}	GND	MV_{REF} – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	µA	6

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times. The DRAM and memory controller can use the same or different sources.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±1% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} with a minimum value of MV_{REF} – 0.4 and a maximum value of MV_{REF} + 0.04 V. V_{TT} should track variations in the DC-level of MV_{REF}.
4. The voltage regulator for MV_{REF} must be able to supply up to 250 µA.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ signals are available in the IBIS models.
6. Output leakage is measured with all outputs are disabled, $0 V \le V_{OUT} \le V_{DDDDR}$.

2.5.1.3 DDR2/DDR3 SDRAM Capacitance

Table 8 provides the DDR controller interface capacitance for DDR2 and DDR3 memory.

Note: At recommended operating conditions (see Table 3) with V_{DDDDR} = 1.8 V for DDR2 memory or V_{DDDDR} = 1.5 V for DDR3 memory.

Table 8. DDR2/DDR3 SDRAM Capacitance

Parameter	Symbol	Min	Max	Unit
I/O capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF
Delta I/O capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF

Note: Guaranteed by FAB process and micro-construction.

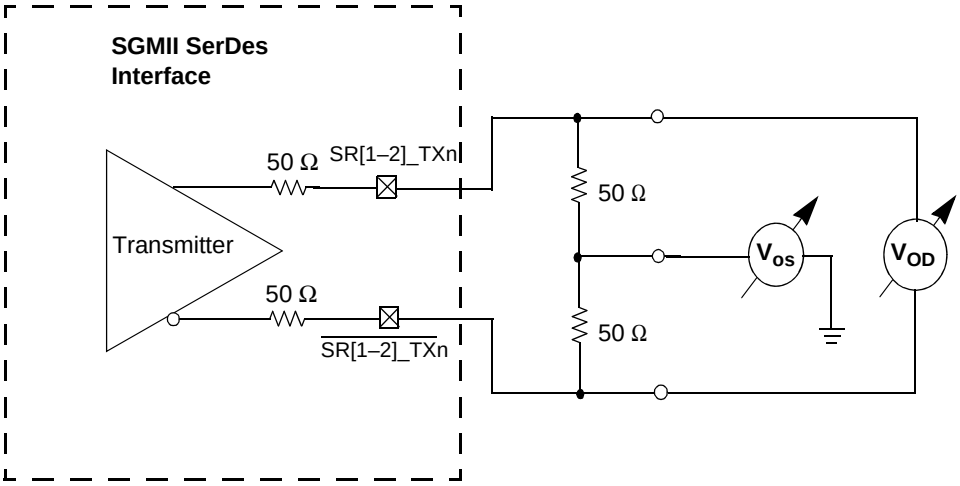

Figure 10. SGMII Transmitter DC Measurement Circuit

Table 16 describes the SGMII SerDes receiver AC-coupled DC electrical characteristics.

Table 16. SGMII DC Receiver Electrical Characteristics[5]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC Input voltage range		—		N/A		—	1
Input differential voltage	SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2	$V_{RX\_DIFFp\text{-}p}$	100	—	1200	mV	2, 4
	SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2		175	—			
Loss of signal threshold	SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2	VLOS	30	—	100	mV	3, 4
	SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	W	—

Notes:
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in the PCI Express interface. Refer to the PCI Express Differential Receiver (RX) Input Specifications section of the *PCI Express Specification* document. for details.
4. The values for SGMII1 and SGMII2 are selected in the SRDS control registers.
5. The supply voltage is 1.0 V.

2.6 AC Timing Characteristics

This section describes the AC timing characteristics for the MSC8154E.

2.6.1 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.6.1.1 DDR SDRAM Input AC Timing Specifications

Table 18 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.20	V
AC input high voltage	V_{IH}	MV_{REF} + 0.20	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.8 ± 5%.				

Table 19 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.5 V.

Table 19. DDR3 SDRAM Input AC Timing Specifications for 1.5 V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.175	V
AC input high voltage	V_{IH}	MV_{REF} + 0.175	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.5 ± 5%.				

Table 20 provides the input AC timing specifications for the DDR SDRAM interface.

Table 20. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}				1, 2
• 800 MHz data rate		–200	200	ps	
• 667 MHz data rate		–240	240	ps	
Tolerated Skew for MDQS—MDQ/MECC/MDM	t_{DISKEW}				2, 3
• 800 MHz data rate		–425	425	ps	
• 667 MHz data rate		–510	510	ps	

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.
2. At recommended operating conditions with V_{DDDDR} (1.8 V or 1.5 V) ± 5%
3. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

Figure 13 shows the DDR SDRAM output timing diagram.

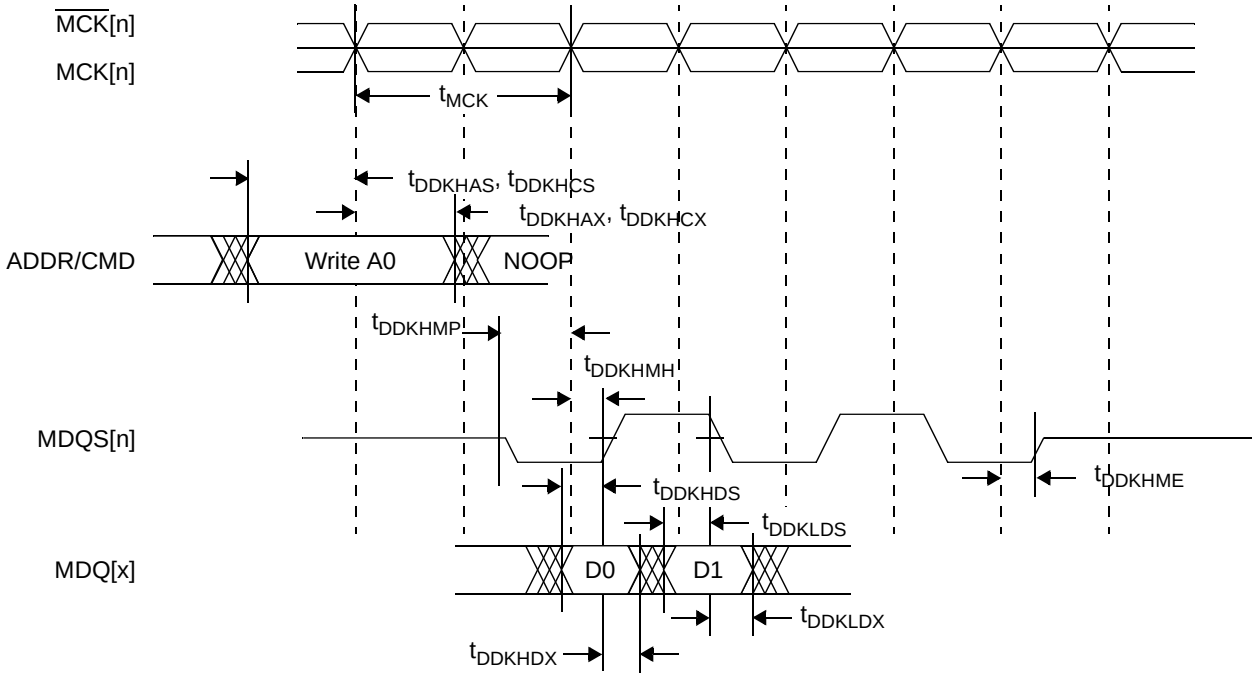

Figure 13. DDR SDRAM Output Timing

Figure 14 provides the AC test load for the DDR2 and DDR3 controller bus.

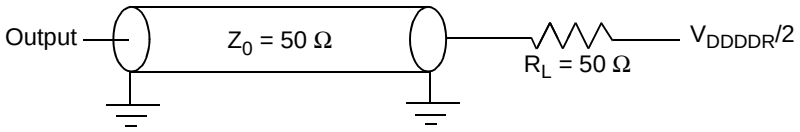

Figure 14. DDR2 and DDR3 Controller Bus AC Test Load

2.6.1.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR2 and DDR3 SDRAM controller interface. Figure 15 shows the differential timing specification.

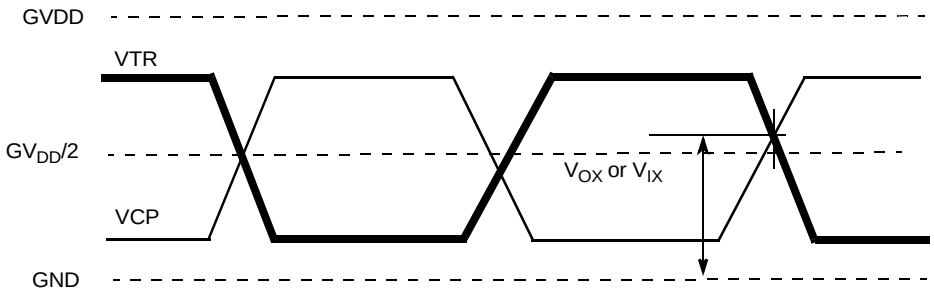

Figure 15. DDR2 and DDR3 SDRAM Differential Timing Specifications

Note: VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

Table 24. SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ Input Clock Requirements (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes

Notes:
1. Caution: Only 100 and 125 have been tested. Other values will not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 1.0a
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SR[1–2]_REF_CLK minus $\overline{\text{SR[1–2]\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 16.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SR[1–2]_REF_CLK and falling edge rate for $\overline{\text{SR[1–2]\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SR[1–2]_REF_CLK rising meets $\overline{\text{SR[1–2]\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SR[1–2]_REF_CLK should be compared to the fall edge rate of $\overline{\text{SR[1–2]\_REF\_CLK}}$; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 17.

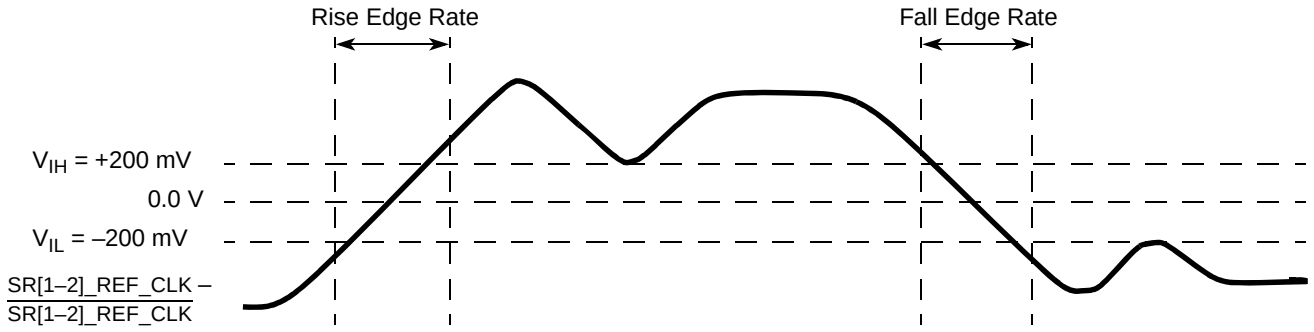

Figure 16. Differential Measurement Points for Rise and Fall Time

Figure 17. Single-Ended Measurement Points for Rise and Fall Time Matching

2.6.2.3 Serial RapidIO AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 27 defines the transmitter AC specifications for the Serial RapidIO interface. The AC timing specifications do not include REF_CLK jitter.

Table 27. Serial RapidIO Transmitter AC Timing Specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Deterministic Jitter	J_D	—	—	0.17	UI p-p
Total Jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps

Table 28 defines the Receiver AC specifications for the Serial RapidIO interface. The AC timing specifications do not include REF_CLK jitter.

Table 28. Serial RapidIO Receiver AC Timing Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	Notes
Deterministic Jitter Tolerance	J_D	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total Jitter Tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit Error Rate	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

Notes:
1. Measured at receiver.
2. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 18. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

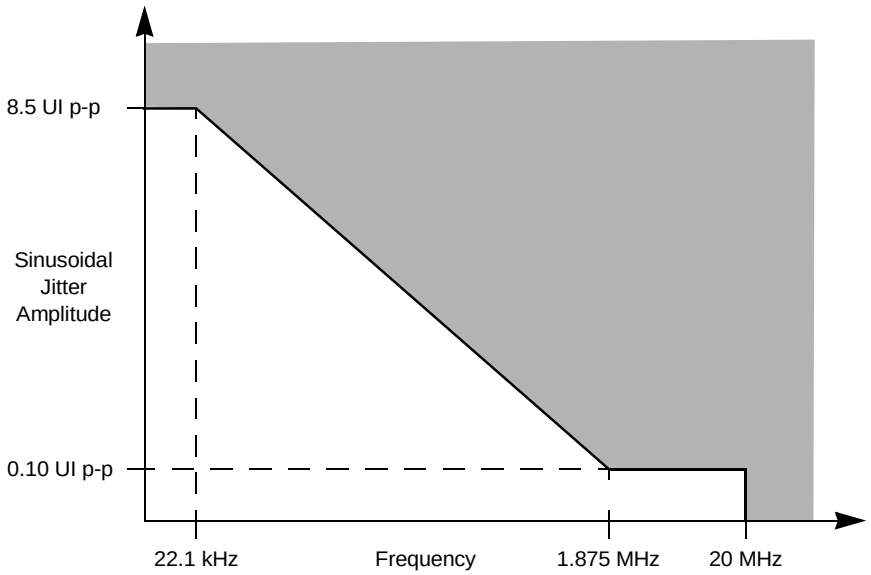

Figure 18. Single Frequency Sinusoidal Jitter Limits

2.6.3 TDM Timing

Table 31 provides the input and output AC timing specifications for the TDM interface.

Table 31. TDM AC Timing Specifications for 62.5 MHz[1]

Parameter	Symbol[2]	Min	Max	Unit
TDMxRCK/TDMxTCK	t_{DM}	16.0	—	ns
TDMxRCK/TDMxTCK high pulse width	t_{DM_HIGH}	7.0	—	ns
TDMxRCK/TDMxTCK low pulse width	t_{DM_LOW}	7.0	—	ns
TDM all input setup time	t_{DMIVKH}	3.6	—	ns
TDMxRD hold time	$t_{DMRDIXKH}$	1.9	—	ns
TDMxTFS/TDMxRFS input hold time	$t_{DMFSIXKH}$	1.9	—	ns
TDMxTCK High to TDMxTD output active	t_{DM_OUTAC}	2.5	—	ns
TDMxTCK High to TDMxTD output valid	$t_{DMTKHOV}$	—	9.8	ns
TDMxTD hold time	$t_{DMTKHOX}$	2.5	—	ns
TDMxTCK High to TDMxTD output high impedance	t_{DM_OUTHI}	—	9.8	ns
TDMxTFS/TDMxRFS output valid	$t_{DMFSKHOV}$	—	9.25	ns
TDMxTFS/TDMxRFS output hold time	$t_{DMFSKHOX}$	2.0	—	ns

Notes:
1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the output internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output values are based on 30 pF capacitive load.
3. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. T_{DMxTCK} and T_{DMxRCK} are shown using the rising edge.
4. All values are based on a maximum TDM interface frequency of 62.5 MHz.

Figure 20 shows the TDM receive signal timing.

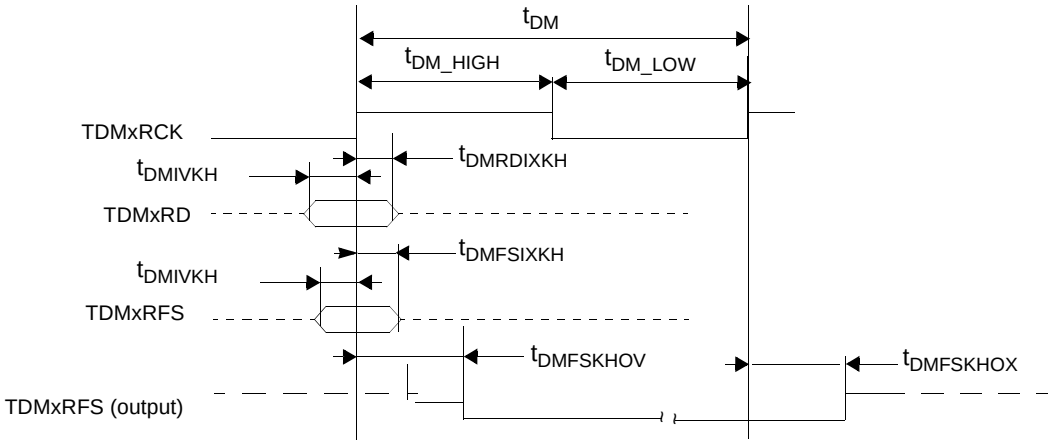

Figure 20. TDM Receive Signals

2.6.5 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are programmable delay units (PDU) that should be programmed differently for each interface to meet timing. There is a general configuration register 4 (GCR4) used to configure the timing. For additional information, see the *MSC8154E Reference Manual*.

2.6.5.1 Management Interface Timing

Table 33 lists the timer input Ethernet controller management interface timing specifications shown in Figure 24.

Table 33. Ethernet Controller Management Interface Timing

Characteristics	Symbol	Min	Max	Unit
GE_MDC frequency	f_{MDC}	—	2.5	MHz
GE_MDC period	t_{MDC}	400	—	ns
GE_MDC clock pulse width high	t_{MDC_H}	160	—	ns
GE_MDC clock pulse width low	t_{MDC_L}	160	—	ns
GE_MDC to GE_MDIO delay[2]	t_{MDKHDX}	10	70	ns
GE_MDIO to GE_MDC rising edge setup time	t_{MDDVKH}	20	—	ns
GE_MDC rising edge to GE_MDIO hold time	t_{MDDXKH}	0	—	ns

Notes:
1. Program the GE_MDC frequency (f_{MDC}) to a maximum value of 2.5 MHz (400 ns period for t_{MDC}). The value depends on the source clock and configuration of MIIMCFG[MCS] and UPSMR[MDCP]. For example, for a source clock of 400 MHz to achieve f_{MDC} = 2.5 MHz, program MIIMCFG[MCS] = 0x4 and UPSMR[MDCP] = 0. See the *MSC8154E Reference Manual* for configuration details.
2. The value depends on the source clock. For example, for a source clock of 267 MHz, the delay is 70 ns. For a source clock of 333 MHz, the delay is 58 ns.

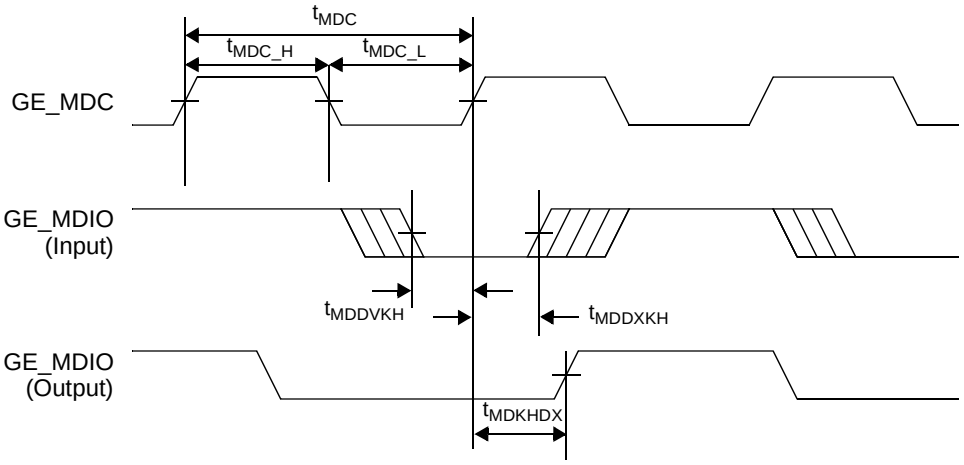

Figure 24. MII Management Interface Timing

2.6.5.2 RGMII AC Timing Specifications

Table 34 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 34. RGMII at 1 Gbps[2] with On-Board Delay[3] AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)[4]	t_{SKEWT}	–-0.5	—	0.5	ns
Data to clock input skew (at receiver) [4]	t_{SKEWR}	1	—	2.6	ns

Notes:
1. At recommended operating conditions with V_{DDIO} of 2.5 V ± 5%.
2. RGMII at 100 Mbps support is guaranteed by design.
3. Program GCR4 as 0x00000000.
4. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.

Table 35 presents the RGMII AC timing specification for applications required non-delayed clock on board.

Table 35. RGMII at 1 Gbps[2] with No On-Board Delay[3] AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)[4]	t_{SKEWT}	–2.6	—	–1.0	ns
Data to clock input skew (at receiver)[4]	t_{SKEWR}	–0.5	—	0.5	ns

Notes:
1. At recommended operating conditions with V_{DDIO} of 2.5 V ± 5%.
2. RGMII at 100 Mbps support is guaranteed by design.
3. GCR4 should be programmed as 0x000CC330.
4. This implies that PC board design requires clocks to be routed with no additional trace delay

Figure 25 shows the RGMII AC timing and multiplexing diagrams.

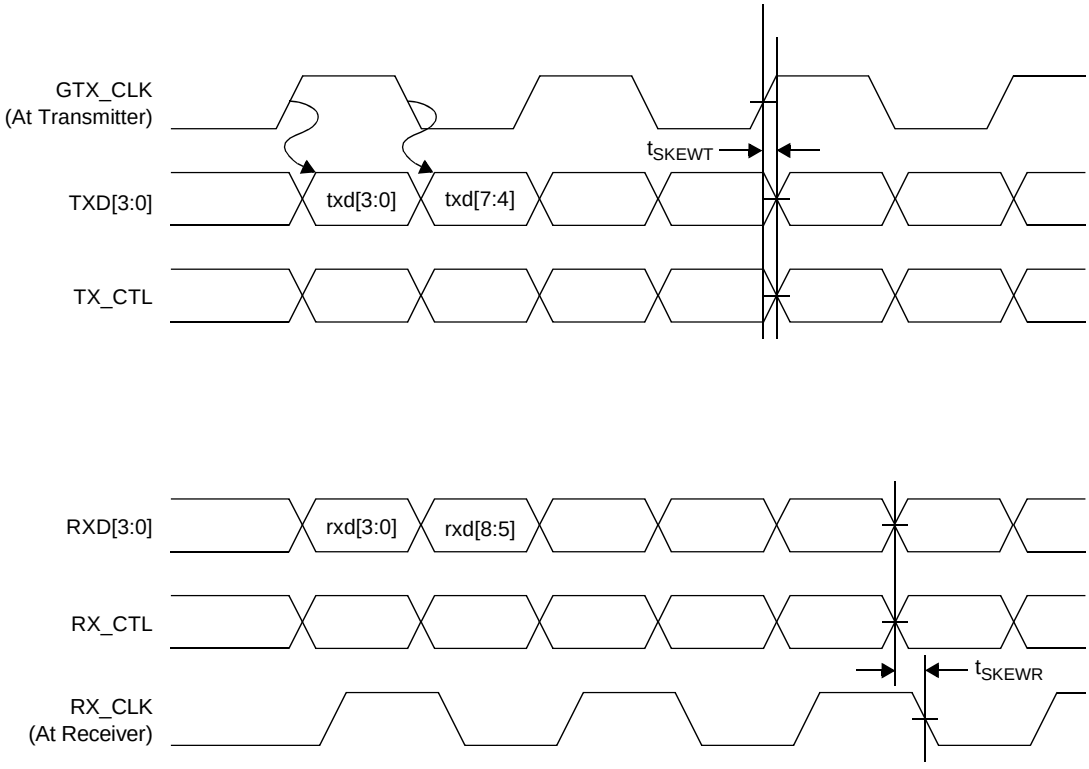

Figure 25. RGMII AC Timing and Multiplexing

2. After the above rails rise to 90% of their nominal voltage, the following I/O power rails may rise in any sequence (see Figure 34): QVDD, NVDD, GVDD1, and GVDD2.

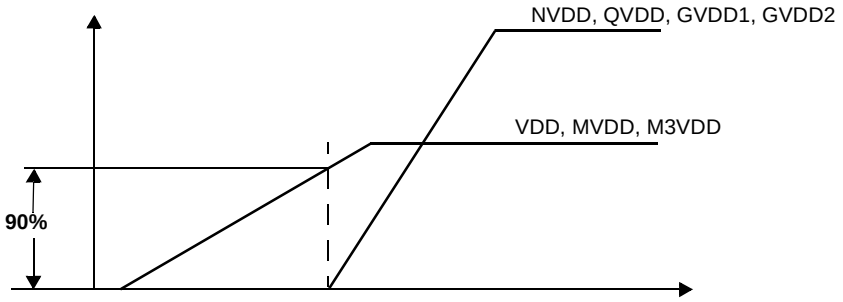

Figure 34. Supply Ramp-Up Sequence

Notes: **1.** If the M3 memory is not used, M3VDD can be tied to GND.
2. If the MAPLE-B is not used, MVDD can be tied to GND.
3. If the HSSI port1 is not used, SXCVDD1and SXPVDD1 must be connected to the designated power supplies.
4. If the HSSI port2 is not used, SXCVDD2 and SXPVDD2 must be connected to the designated power supplies.
5. If the DDR port 1 interface is not used, it is recommended that GVDD1 be left unconnected.
6. If the DDR port 2 interface is not used, it is recommended that GVDD2 be left unconnected.

3.1.4 Reset Guidelines

When a debugger is not used, implement the connection scheme shown in Figure 35.

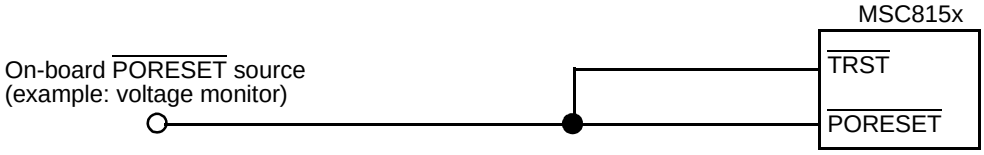

Figure 35. Reset Connection in Functional Application

When a debugger is used, implement the connection scheme shown in Figure 36.

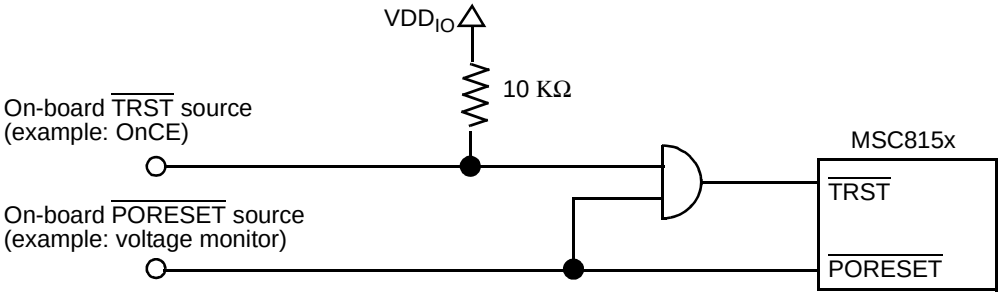

Figure 36. Reset Connection in Debugger Application

3.2 PLL Power Supply Design Considerations

Each global PLL power supply must have an external RC filter for the PLLn_AVDD input (see Figure 37) in which the following components are defined as listed:

- R = 5 Ω ± 5%
- C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.
- C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.

Note: A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change.

All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately. For optimal noise filtering, place the circuit as close as possible to its PLLn_AVDD inputs.

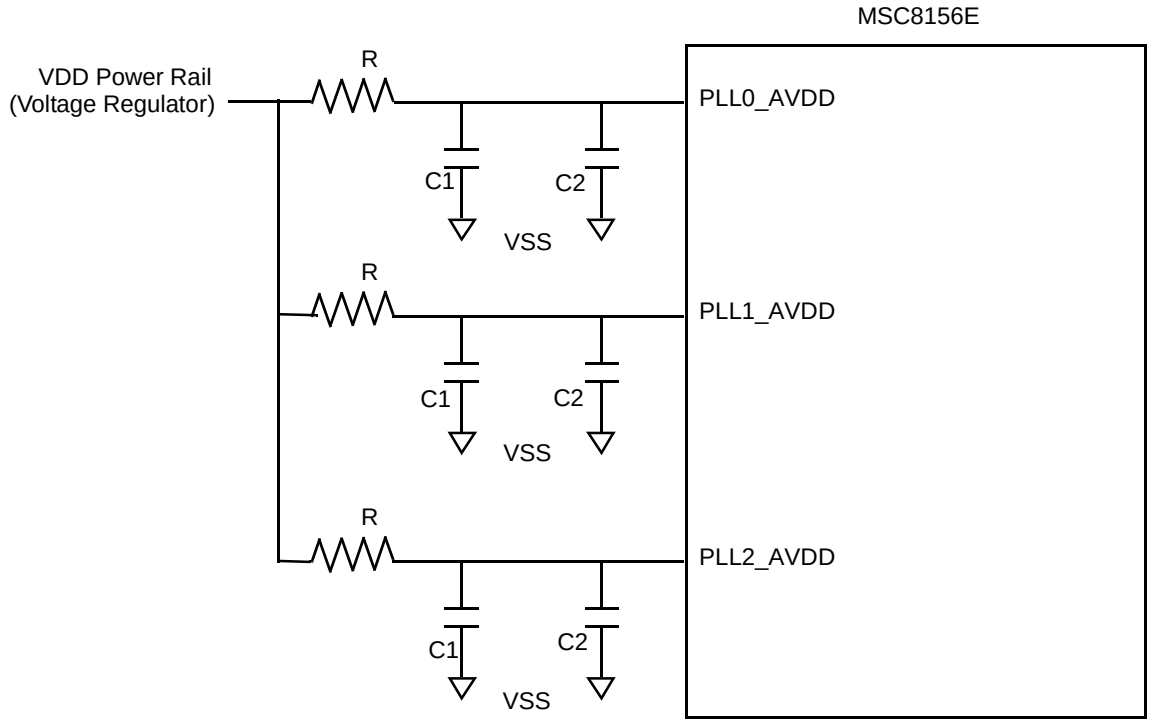

Figure 37. PLL Supplies

Each SerDes PLL power supply must be filtered using a circuit similar to the one shown in Figure 38, to ensure stability of the internal clock. For maximum effectiveness, the filter circuit should be placed as closely as possible to the SRn_PLL_AVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the SRn_PLL_AVDD ball. The 0.003 µF capacitor is closest to the ball, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from SRn_PLL_AVDD to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All trances should be kept short, wide, and direct.

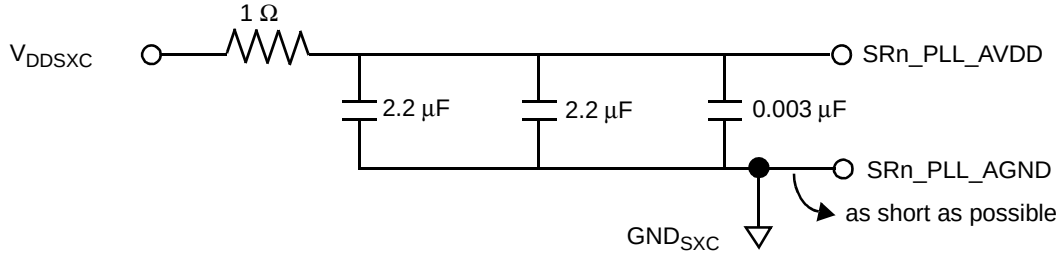

Figure 38. SerDes PLL Supplies

Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDM***n***TCLK	GND
TDMT***n***DAT	GND
TDM***n***TSYN	GND
V_{DDIO}	2.5 V

Notes: **1.** ***n*** = {0, 1, 2,3}
2. In case of subset of TDM interface usage please make sure to disable unused TDM modules. See *TDM* chapter in the ***MSC8154E Reference Manual*** for details.

3.5.5 Miscellaneous Pins

Table 49 lists the board connections for the pins not required by the system design. Table 49 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 49. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[31–0]	NC
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT\_OUT}}$	NC
$\overline{\text{IRQ}}$[15–0]	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$	NC
RC[21–0]	GND
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[4–0]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	See **Section 3.1** for guidelines.
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
DDN[1–0]	See the GPIO connectivity guidelines in this table.
DRQ[1–0]	See the GPIO connectivity guidelines in this table.
$\overline{\text{RCW\_LSEL\_0}}$	GND
$\overline{\text{RCW\_LSEL\_1}}$	GND
$\overline{\text{RCW\_LSEL\_2}}$	GND
$\overline{\text{RCW\_LSEL\_3}}$	GND
V_{DDIO}	2.5 V

Note: For details on configuration, see the *MSC8154E Reference Manual*. For additional information, refer to the *MSC815x and MSC825x DSP Family Design Checklist*.

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