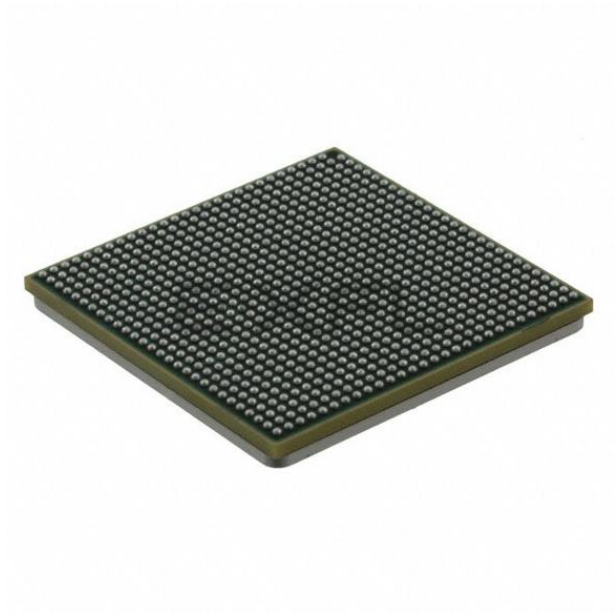

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Quad Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc8154etvt1000b

Table of Contents

List of Figures

1 Pin Assignment

This section includes diagrams of the MSC8154E package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in Figure 3 with the ball location index numbers.

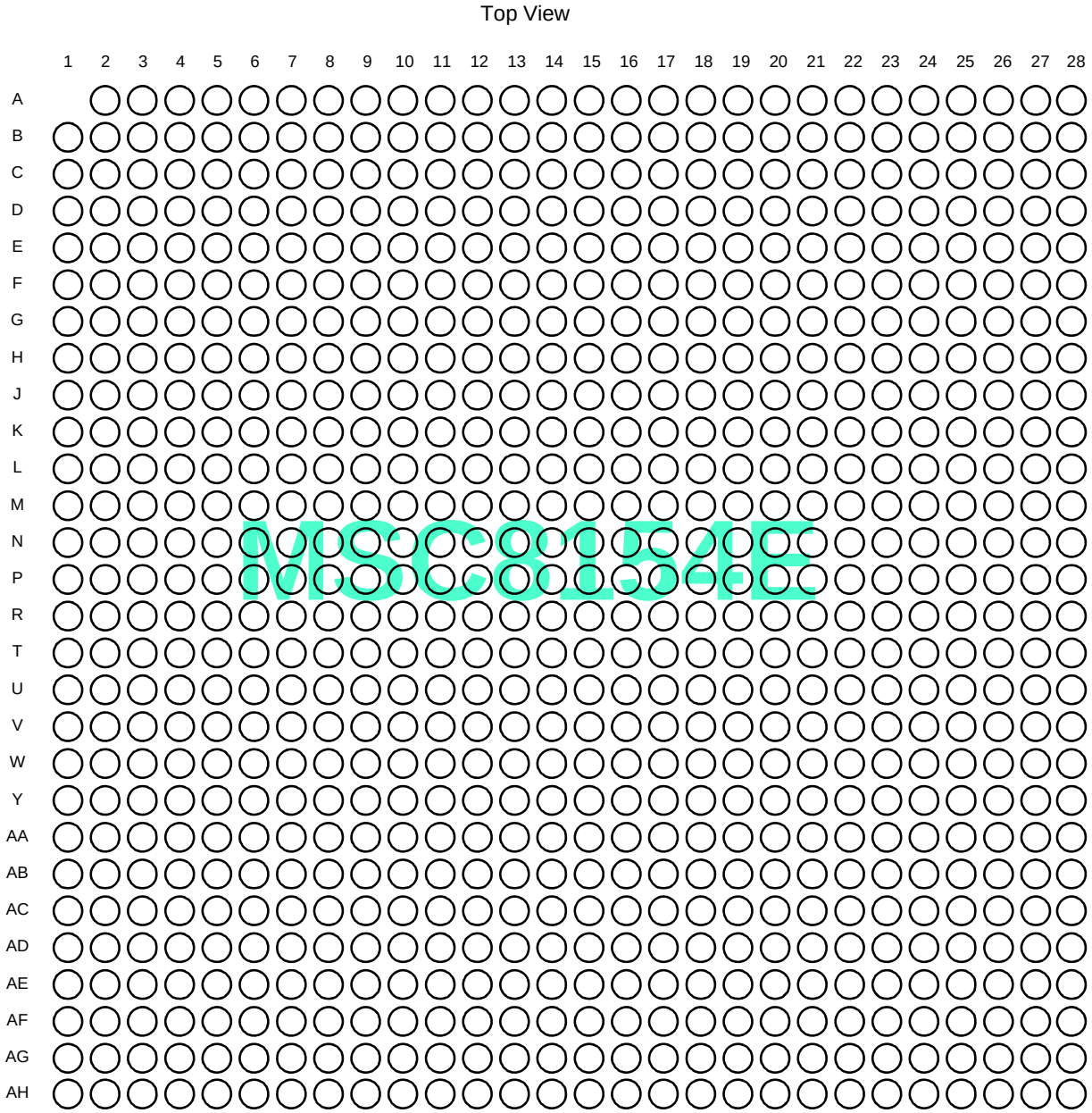


Figure 3. MSC8154E FC-PBGA Package, Top View

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N24	$\overline{\text{SR2\_TXD2}}$/$\overline{\text{PE\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	$\overline{\text{SR2\_RXD2}}$/$\overline{\text{PE\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD2
N28	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD[9]	Power	VDD
P9	PLL2_AVDD[9]	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	MVDD	Power	N/A
P16	VSS	Ground	N/A
P17	MVDD	Power	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND[9]	Ground	SXCVSS2
P26	SR2_PLL_AVDD[9]	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	$\overline{\text{NMI}}$	I	QVDD
R3	$\overline{\text{NMI\_OUT}}$[6]	O	QVDD
R4	$\overline{\text{HRESET}}$[6,7]	I/O	QVDD
R5	$\overline{\text{INT\_OUT}}$[6]	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD[9]	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
V21	$\overline{\text{RCW\_LSEL\_3}}$/RC20	I/O	NVDD
V22	$\overline{\text{RCW\_LSEL\_2}}$/RC19	I/O	NVDD
V23	SXPVDD2	Power	N/A
V24	SXPVSS2	Ground	N/A
V25	$\overline{\text{RCW\_LSEL\_1}}$/RC18	I/O	NVDD
V26	RC21	I	NVDD
V27	SXCVDD2	Power	N/A
V28	SXCVSS2	Ground	N/A
W1	VSS	Ground	N/A
W2	GVDD1	Power	N/A
W3	M1DM1	O	GVDD1
W4	VSS	Ground	N/A
W5	GVDD1	Power	N/A
W6	M1DQ0	I/O	GVDD1
W7	VSS	Ground	N/A
W8	GVDD1	Power	N/A
W9	M1DQ5	I/O	GVDD1
W10	VDD	Power	N/A
W11	VSS	Ground	N/A
W12	VDD	Power	N/A
W13	VSS	Ground	N/A
W14	VDD	Power	N/A
W15	VSS	Ground	N/A
W16	VDD	Power	N/A
W17	VSS	Ground	N/A
W18	VDD	Power	N/A
W19	VSS	Ground	N/A
W20	VSS	Ground	N/A
W21	$\overline{\text{RCW\_LSEL0}}$/RC17	I/O	NVDD
W22	GPIO19/SPI_MISO[5,8]	I/O	NVDD
W23	VSS	Ground	N/A
W24	NVDD	Power	N/A
W25	GPIO11/$\overline{\text{IRQ11}}$/RC11[5,8]	I/O	NVDD
W26	GPIO3/DRQ1/$\overline{\text{IRQ3}}$/RC3[5,8]	I/O	NVDD
W27	GPIO7/$\overline{\text{IRQ7}}$/RC7[5,8]	I/O	NVDD
W28	GPIO2/$\overline{\text{IRQ2}}$/RC2[5,8]	I/O	NVDD
Y1	M1DQS1	I/O	GVDD1
Y2	$\overline{\text{M1DQS1}}$	I/O	GVDD1
Y3	M1DQ10	I/O	GVDD1
Y4	M1DQ11	I/O	GVDD1
Y5	M1DQ14	I/O	GVDD1
Y6	M1DQ23	I/O	GVDD1
Y7	M1ODT0	O	GVDD1
Y8	M1A12	O	GVDD1
Y9	M1A14	O	GVDD1
Y10	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AH17	$\overline{\text{M1DQS6}}$	I/O	GVDD1
AH18	M1DQS6	I/O	GVDD1
AH19	M1DQ48	I/O	GVDD1
AH20	M1DQ49	I/O	GVDD1
AH21	VSS	Ground	N/A
AH22	TDM0RCK/GE2_RD2[3]	I/O	NVDD
AH23	TDM0RDT/GE2_RD3[3]	I/O	NVDD
AH24	TDM0TSN/GE2_RD0[3]	I/O	NVDD
AH25	TDM1RCK/GE2_RD1[3]	I/O	NVDD
AH26	TDM3TDT/GE1_RD3[3]	I/O	NVDD
AH27	TDM3TCK/GE1_RD2[3]	I	NVDD
AH28	VSS	Ground	N/A

Notes:
1. Reserved signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS), or pulled up (VDD).
2. Signal function during power-on reset is determined by the RCW source type.
3. Selection of TDM versus RGMII functionality is determined by the RCW bit values.
4. Selection of RapidIO, SGMII, and PCI Express functionality is determined by the RCW bit values.
5. Selection of the GPIO function and other functions is done by GPIO register setup. For configuration details, see the *GPIO* chapter in the *MSC8154E Reference Manual*.
6. Open-drain signal.
7. Internal 20 KΩ pull-up resistor.
8. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See the *GPIO* chapter of the *MSC8154E Reference Manual* for configuration details.
9. Connect to power supply via external filter. See **Section 3.2**, *PLL Power Supply Design Considerations* for details.
10. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected.

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8154E Reference Manual*.

2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8154E.

Table 2. Absolute Maximum Ratings

Rating	Power Rail Name	Symbol	Value	Unit
Core supply voltage • Cores 0–3	VDD	V_{DD}	–0.3 to 1.1	V
PLL supply voltage[3]		V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	–0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1	V V V
M3 memory supply voltage	M3VDD	V_{DDM3}	–0.3 to 1.1	V
MAPLE-B supply voltage	MVDD	V_{DDM}	–0.3 to 1.1	V
DDR memory supply voltage • DDR2 mode • DDR3 mode	GVDD1, GVDD2	V_{DDDDR}	 –0.3 to 1.98 –0.3 to 1.65	 V V
DDR reference voltage	MVREF	MV_{REF}	–0.3 to 0.51 × V_{DDDDR}	V
Input DDR voltage		V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
I/O voltage excluding DDR and RapidIO lines	NVDD, QVDD	V_{DDIO}	–0.3 to 2.625	V
Input I/O voltage		V_{INIO}	–0.3 to V_{DDIO} + 0.3	V
RapidIO pad voltage	SXPVDD1, SXPVDD2	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O core voltage	SXCVDD1, SXCVDD2	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O PLL voltage[3]		$V_{DDRIOPLL}$	–0.3 to 1.21	V
Input RapidIO I/O voltage		V_{INRIO}	–0.3 to V_{DDSXC} + 0.3	V
Operating temperature		T_J	–40 to 105	°C
Storage temperature range		T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 3.
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8154E (see Figure 37 and Figure 38)

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8154E.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8154E.

Note: DDR2 SDRAM uses V_{DDDDR}(typ) = 1.8 V and DDR3 SDRAM uses V_{DDDDR}(typ) = 1.5 V.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR2 SDRAM.

Note: At recommended operating conditions (see Table 3) with V_{DDDDR} = 1.8 V.

Table 6. DDR2 SDRAM Interface DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V	2, 3, 4
Input high voltage	V_{IH}	MV_{REF} + 0.125	V_{DDDDR} + 0.3	V	5
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	5
I/O leakage current	I_{OZ}	–50	50	µA	6
Output high current (V_{OUT} (VOH) = 1.37 V)	I_{OH}	–13.4	—	mA	7
Output low current (V_{OUT} (VOL) = 0.33 V)	I_{OL}	13.4	—	mA	7

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} supply voltage at all times. The DRAM and memory controller can use the same or different sources.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$ and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} with a minimum value of MV_{REF} – 0.4 and a maximum value of MV_{REF} + 0.04 V. V_{TT} should track variations in the DC-level of MV_{REF}.
4. The voltage regulator for MV_{REF} must be able to supply up to 300 µA.
5. Input capacitance load for DQ, DQS, and DQS signals are available in the IBIS models.
6. Output leakage is measured with all outputs are disabled, $0 V \le V_{OUT} \le V_{DDDDR}$.
7. Refer to the IBIS model for the complete output IV curve characteristics.

2.5.1.4 DDR Reference Current Draw

Table 9 lists the current draw characteristics for MV_{REF}.

Note: Values when used at recommended operating conditions (see Table 3).

Table 9. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV_{REFn} • DDR2 SDRAM • DDR3 SDRAM	I_{MVREFn}	—	 300 250	 µA µA

2.5.2 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The MSC8154E features an HSSI that includes two 4-channel SerDes ports used for high-speed serial interface applications (PCI Express, Serial RapidIO interfaces, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 2.6.2, "HSSI AC Timing Specifications."

2.5.2.1 Signal Term Definitions

The SerDes interface uses differential signalling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 4 shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 4 shows the waveform for either a transmitter output (SR[1–2]_TX and $\overline{\text{SR[1–2]\_TX}}$) or a receiver input (SR[1–2]_RX and $\overline{\text{SR[1–2]\_RX}}$). Each signal swings between A volts and B volts where A > B.

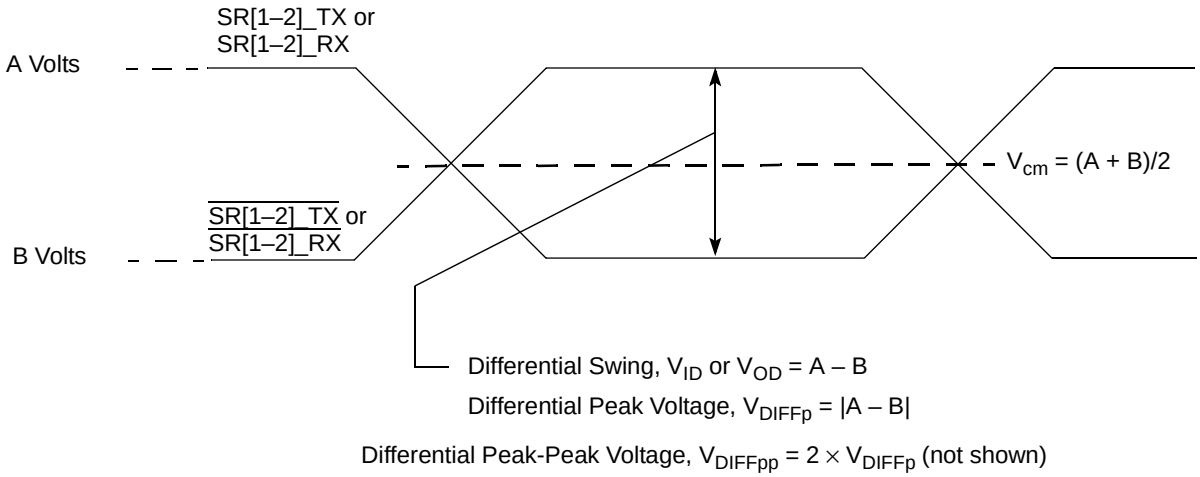
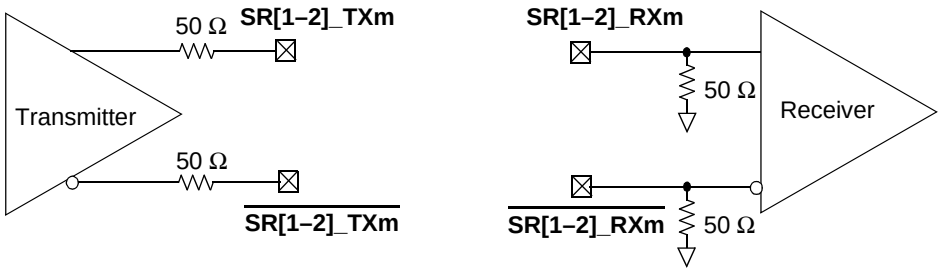


Figure 4. Differential Voltage Definitions for Transmitter or Receiver

2.5.2.3 SerDes Transmitter and Receiver Reference Circuits

Figure 6 shows the reference circuits for SerDes data lane transmitter and receiver.



Note: The [1–2] indicates the specific SerDes Interface (1 or 2) and the m indicates the specific channel within that interface (0,1,2,3). Actual signals are assigned by the HRCW assignments at reset (see **Chapter 5**, *Reset* in the reference manual for details)

Figure 6. SerDes Transmitter and Receiver Reference Circuits

2.5.3 DC-Level Requirements for SerDes Interfaces

The following subsections define the DC-level requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.5.3.1 DC-Level Requirements for SerDes Reference Clocks

The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 7 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

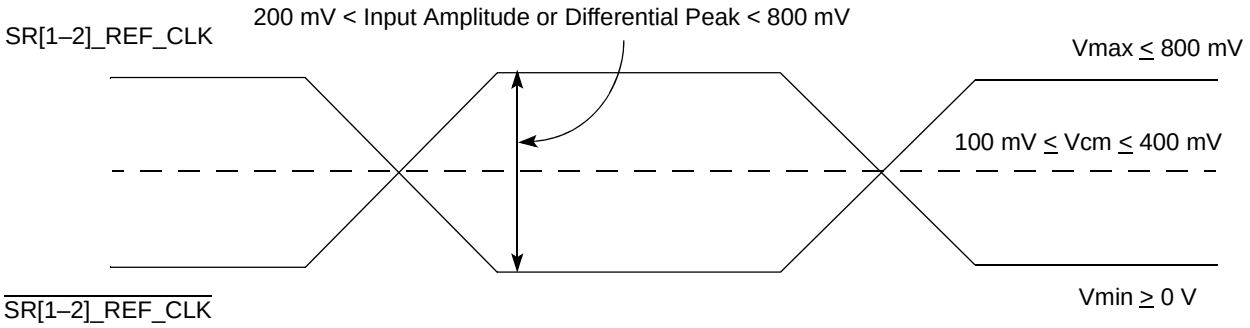


Figure 7. Differential Reference Clock Input DC Requirements (External DC-Coupled)

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC-level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to GND_{SXC}. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage GND_{SXC}. Figure 8 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

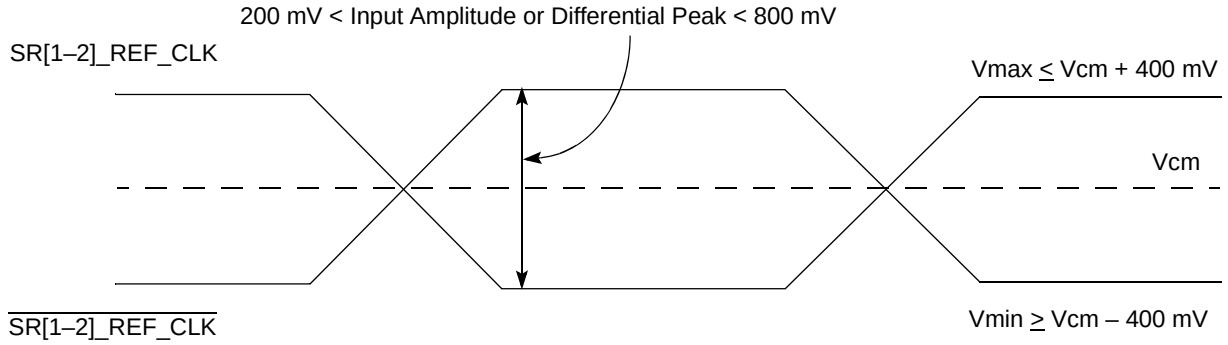


Figure 8. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  — The reference clock can also be single-ended. The SR[1–2]_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SR[1–2]\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SR[1–2]_REF_CLK input average voltage must be between 200 and 400 mV. Figure 9 shows the SerDes reference clock input requirement for single-ended signalling mode.
  — To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SR[1–2]\_REF\_CLK}}$) through the same source impedance as the clock input (SR[1–2]_REF_CLK) in use.

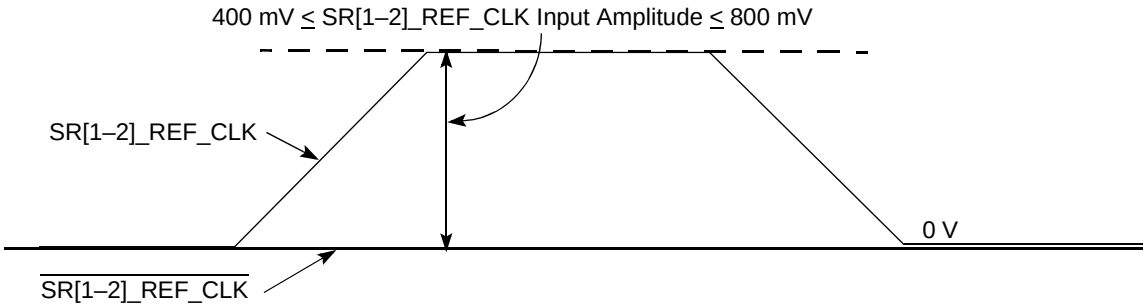


Figure 9. Single-Ended Reference Clock Input DC Requirements

2.5.3.2 DC-Level Requirements for PCI Express Configurations

The DC-level requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8154E supports a 2.5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 1.0a*. The transmitter specifications are defined in Table 11 and the receiver specifications are defined in Table 12.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 11. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	1
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	2
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	3
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	4

Notes:
1. $V_{TX-DIFFp-p} = 2 \times |V_{TX-D+} - V_{TX-D-}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.
3. Tx DC differential mode low impedance
4. Required Tx D+ as well as D– DC Impedance during all states

Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	1
DC differential Input Impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	3
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	KΩ	4
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	5

Notes:
1. $V_{RX-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D-}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D-}|$. Measured at the package pins of the receiver

2.5.3.3 DC-Level Requirements for Serial RapidIO Configurations

This sections provided various DC-level requirements for Serial RapidIO Configurations.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 13. Serial RapidIO Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Long run differential output voltage	V_{DIFFPP}	800	—	1600	mVp-p	—
Short run differential output voltage	V_{DIFFPP}	500	—	1000	mVp-p	—

Note: Voltage relative to COMMON of either signal comprising a differential pair.

Table 14. Serial RapidIO Receiver DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{IN}	200	—	1600	mVp-p	1

Notes: **1.** Measured at receiver.

2.5.3.4 DC-Level Requirements for SGMII Configurations

Note: Specifications are valid at the recommended operating conditions listed in Table 3

Table 15 describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SR[1–2]_TX[n] and $\overline{\text{SR[1–2]\_TX[n]}}$) as shown in Figure 10.

Table 15. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	$XV_{DD\_SRDS\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\_SRDS\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output differential voltage ($XV_{DD\text{-}Typ}$ at 1.0 V)	$\lvert V_{OD}\rvert$	323	500	725	mV	2,3,4
		296	459	665		2,3,5
		269	417	604		2,3,6
		243	376	545		2,3,7
		215	333	483		2,3,8
		189	292	424		2,3,9
		162	250	362		2,3,10
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Notes:
1. This does not align to DC-coupled SGMII. $XV_{DD\_SRDS2\text{-}Typ}$ = 1.1 V.
2. The $\lvert V_{OD}\rvert$ value shown in the table assumes full multitude by setting srd_smit_lvl as 000 and the following transmit equalization setting in the XMITEQ**AB** (for lanes A and B) or XMITEQ**EF** (for lanes E and F) bit field of Control Register:
• The MSB (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude which is power up default);
• The LSB (bit [1–3]) of the above bit field is set based on the equalization settings listed in notes 4 through 10.
3. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0 V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between
4. Equalization setting: 1.0x: 0000.
5. Equalization setting: 1.09x: 1000.
6. Equalization setting: 1.2x: 0100.
7. Equalization setting: 1.33x: 1100.
8. Equalization setting: 1.5x: 0010.
9. Equalization setting: 1.71x: 1010.
10. Equalization setting: 2.0x: 0110.
11. $\lvert V_{OD}\rvert = \lvert V_{SR[1–2]\_TXn} - V_{\overline{SR[1–2]\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.

Figure 11 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

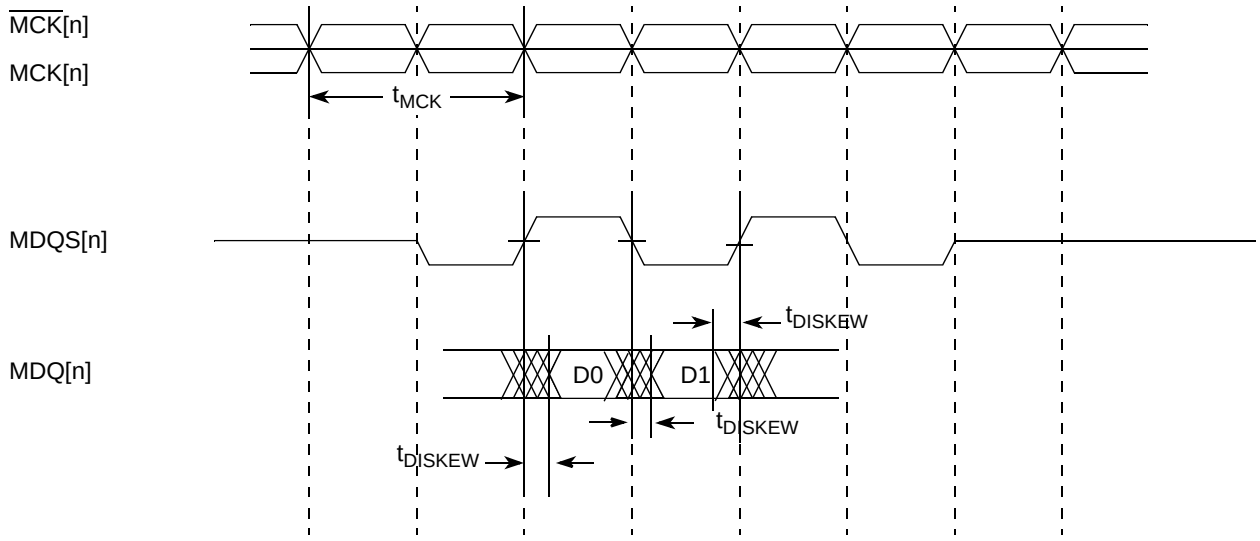


Figure 11. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

2.6.1.2 DDR SDRAM Output AC Timing Specifications

Table 21 provides the output AC timing specifications for the DDR SDRAM interface.

Table 21. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHAS}	 0.917 1.10	 — —	 ns ns	3
ADDR/CMD output hold with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHAX}	 0.767 1.02	 — —	 ns ns	3
$\overline{\text{MCS}}$n output setup with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHCS}	 0.917 1.10	 — —	 ns ns	3
$\overline{\text{MCS}}$n output hold with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHCX}	 0.767 1.02	 — —	 ns ns	3
MCK to MDQS Skew • 800 MHz data rate • 667 MHz data rate	t_{DDKHMH}	 –0.4 –0.6	 0.375 0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS • 800 MHz • 667 MHz	t_{DDKHDS}, t_{DDKLDS}	 300 375	 — —	 ps ps	5
MDQ/MECC/MDM output hold with respect to MDQS • 800 MHz • 667 MHz	t_{DDKHDX}, t_{DDKLDX}	 300 375	 — —	 ps ps	5
MDQS preamble	t_{DDKHMP}	$-0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$-0.4 \times t_{MCK}$	$-0.6 \times t_{MCK}$	ns	—

Table 22 provides the DDR2 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 22. DDR2 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input AC differential cross-point voltage	V_{IXAC}	0.5 × GVDD – 0.175	0.5 × GVDD + 0.175	V
Output AC differential cross-point voltage	V_{OXAC}	0.5 × GVDD – 0.125	0.5 × GVDD + 0.125	V

Table 23 provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 23. DDR3 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input AC differential cross-point voltage	V_{IXAC}	0.5 × GVDD – 0.150	0.5 × GVDD + 0.150	V
Output AC differential cross-point voltage	V_{OXAC}	0.5 × GVDD – 0.115	0.5 × GVDD + 0.115	V

2.6.2 HSSI AC Timing Specifications

The following subsections define the AC timing requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.6.2.1 AC Requirements for SerDes Reference Clock

Table 24 lists AC requirements for the SerDes reference clocks.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 24. SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ Input Clock Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at ref_clk input)	t_{CLK_TJ}	—	—	86	ps	2
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SR[1–2]_REF_CLK) to falling edge rate (SR[1–2]_REF_CLK) matching	Rise-Fall Matching	—	—	20	%	5, 6

2.6.2.2 PCI Express AC Physical Layer Specifications

The AC requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8154E supports a 2.5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 1.0a*. The transmitter specifications are defined in Table 25 and the receiver specifications are defined in Table 26. The parameters are specified at the component pins. the AC timing specifications do not include REF_CLK jitter.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 25. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit interval	UI	399.88	400.00	400.12	ps	1
Minimum Tx eye width	T_{TX-EYE}	0.70	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median.	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.15	UI	3, 4
AC coupling capacitor	C_{TX}	75	—	200	nF	5

Notes:
1. Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. No test load is necessarily associated with this value.
2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 – T_{TX-EYE} = 0.3$ UI.
3. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 8 and measured over any 250 consecutive Tx UIs. A $T_{TX-EYE} = 0.70$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.30$ UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data.
4. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.
5. All transmitters shall be AC-coupled. The AC coupling is required either within the media or within the transmitting component itself. The SerDes transmitter does not have built-in Tx capacitance. An external AC coupling capacitor is required.

Table 26. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	1
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	2, 3, 4
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	3, 4, 5

Notes:
1. Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. No test load is necessarily associated with this value.
2. The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 – T_{RX-EYE} = 0.6$ UI.
3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 8 should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
4. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
5. Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.6.6 SPI Timing

Table 36 lists the SPI input and output AC timing specifications.

Table 36. SPI AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Note
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns	2
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns	2
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	12	ns	2
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns	2
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	12	—	ns	—
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns	—
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.

Figure 26 provides the AC test load for the SPI.

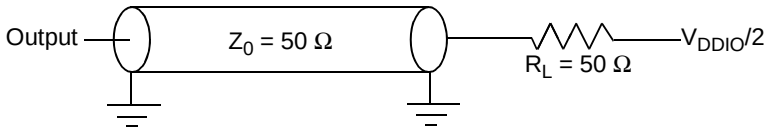
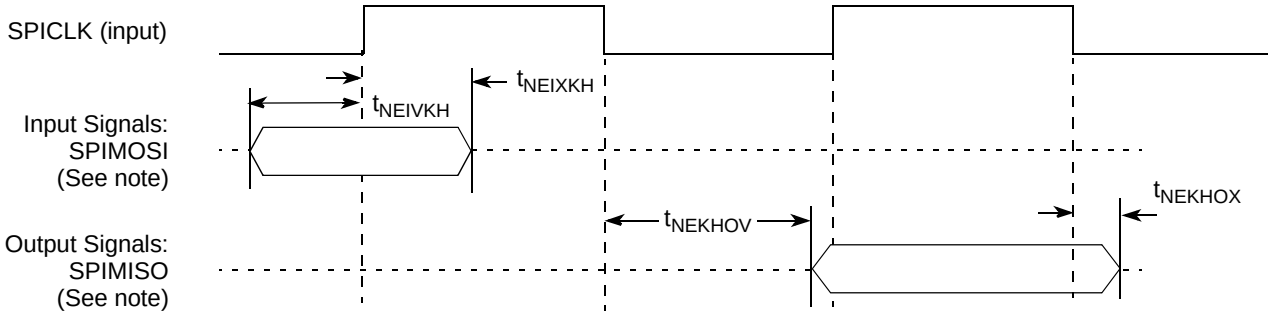


Figure 26. SPI AC Test Load

Figure 27 and Figure 28 represent the AC timings from Table 36. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 27 shows the SPI timings in slave mode (external clock).



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 27. SPI AC Timing in Slave Mode (External Clock)

Figure 28 shows the SPI timings in master mode (internal clock).

Figure 30 shows the boundary scan (JTAG) timing diagram.

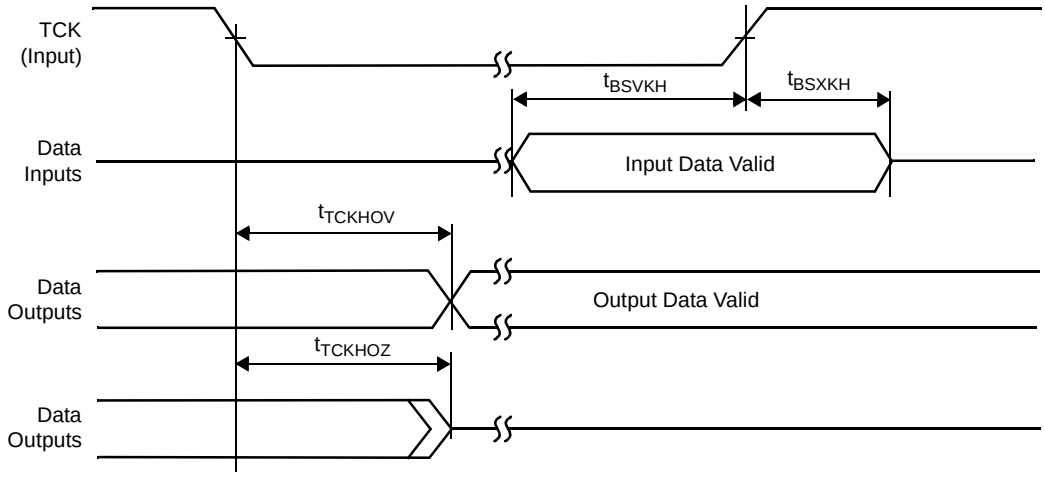


Figure 30. Boundary Scan (JTAG) Timing

Figure 31 shows the test access port timing diagram

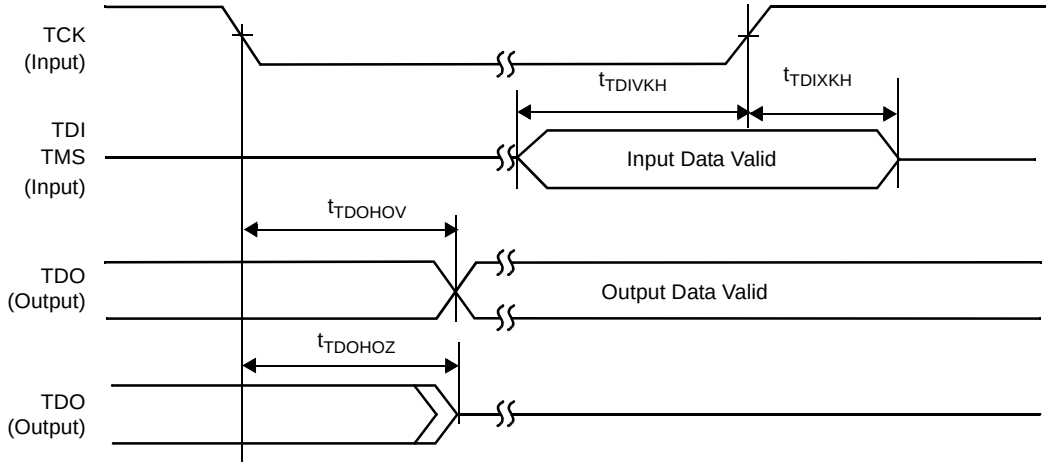


Figure 31. Test Access Port Timing

Figure 32 shows the $\overline{\text{TRST}}$ timing diagram.

Figure 32. $\overline{\text{TRST}}$ Timing

3.1.2 Power-On Ramp Time

This section describes the AC electrical specification for the power-on ramp rate requirements for all voltage supplies (including GVDD/SXPVDD/SXCVDD/QVDD/GVDD/NVDD, all VDD supplies, MVREF, and all AVDD supplies). Controlling the power-on ramp time is required to avoid falsely triggering the ESD circuitry. Table 39 defines the power supply ramp time specification.

Table 39. Power Supply Ramp Rate

Parameter	Min	Max	Unit
Required ramp rate.	—	36000	V/s

Notes:
1. Ramp time is specified as a linear ramp from 10% to 90% of nominal voltage of the specific voltage supply. If the ramp is non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical because this range might falsely trigger the ESD circuitry.
2. Required over the full recommended operating temperature range (see Table 3).
3. All supplies must be at their stable values within 50 ms.
4. The GVDD pins can be held low on the application board at powerup. If GVDD is not held low, then GVDD will rise to a voltage level that depends on the board-level impedance-to-ground. If the impedance is high (that is, infinite), then theoretically, GVDD can rise up close to the VDD levels.

3.1.3 Power Supply Guidelines

Use the following guidelines for power-up sequencing:

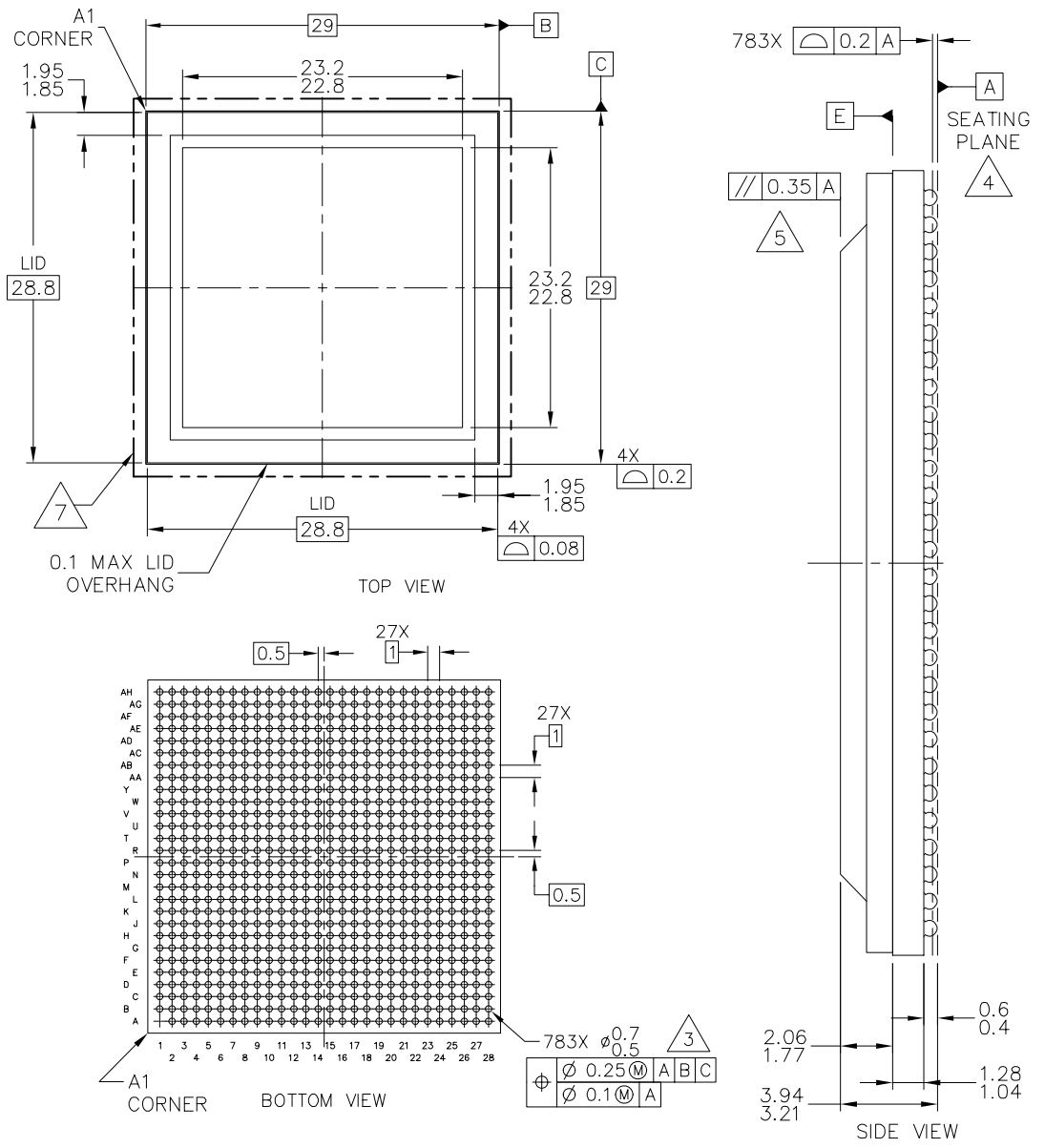
- Couple M3VDD with the VDD power rail using an extremely low impedance path.
- Couple inputs PLL1_AVDD, PLL2_AVDD and PLL3_AVDD with the VDD power rail using an RC filter (see Figure 37).
- There is no dependency in power-on/power-off sequence between the GVDD1, GVDD2, NVDD, and QVDD power rails.
- Couple inputs M1VREF and M2VREF with the GVDD1 and GVDD2 power rails, respectively. They should rise at the same time as or after their respective power rail.
- There is no dependency between RapidIO supplies: SXCVDD1, SXCVDD2, SXPVDD1 and SXPVDD2 and other MSC8154E supplies in the power-on/power-off sequence
- Couple inputs SR1_PLL_AVDD and SR2_PLL_AVDD with SXCVDD1 and SXCVDD2 power rails, respectively, using an RC filter (see Figure 38).

External voltage applied to any input line must not exceed the I/O supply voltage related to this line by more than 0.6 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule during start-up. However, each such input can draw up to 80 mA per input pin per MSC8154E device in the system during power-up. An assertion of the inputs to the high voltage level before power-up should be with slew rate less than 4 V/ns.

The device power rails should rise in the following sequence:

1. VDD (and all coupled supplies)

5 Package Information



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURE PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
7. 29.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y.

Figure 40. MSC8154E Mechanical Information, 783-ball FC-PBGA Package

6 Product Documentation

Following is a general list of supporting documentation:

- *MSC8154E Technical Data Sheet* (MSC8154E). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8154E device.
- *MSC8154E Reference Manual* (MSC8154ERM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8154E device.
- *QUICC Engine Block Reference Manual with Protocol Interworking* (QEIWRM). Provides detailed information regarding the QUICC Engine technology including functional description, registers, and programming information.
- *SC3850 DSP Core Reference Manual*. Covers the SC3850 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8156SC3850 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

7 Revision History

Table 50 provides a revision history for this data sheet.

Table 50. Document Revision History

Rev.	Date	Description
0	Dec. 2010	• Initial public release.
1	Mar 2011	• Updated Table 8. • Updated Table 15. • Updated Table 17. • Updated Table 33. • Updated Table 35. • Updated Table 39.
2	May 2011	• Updated Table 1. Changed the pin types for the following: – F25 from ground to power. – F26 from power to ground. – T6 from power to O.
3	Oct 2011	• Updated Table 34 and Table 35 to reflect 1 Gbps and 100 Mbps data rate instead of 1 GHz and 100 MHz.
4	Dec 2011	• Added note 4 to Table 39.