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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l073czt3

- **Stop mode without RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

  The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode. The LCD is not stopped automatically by entering Stop mode.

3.10 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, LPUART, general-purpose timers, DAC, and ADC.

3.11 Liquid crystal display (LCD)

The LCD drives up to 8 common terminals and 48 segment terminals to drive up to 384 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode
- V_{LCD} rails decoupling capability

3.12 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L073xx device. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference, V_{LCD} voltage measurement). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.

The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 µA at 10 kSPS, ~240 µA at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

Table 16. STM32L073xx pin definition (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100						
-	18	C2	27	E3	VSS	S	-	-	-	-
-	19	D2	28	H3	VDD	S	-	-	-	-
14	20	H3	29	M3	PA4	I/O	TC	(1)	SPI1_NSS, TSC_G2_IO1, USART2_CK, TIM22_ETR	COMP1_INM, COMP2_INM, ADC_IN4, DAC_OUT1
15	21	F4	30	K4	PA5	I/O	TC	-	SPI1_SCK, TIM2_ETR, TSC_G2_IO2, TIM2_CH1	COMP1_INM, COMP2_INM, ADC_IN5, DAC_OUT2
16	22	G4	31	L4	PA6	I/O	FT	-	SPI1_MISO, LCD_SEG3, TIM3_CH1, TSC_G2_IO3, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6
17	23	H4	32	M4	PA7	I/O	FT	-	SPI1_MOSI, LCD_SEG4, TIM3_CH2, TSC_G2_IO4, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	24	H5	33	K5	PC4	I/O	FT	-	EVENTOUT, LCD_SEG22, LPUART1_TX	ADC_IN14
-	25	H6	34	L5	PC5	I/O	FT	-	LCD_SEG23, LPUART1_RX, TSC_G3_IO1	ADC_IN15
18	26	F5	35	M5	PB0	I/O	FT	-	EVENTOUT, LCD_SEG5, TIM3_CH3, TSC_G3_IO2	LCD_VLCD3, ADC_IN8, VREF_OUT
19	27	G5	36	M6	PB1	I/O	FT	-	LCD_SEG6, TIM3_CH4, TSC_G3_IO3, LPUART1_RTS_DE	ADC_IN9, VREF_OUT
20	28	G6	37	L6	PB2	I/O	FT	-	LPTIM1_OUT, TSC_G3_IO4, I2C3_SMBA	LCD_VLCD1
-	-	-	38	M7	PE7	I/O	FT	-	LCD_SEG45, USART5_CK/USART5_RTS	-
-	-	-	39	L7	PE8	I/O	FT	-	LCD_SEG46, USART4_TX	-
-	-	-	40	M8	PE9	I/O	FT	-	TIM2_CH1, LCD_SEG47, TIM2_ETR, USART4_RX	-

Table 16. STM32L073xx pin definition (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100						
33	45	B8	71	A12	PA12	I/O	FT	(2)	SPI1_MOSI, EVENTOUT, TSC_G4_IO4, USART1_RTS_DE, COMP2_OUT	USB_DP
34	46	A8	72	A11	PA13	I/O	FT	-	SWDIO, USB_OE, LPUART1_RX	-
-	-	-	73	C11	VDD	S		-	-	-
35	47	D5	74	F11	VSS	S		-	-	-
36	48	E6	75	G11	VDD_USB	S		-	-	-
37	49	A7	76	A10	PA14	I/O	FT	-	SWCLK, USART2_TX, LPUART1_TX	-
38	50	A6	77	A9	PA15	I/O	FT	-	SPI1_NSS, LCD_SEG17, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1, USART4_RTS_DE	-
-	51	B7	78	B11	PC10	I/O	FT	-	LPUART1_TX, LCD_COM4/LCD_SEG28/ LCD_SEG48, USART4_TX	-
-	52	B6	79	C10	PC11	I/O	FT	-	LPUART1_RX, LCD_COM5/LCD_SEG29/ LCD_SEG49, USART4_RX	-
-	53	C5	80	B10	PC12	I/O	FT	-	LCD_COM6/LCD_SEG30/ LCD_SEG50, USART5_TX, USART4_CK	-
-	-	-	81	C9	PD0	I/O	FT	-	TIM21_CH1, SPI2_NSS/I2S2_WS	-
-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK/I2S2_CK	-
-	54	B5	83	C8	PD2	I/O	FT	-	LPUART1_RTS_DE, LCD_COM7/LCD_SEG31/ LCD_SEG51, TIM3_ETR, USART5_RX	-
-	-	-	84	B8	PD3	I/O	FT	-	USART2_CTS, LCD_SEG44, SPI2_MISO/I2S2_MCK	-

Table 17. Alternate functions port A

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/USART1/2/ LPUART1/USB/LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1/LCD/ TIM2/21	SPI1/SPI2/I2S2/LPUART1/ USART5/USB/LPTIM1/TIM2/3/EVENTOUT/ SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2/I2C2/USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/EVENTOUT	I2C3/LPUART1/COMP1/2/ TIM3
Port A	PA0	-	-	TIM2_CH1	TSC_G1_IO1	USART2_CTS	TIM2_ETR	USART4_TX	COMP1_OUT
	PA1	EVENTOUT	LCD_SEG0	TIM2_CH2	TSC_G1_IO2	USART2_RTS_DE	TIM21_ETR	USART4_RX	-
	PA2	TIM21_CH1	LCD_SEG1	TIM2_CH3	TSC_G1_IO3	USART2_TX	-	LPUART1_TX	COMP2_OUT
	PA3	TIM21_CH2	LCD_SEG2	TIM2_CH4	TSC_G1_IO4	USART2_RX	-	LPUART1_RX	-
	PA4	SPI1_NSS	-	-	TSC_G2_IO1	USART2_CK	TIM22_ETR	-	-
	PA5	SPI1_SCK	-	TIM2_ETR	TSC_G2_IO2		TIM2_CH1	-	-
	PA6	SPI1_MISO	LCD_SEG3	TIM3_CH1	TSC_G2_IO3	LPUART1_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI	LCD_SEG4	TIM3_CH2	TSC_G2_IO4	-	TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO	LCD_COM0	USB_CRS_SYNC	EVENTOUT	USART1_CK	-	-	I2C3_SCL
	PA9	MCO	LCD_COM1	-	TSC_G4_IO1	USART1_TX	-	I2C1_SCL	I2C3_SMBA
	PA10	-	LCD_COM2	-	TSC_G4_IO2	USART1_RX	-	I2C1_SDA	-
	PA11	SPI1_MISO	-	EVENTOUT	TSC_G4_IO3	USART1_CTS	-	-	COMP1_OUT
	PA12	SPI1_MOSI	-	EVENTOUT	TSC_G4_IO4	USART1_RTS_DE	-	-	COMP2_OUT
	PA13	SWDIO	-	USB_OE	-	-	-	LPUART1_RX	-
	PA14	SWCLK	-	-	-	USART2_TX	-	LPUART1_TX	-
	PA15	SPI1_NSS	LCD_SEG17	TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1	USART4_RTS_DE	-

Table 21. Alternate functions port E

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1 /LCD/TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/LPUART1/ COMP1/2/TIM3
Port E	PE0	-	LCD_SEG36	EVENTOUT	-	-	-	-	-
	PE1	-	LCD_SEG37	EVENTOUT	-	-	-	-	-
	PE2	-	LCD_SEG38	TIM3_ETR	-	-	-	-	-
	PE3	TIM22_CH1	LCD_SEG39	TIM3_CH1	-	-	-	-	-
	PE4	TIM22_CH2	-	TIM3_CH2	-	-	-	-	-
	PE5	TIM21_CH1	-	TIM3_CH3	-	-	-	-	-
	PE6	TIM21_CH2	-	TIM3_CH4	-	-	-	-	-
	PE7	-	LCD_SEG45	-	-	-	-	USART5_CK/U SART5_RTS_D E	-
	PE8	-	LCD_SEG46	-	-	-	-	USART4_TX	-
	PE9	TIM2_CH1	LCD_SEG47	TIM2_ETR	-	-	-	USART4_RX	-
	PE10	TIM2_CH2	LCD_SEG40	-	-	-	-	USART5_TX	-
	PE11	TIM2_CH3	-	-	-	-	-	USART5_RX	-
	PE12	TIM2_CH4	-	SPI1_NSS	-	-	-	-	-
	PE13	-	LCD_SEG41	SPI1_SCK	-	-	-	-	-
	PE14	-	LCD_SEG42	SPI1_MISO	-	-	-	-	-
	PE15	-	LCD_SEG43	SPI1_MOSI	-	-	-	-	-

Table 29. Embedded internal reference voltage(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LPBUF}(4)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(4)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(4)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(4)	3/4 reference voltage	-	74	75	76	

1. Refer to *Table 41: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption (I_{REFINT}).
2. Guaranteed by test in production.
3. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
4. Guaranteed by design.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is on, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 43: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in *Table 51*, *Table 26* and *Table 27* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

Figure 14. I_{DD} vs V_{DD}, at T_A= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS

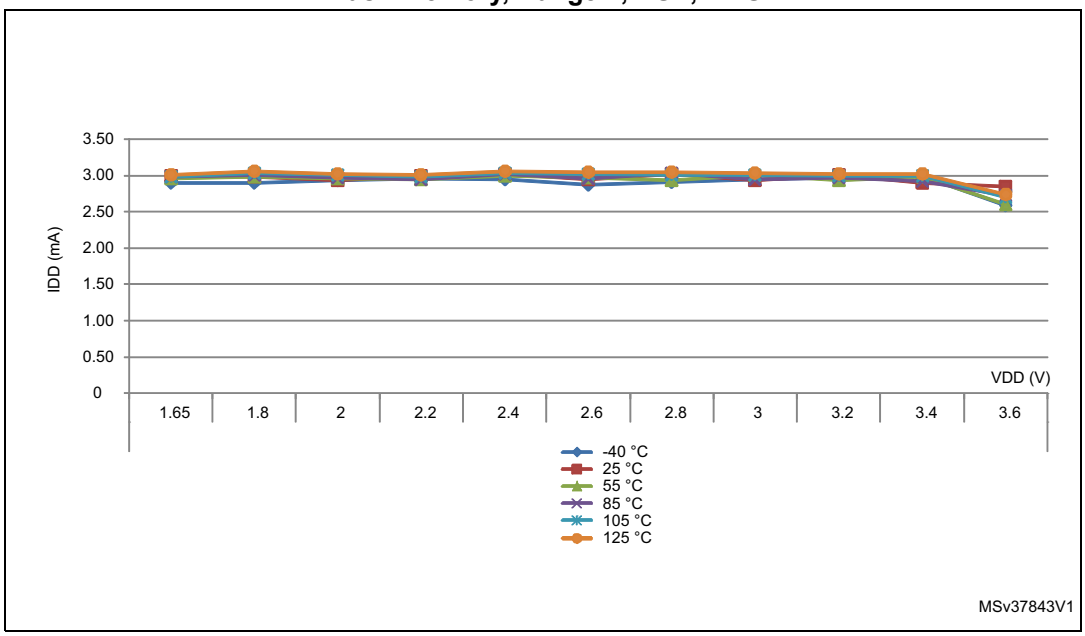


Figure 15. I_{DD} vs V_{DD}, at T_A= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS

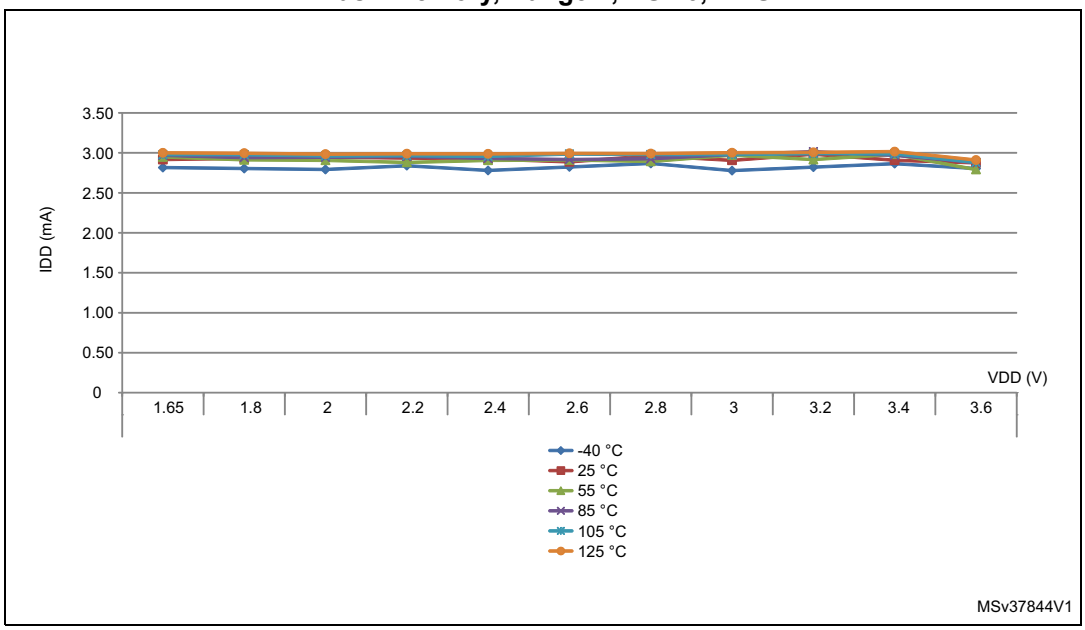


Table 39. Average current consumption during Wakeup

Symbol	parameter	System frequency	Current consumption during wakeup	Unit
I_{DD} (Wakeup from Stop)	Supply current during Wakeup from Stop mode	HSI	1	mA
		HSI/4	0,7	
		MSI clock = 4,2 MHz	0,7	
		MSI clock = 1,05 MHz	0,4	
		MSI clock = 65 KHz	0,1	
I_{DD} (Reset)	Reset pin pulled down	-	0,21	
I_{DD} (Power-up)	BOR on	-	0,23	
I_{DD} (Wakeup from StandBy)	With Fast wakeup set	MSI clock = 2,1 MHz	0,5	
	With Fast wakeup disabled	MSI clock = 2,1 MHz	0,12	

Table 40. Peripheral current consumption in Run or Sleep mode(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB2	ADC1(2)	5.5	5	3.5	4	µA/MHz (f_{HCLK})
	SPI1	4	3	3	2.5	
	USART1	14.5	11.5	9.5	12	
	TIM21	7.5	6	5	5.5	
	TIM22	7	6	5	6	
	FIREWALL	1.5	1	1	0.5	
	DBGMCU	1.5	1	1	0.5	
	SYSCFG	2.5	2	2	1.5	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	µA/MHz (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GPIOD	1	0.5	0.5	0.5	
	GPIOE	8	6	5	6	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	µA/MHz (f_{HCLK})
	FLASH	0(3)	0(3)	0(3)	0(3)	
	DMA1	10	8	6.5	8.5	
	RNG	5.5	1	0.5	0.5	
	TSC	3	2.5	2	3	
All enabled		204	162	130	202	µA/MHz (f_{HCLK})
PWR		2.5	2	2	1	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals off an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is off for this measure.
3. Current consumption is negligible and close to 0 µA.

Table 41. Peripheral current consumption in Stop and Standby mode(1)

Symbol	Peripheral	Typical consumption, T_A = 25 °C		Unit
		V_{DD}=1.8 V	V_{DD}=3.0 V	
$I_{DD(PVD / BOR)}$	-	0.7	1.2	µA
I_{REFINT}	-	-	1.7	
-	LSE Low drive(2)	0.11	0,13	
-	LSI	0.27	0.31	
-	IWDG	0.2	0.3	
-	LPTIM1, Input 100 Hz	0.01	0,01	
-	LPTIM1, Input 1 MHz	11	12	
-	LPUART1	-	0,5	
-	RTC	0.16	0,3	
-	LCD1 (static duty)	0.15	0.15	µA
-	LCD1 (1/8 duty)	1.6	2.6	

1. LCD, LPTIM, LPUART peripherals can operate in Stop mode but not in Standby mode.
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

Low-speed external user clock generated from an external source

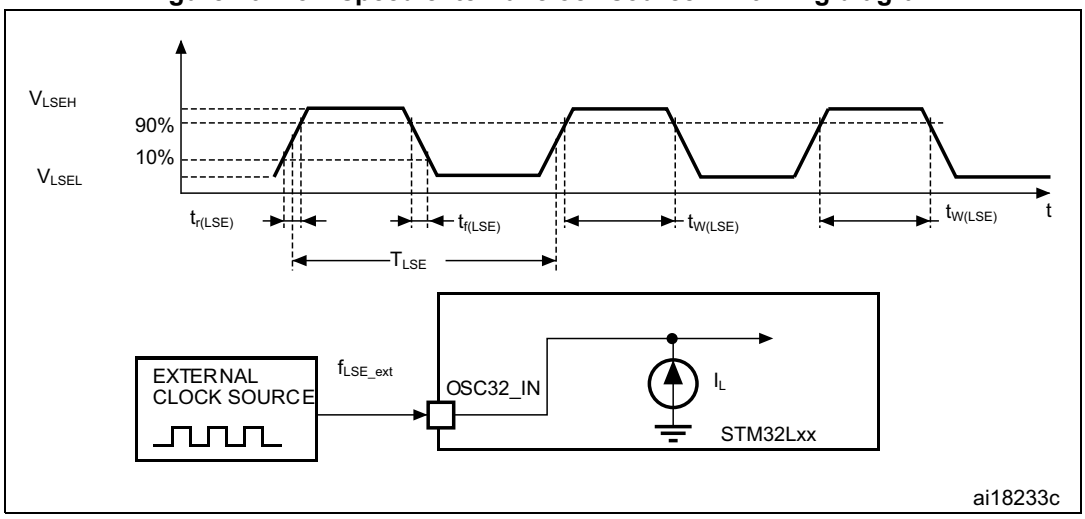
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 26*.

Table 44. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production

Figure 20. Low-speed external clock source AC timing diagram



Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

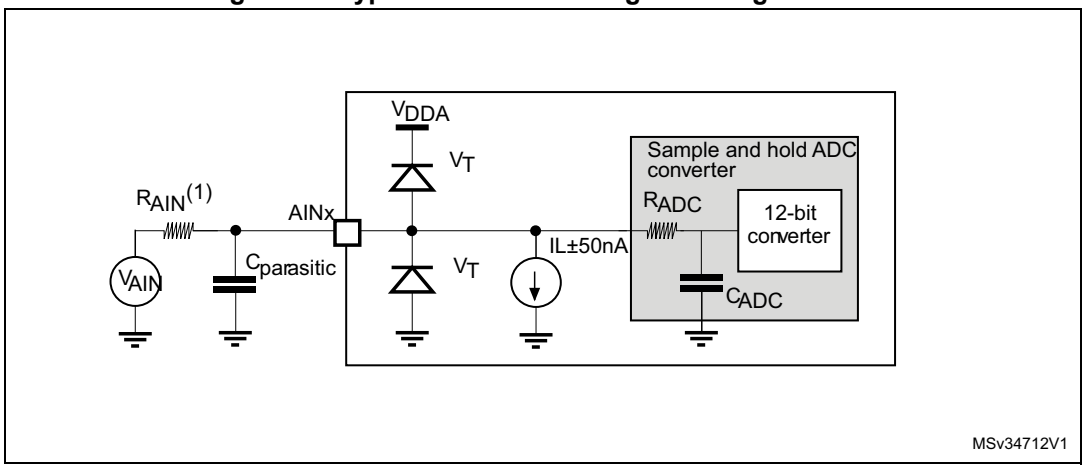
Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 56. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range at 32 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	-7	dBµV
			30 to 130 MHz	14	
			130 MHz to 1 GHz	9	
			EMI Level	2	-

Figure 29. Typical connection diagram using the ADC



1. Refer to *Table 64: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 30* or *Figure 31*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 30. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

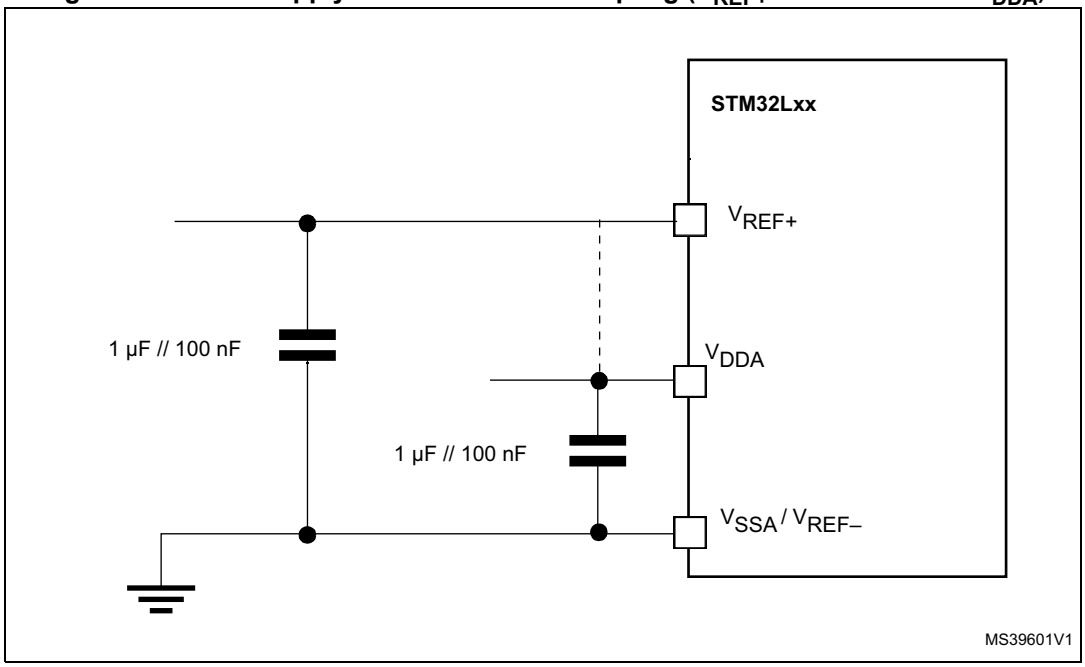
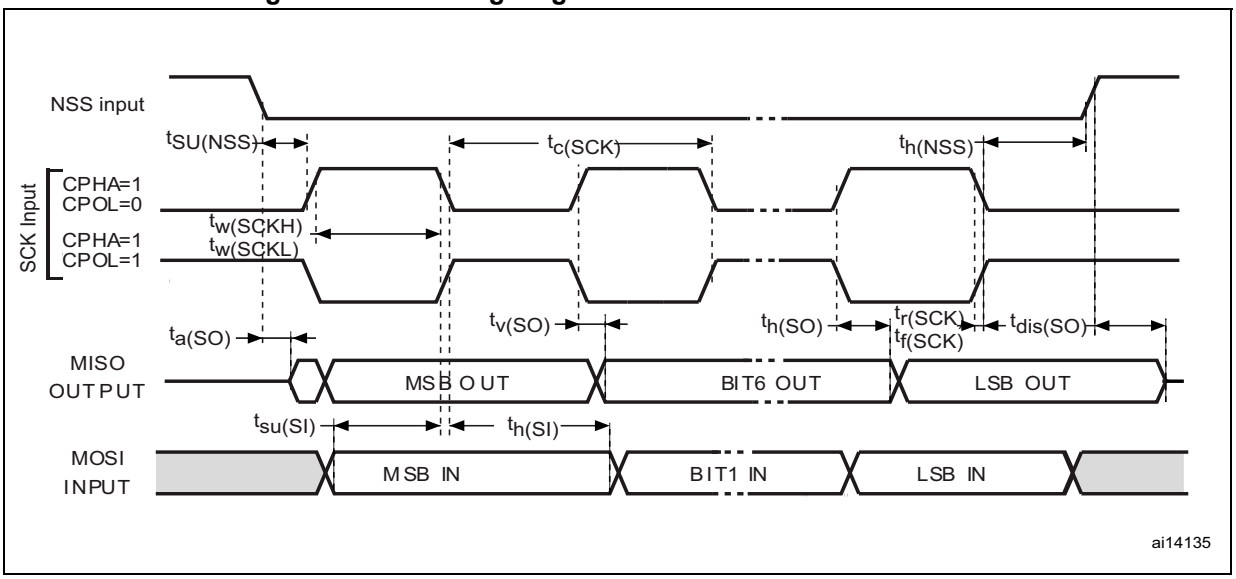
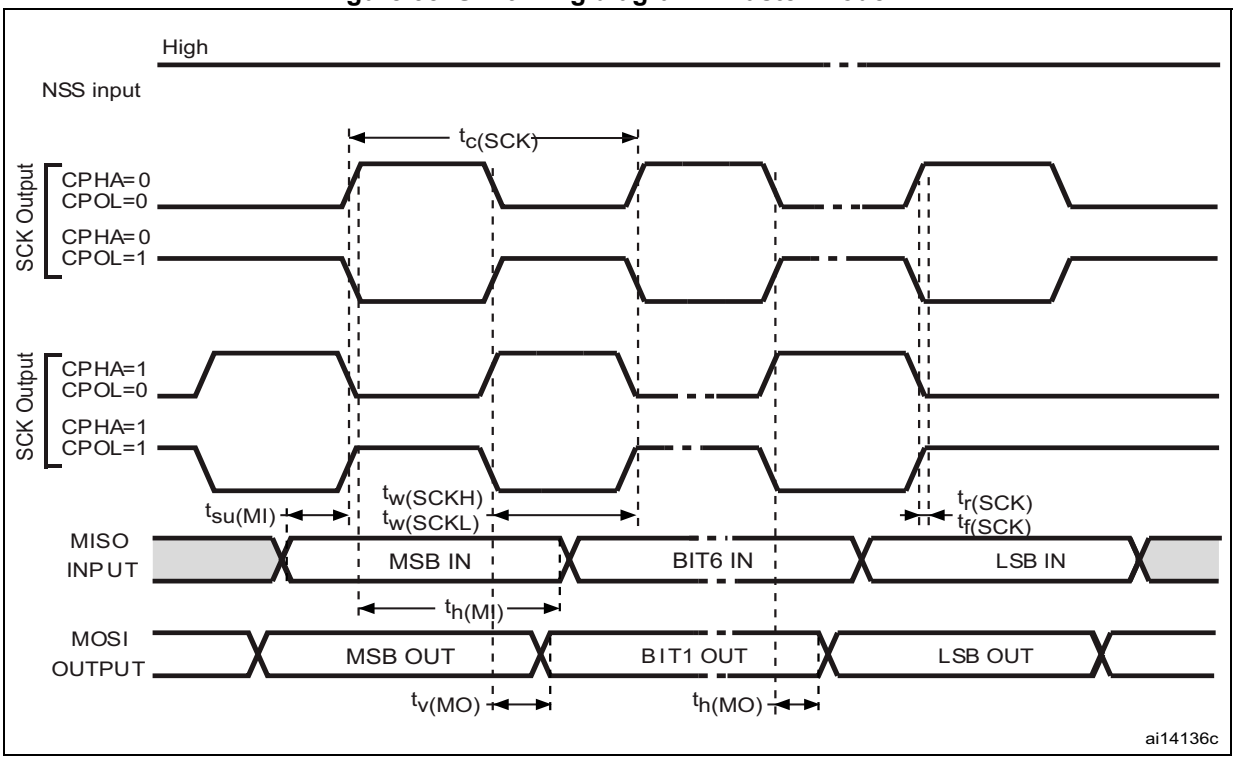


Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 35. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

I2S characteristics

Table 78. I2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs (2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	15	ns
$t_{h(WS)}$	WS hold time	Master mode	11	-	
$t_{su(WS)}$	WS setup time	Slave mode	6	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	0	-	
$t_{su(SD\_SR)}$		Slave receiver	6.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	18	-	
$t_{h(SD\_SR)}$		Slave receiver	15.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	77	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	8	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	18	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	1.5	-	

1. Guaranteed by characterization results.
2. 256xFs maximum value is equal to the maximum clock frequency.

*Note: Refer to the I2S section of the product reference manual for more details about the sampling frequency (Fs), f_{MCK}, f_{CK} and D_{CK} values. These values reflect only the digital peripheral behavior, source clock precision might slightly change them. DCK depends mainly on the ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 79. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 80. USB DC electrical characteristics

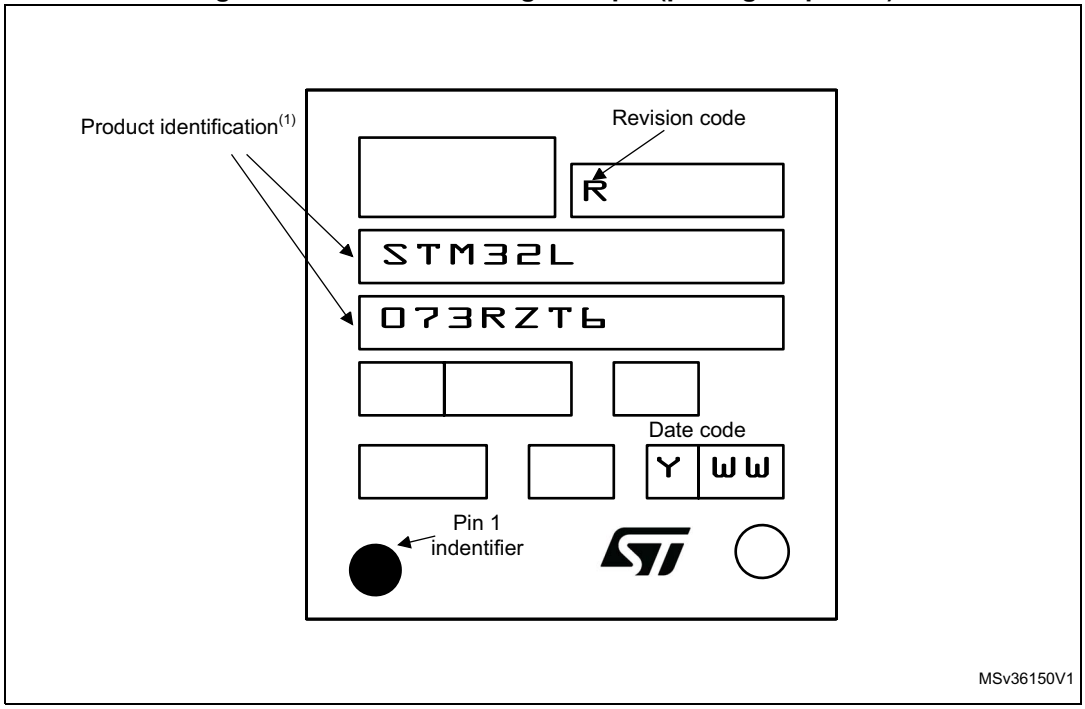
Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage	-	3.0	3.6	V
V_{DI}(2)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(2)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(2)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}(3)	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	0.3	V
V_{OH}(3)	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.
4. R_L is the load connected on the USB drivers.

Device marking for LQFP64

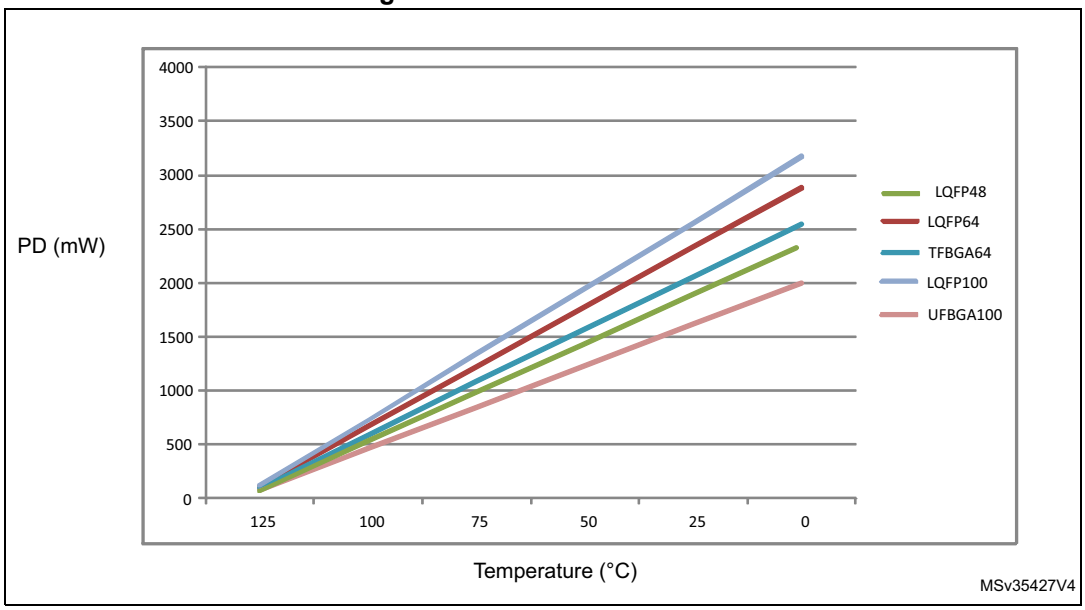
The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 47. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 54. Thermal resistance



7.6.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

9 Revision history

Table 92. Document revision history

Date	Revision	Changes
03-Aug-2015	1	Initial release
26-Oct-2015	2	Changed confidentiality level to public. Updated datasheet status to “production data”. Modified ultra-low-power platform features on cover page. Changed number of GPIOs for LQFP48 for 37 in *Table 2: Ultra-low-power STM32L073xxx device features and peripheral counts*. Changed LCD_VLCD1 into LCD_VLCD2 in *Section 3.13.2: VLCD voltage monitoring*. In *Section 6: Electrical characteristics*, updated notes related to values guaranteed by characterization. Updated $\lvert\Delta V_{SS}\rvert$ definition to include V_{REF-} in *Table 23: Voltage characteristics*. Added ΣV_{DD_USB} and updated $\Sigma I_{IO(PIN)}$ in *Figure 24: Current characteristics*. Updated *Table 56: EMI characteristics*. Updated f_{TRIG} and V_{AIN} maximum value, added V_{REF+} and V_{REF-} in *Table 64: ADC characteristics*. Updated *Section 7.2: UFBGA100 package information*. Updated *Figure 53: LQFP48 marking example (package top view)*.