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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l073rbt6

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# 2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM<sup>®</sup> Cortex<sup>®</sup>-M4, including ARM<sup>®</sup> Cortex<sup>®</sup>-M3 and ARM<sup>®</sup> Cortex<sup>®</sup>-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.



#### • Stop mode without RTC

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5  $\mu$ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB/USART/I2C/LPUART/LPTIMER wakeup events.

#### • Standby mode with RTC

The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire  $V_{CORE}$  domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC\_CSR register).

The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

#### Standby mode without RTC

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire  $V_{CORE}$  domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC\_CSR register).

The device exits Standby mode in 60  $\mu$ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode. The LCD is not stopped automatically by entering Stop mode.



			Low-	Low-	Stop		Standby	
IPs	Run/Active	Sleep	power run	power sleep		Wakeup capability		Wakeup capability
CPU	Y		Y					
Flash memory	0	0	0	0				
RAM	Y	Y	Y	Y	Y			
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	0	0	0	0				
Brown-out reset (BOR)	0	0	0	0	0	0	0	0
DMA	0	0	0	0				
Programmable Voltage Detector (PVD)	0	0	О	О	0	0	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	0	0			(3)			
High Speed External (HSE)	0	0	0	0				
Low Speed Internal (LSI)	0	0	0	0	0		0	
Low Speed External (LSE)	0	О	0	0	0		0	
Multi-Speed Internal (MSI)	0	0	Y	Y				
Inter-Connect Controller	Y	Y	Y	Y	Y			
RTC	0	0	0	0	0	0	0	
RTC Tamper	0	0	0	0	0	0	0	0
Auto WakeUp (AWU)	Ο	О	О	О	0	О	0	Ο
LCD	0	0	0	0	0			
USB	0	0				0	1	
USART	0	0	0	0	O <sup>(4)</sup>	0		
LPUART	0	0	0	0	0 <sup>(4)</sup>	0		
SPI	0	0	0	0				
I2C	0	0	0	0	O <sup>(5)</sup>	0		
ADC	0	0						

# Table 5. Functionalities depending on the working mode (from Run/active down to standby) <sup>(1)(2)</sup>



			Low-	Low-		Stop	Standby	
IPs	Run/Active	Sleep	power run	power sleep		Wakeup capability		Wakeup capability
DAC	0	0	0	0	0			
Temperature sensor	0	О	0	0	0			
Comparators	0	0	0	0	0	0		
16-bit timers	0	0	0	0				
LPTIMER	0	0	0	0	0	0		
IWDG	0	0	0	0	0	0	0	0
WWDG	0	0	0	0				
Touch sensing controller (TSC)	0	О						
SysTick Timer	0	0	0	0				
GPIOs	0	0	0	0	0	0		2 pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs		3.5 µs		50 µs
					0. RTC	4 µA (No ) V <sub>DD</sub> =1.8 V	0.1 RTC	28 µA (No ) V <sub>DD</sub> =1.8 V
Consumption $V_{-} = 1.8 \text{ to } 3.6 \text{ V}$	Down to 140 µA/MHz	Down to 37 µA/MHz	Down to	Down to	0.8 µA (with RTC) V <sub>DD</sub> =1.8 V		0.65 µA (with RTC) V <sub>DD</sub> =1.8 V	
(Typ)	(from Flash memory)	(from Flash memory)	8 µA	4.5 µA	0.4 μA (No RTC) V <sub>DD</sub> =3.0 V		0.29 µA (No RTC) V <sub>DD</sub> =3.0 V	
					1 μΑ V	(with RTC) <sub>DD</sub> =3.0 V	0.8 RTC	85 μΑ (with ) V <sub>DD</sub> =3.0 V

Table 5.	Functionalities	depending on	the working	mode
(from	Run/active dow	vn to standby)	(continued) <sup>(1</sup>	1)(2)

Legend: "Y" = Yes (enable). "O" = Optional can be enabled/disabled by software) "-" = Not available

2. The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.

Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.

4. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.

5. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.





1. The above figure shows the package top view.

2. I/O pin supplied by VDD\_USB.



STM32L073xx

Table 16.	STM32L	.073xx	pin	definition	(continued)
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	Pi	n num	ber							
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100	Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
-	8	E3	15	H1	PC0	I/O	FTf	-	LPTIM1_IN1, LCD_SEG18, EVENTOUT, TSC_G7_IO1, LPUART1_RX, I2C3_SCL	ADC_IN10
-	9	E2	16	J2	PC1	I/O	FTf	-	LPTIM1_OUT, LCD_SEG19, EVENTOUT, TSC_G7_IO2, LPUART1_TX, I2C3_SDA	ADC_IN11
-	10	F2	17	J3	PC2	I/O	FTf	-	LPTIM1_IN2, LCD_SEG20, SPI2_MISO/I2S2_MCK, TSC_G7_IO3	ADC_IN12
-	11	-	18	K2	PC3	I/O	FT	-	LPTIM1_ETR, LCD_SEG21, SPI2_MOSI/I2S2_SD, TSC_G7_IO4	ADC_IN13
8	12	F1	19	J1	VSSA	S	-	-	-	-
-	-	-	20	K1	VREF-	S	-	-	-	-
-	-	G1	21	L1	VREF+	S	-	-	-	-
9	13	H1	22	M1	VDDA	S	-	-	-	-
10	14	G2	23	L2	PA0	I/O	тс	-	TIM2_CH1, TSC_G1_IO1, USART2_CTS, TIM2_ETR, USART4_TX, COMP1_OUT	COMP1_INM, ADC_IN0, RTC_TAMP2/WKUP1
11	15	H2	24	M2	PA1	I/O	FT	-	EVENTOUT, LCD_SEG0, TIM2_CH2, TSC_G1_IO2, USART2_RTS_DE, TIM21_ETR, USART4_RX	COMP1_INP, ADC_IN1
12	16	F3	25	K3	PA2	I/O	FT	-	TIM21_CH1, LCD_SEG1, TIM2_CH3, TSC_G1_IO3, USART2_TX, LPUART1_TX, COMP2_OUT	COMP2_INM, ADC_IN2
13	17	G3	26	L3	PA3	I/O	FT	-	TIM21_CH2, LCD_SEG2, TIM2_CH4, TSC_G1_IO4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3



Table 16. STM32	_073xx pin	definition	(continued)
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	Pi	n num	ber							
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100	Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
-	-	-	41	L8	PE10	I/O	FT	-	TIM2_CH2, LCD_SEG40, USART5_TX	-
-	-	-	42	M9	PE11	I/O	FT	-	TIM2_CH3, USART5_RX	LCD_VLCD2
-	-	-	43	L9	PE12	I/O	FT	-	TIM2_CH4, SPI1_NSS	LCD_VLCD3
-	-	-	44	M10	PE13	I/O	FT	-	LCD_SEG41, SPI1_SCK	-
-	-	-	45	M11	PE14	I/O	FT	-	LCD_SEG42, SPI1_MISO	-
-	-	-	46	M12	PE15	I/O	FT	-	LCD_SEG43, SPI1_MOSI	-
21	29	G7	47	L10	PB10	I/O	FT	-	LCD_SEG10, TIM2_CH3, TSC_SYNC, LPUART1_TX, SPI2_SCK, I2C2_SCL, LPUART1_RX	-
22	30	H7	48	L11	PB11	I/O	FT	-	EVENTOUT, LCD_SEG11, TIM2_CH4, TSC_G6_IO1, LPUART1_RX, I2C2_SDA, LPUART1_TX	-
23	31	D6	49	F12	VSS	S		-	-	-
24	32	E5	50	G12	VDD	S		-	-	-
25	33	H8	51	L12	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LCD_SEG12, LPUART1_RTS_DE, TSC_G6_IO2, I2C2_SMBA, EVENTOUT	LCD_VLCD2
26	34	G8	52	K12	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, LCD_SEG13, MCO, TSC_G6_IO3, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
27	35	F8	53	K11	PB14	I/O	FTf	-	SPI2_MISO/I2S2_MCK, LCD_SEG14, RTC_OUT, TSC_G6_IO4, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
28	36	F7	54	K10	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD, LCD_SEG15, RTC_REFIN	-
-	-	-	55	К9	PD8	I/O	FT	-	LPUART1_TX, LCD_SEG28	-



Table 16.	STM32L	073xx	pin	definition	(continued)
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	Pi	n num	ber							
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100	Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
33	45	B8	71	A12	PA12	I/O	FT	(2)	SPI1_MOSI, EVENTOUT, TSC_G4_IO4, USART1_RTS_DE, COMP2_OUT	USB_DP
34	46	A8	72	A11	PA13	I/O	FT	-	SWDIO, USB_OE, LPUART1_RX	-
-	-	-	73	C11	VDD	S		-	-	-
35	47	D5	74	F11	VSS	S		-	-	-
36	48	E6	75	G11	VDD_USB	S		-	-	-
37	49	A7	76	A10	PA14	I/O	FT	-	SWCLK, USART2_TX, LPUART1_TX	-
38	50	A6	77	A9	PA15	I/O	FT	-	SPI1_NSS, LCD_SEG17, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1, USART4_RTS_DE	-
-	51	B7	78	B11	PC10	I/O	FT	-	LPUART1_TX, LCD_COM4/LCD_SEG28/ LCD_SEG48, USART4_TX	-
-	52	B6	79	C10	PC11	I/O	FT	-	LPUART1_RX, LCD_COM5/LCD_SEG29/ LCD_SEG49, USART4_RX	-
-	53	C5	80	B10	PC12	I/O	FT	-	LCD_COM6/LCD_SEG30/ LCD_SEG50, USART5_TX, USART4_CK	-
-	-	-	81	C9	PD0	I/O	FT	-	TIM21_CH1, SPI2_NSS/I2S2_WS	-
-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK/I2S2_CK	-
-	54	В5	83	C8	PD2	I/O	FT	-	LPUART1_RTS_DE, LCD_COM7/LCD_SEG31/ LCD_SEG51, TIM3_ETR, USART5_RX	-
-	-	-	84	B8	PD3	I/O	FT	-	USART2_CTS, LCD_SEG44, SPI2_MISO/I2S2_MCK	-



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	Table 18. Alternate functions port B											
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7			
	Port	SPI1/SPI2/I2S2/ USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I 2C1/LCD/ TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/L I2C1/TSC/ PTIM1/TIM2/3/E EVENTOUT VENTOUT/ SYS_AF		I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT SPI2/I2S2/I2C2/ USART1/ TIM2/21/22		I2C3/LPUART1/ COMP1/2/ TIM3			
	PB0	EVENTOUT	LCD_SEG5	TIM3_CH3	TSC_G3_IO2	-	-	-	-			
	PB1	-	LCD_SEG6	TIM3_CH4	TSC_G3_IO3	LPUART1_RTS_DE	-	-	-			
	PB2	-	-	LPTIM1_OUT	TSC_G3_IO4	-	-	-	I2C3_SMBA			
	PB3	SPI1_SCK	LCD_SEG7	TIM2_CH2	TSC_G5_IO1	EVENTOUT	USART1_RTS_DE	USART5_TX	-			
	PB4	SPI1_MISO	LCD_SEG8	TIM3_CH1	TSC_G5_IO2	TIM22_CH1	USART1_CTS	USART5_RX	I2C3_SDA			
	PB5	SPI1_MOSI	LCD_SEG9	LPTIM1_IN1	I2C1_SMBA	TIM3_CH2/ TIM22_CH2	USART1_CK	USART5_CK/ USART5_RTS_D E	-			
	PB6	USART1_TX	I2C1_SCL	LPTIM1_ETR	TSC_G5_IO3	-	-	-	-			
	PB7	USART1_RX	I2C1_SDA	LPTIM1_IN2	TSC_G5_IO4	-	-	USART4_CTS	-			
ort B	PB8	-	LCD_SEG16	-	TSC_SYNC	I2C1_SCL	-	-	-			
đ	PB9	-	LCD_COM3	EVENTOUT	-	I2C1_SDA	SPI2_NSS/ I2S2_WS	-	-			
	PB10	-	LCD_SEG10	TIM2_CH3	TSC_SYNC	LPUART1_TX	SPI2_SCK	I2C2_SCL	LPUART1_RX			
	PB11	EVENTOUT	LCD_SEG11	TIM2_CH4	TSC_G6_IO1	LPUART1_RX	-	I2C2_SDA	LPUART1_TX			
	PB12	SPI2_NSS/I2S2_WS	LCD_SEG12	LPUART1_RTS_ DE	TSC_G6_IO2		I2C2_SMBA	EVENTOUT	-			
	PB13	SPI2_SCK/I2S2_CK	LCD_SEG13	MCO	TSC_G6_IO3	LPUART1_CTS	I2C2_SCL	TIM21_CH1	-			
	PB14	SPI2_MISO/ I2S2_MCK	LCD_SEG14	RTC_OUT	TSC_G6_IO4	LPUART1_RTS_DE	I2C2_SDA	TIM21_CH2	-			
	PB15	SPI2_MOSI/ I2S2_SD	LCD_SEG15	RTC_REFIN	-	-	-	-	-			

# Pin descriptions

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# 6.1.7 Optional LCD power supply scheme



# Figure 12. Optional LCD power supply scheme

1. Option 1: LCD power supply is provided by a dedicated VLCD supply source, VSEL switch is open.

2. Option 2: LCD power supply is provided by the internal step-up converter, VSEL switch is closed, an external capacitance is needed for correct behavior of this converter.

# 6.1.8 Current consumption measurement



# Figure 13. Current consumption measurement scheme



Symbol	Parameter	Conditions	Тур	Мах	Unit			
t <sub>WUSLEEP</sub>	Wakeup from Sleep mode	f <sub>HCLK</sub> = 32 MHz	7	8				
twusleep	Wakeup from Low-power sleep mode,	f <sub>HCLK</sub> = 262 kHz Flash memory enabled	7	8	Number of clock			
LP	f <sub>HCLK</sub> = 262 kHz	f <sub>HCLK</sub> = 262 kHz Flash memory switched OFF	9	10	cycles			
		f <sub>HCLK</sub> = f <sub>MSI</sub> = 4.2 MHz	5.0	8				
	Wakeup from Stop mode, regulator in Run mode	f <sub>HCLK</sub> = f <sub>HSI</sub> = 16 MHz	4.9	7	1			
		f <sub>HCLK</sub> = f <sub>HSI</sub> /4 = 4 MHz	8.0	11				
		f <sub>HCLK</sub> = f <sub>MSI</sub> = 4.2 MHz Voltage range 1	5.0	8				
		f <sub>HCLK</sub> = f <sub>MSI</sub> = 4.2 MHz Voltage range 2	5.0	8				
		f <sub>HCLK</sub> = f <sub>MSI</sub> = 4.2 MHz Voltage range 3	5.0	8				
		f <sub>HCLK</sub> = f <sub>MSI</sub> = 2.1 MHz	7.3	13				
t <sub>WUSTOP</sub>	Wakeup from Stop mode, regulator in low- power mode	f <sub>HCLK</sub> = f <sub>MSI</sub> = 1.05 MHz	13	23				
		f <sub>HCLK</sub> = f <sub>MSI</sub> = 524 kHz	28	38	μs			
		f <sub>HCLK</sub> = f <sub>MSI</sub> = 262 kHz	51	65				
		f <sub>HCLK</sub> = f <sub>MSI</sub> = 131 kHz	100	120				
		f <sub>HCLK</sub> = MSI = 65 kHz	190	260				
		f <sub>HCLK</sub> = f <sub>HSI</sub> = 16 MHz	4.9	7				
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	8.0	11				
		f <sub>HCLK</sub> = f <sub>HSI</sub> = 16 MHz	4.9	7	1			
	wakeup from Stop mode, regulator in low- power mode, code running from RAM	f <sub>HCLK</sub> = f <sub>HSI</sub> /4 = 4 MHz	7.9	10				
		f <sub>HCLK</sub> = f <sub>MSI</sub> = 4.2 MHz	4.7	8				
+	Wakeup from Standby mode FWU bit = 1	f <sub>HCLK</sub> = MSI = 2.1 MHz	65	130				
WUSTDBY	Wakeup from Standby mode FWU bit = 0	f <sub>HCLK</sub> = MSI = 2.1 MHz	2.2	3	ms			

Table 42. Low-power mode wakeup timings



# Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a lowspeed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 26*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f <sub>LSE_ext</sub>	User external clock source frequency		1	32.768	1000	kHz
V <sub>LSEH</sub>	OSC32_IN input pin high level voltage		0.7V <sub>DD</sub>	-	V <sub>DD</sub>	V
V <sub>LSEL</sub>	OSC32_IN input pin low level voltage	-	V <sub>SS</sub>	-	0.3V <sub>DD</sub>	v
t <sub>w(LSE)</sub> t <sub>w(LSE)</sub>	OSC32_IN high or low time		465	-	-	ne
t <sub>r(LSE)</sub> t <sub>f(LSE)</sub>	OSC32_IN rise or fall time		-	-	10	115
C <sub>IN(LSE)</sub>	OSC32_IN input capacitance	-	-	0.6	-	pF
DuCy <sub>(LSE)</sub>	Duty cycle	-	45	-	55	%
١L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

 Table 44. Low-speed external user clock characteristics<sup>(1)</sup>

1. Guaranteed by design, not tested in production







# 6.3.13 I/O port characteristics

# General input/output characteristics

Unless otherwise specified, the parameters given in *Table 60* are derived from tests performed under the conditions summarized in *Table 26*. All I/Os are CMOS and TTL compliant.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
VIL	Input low level voltage	TC, FT, FTf, RST I/Os	-	-	0.3V <sub>DD</sub>	
		BOOT0 pin	-	-	0.14V <sub>DD</sub> <sup>(1)</sup>	
V <sub>IH</sub>	Input high level voltage	All I/Os	0.7 V <sub>DD</sub>	-	-	
V.	I/O Schmitt trigger voltage hysteresis	Standard I/Os	-	10% V <sub>DD</sub> <sup>(3)</sup>	-	
♥ hys	(2)	BOOT0 pin	-	0.01	-	
		$\label{eq:VSS} \begin{array}{l} V_{SS} \leq V_{IN} \leq V_{DD} \\ \mbox{All I/Os except for} \\ \mbox{PA11, PA12, BOOT0} \\ \mbox{and FTf I/Os} \end{array}$	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ , PA11 and PA12 I/Os	-	-	-50/+250	nA
		V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> FTf I/Os	-	-	±100	
l <sub>ikg</sub>	Input leakage current <sup>(4)</sup>	$\label{eq:VDD} \begin{array}{l} V_{DD}{}^{\leq}V_{IN}{}^{\leq}5V\\ \mbox{All I/Os except for}\\ \mbox{PA11, PA12, BOOT0}\\ \mbox{and FTf I/Os} \end{array}$	-	-	200	nA
		V <sub>DD</sub> ≤ V <sub>IN</sub> ≤ 5 V FTf I/Os	-	-	500	
		$V_{DD} \le V_{IN} \le 5 V$ PA11, PA12 and BOOT0	-	-	10	μA
R <sub>PU</sub>	Weak pull-up equivalent resistor <sup>(5)</sup>	$V_{IN} = V_{SS}$	30	45	60	kΩ
R <sub>PD</sub>	Weak pull-down equivalent resistor <sup>(5)</sup>	$V_{IN} = V_{DD}$	30	45	60	kΩ
C <sub>IO</sub>	I/O pin capacitance	-	-	5	-	pF

Table 60. I/O static characteris	stics
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1. Guaranteed by characterization.

2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

3. With a minimum of 200 mV. Guaranteed by characterization results.

4. The max. value may be exceeded if negative current is injected on adjacent pins.

 Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).



# **Output voltage levels**

Unless otherwise specified, the parameters given in *Table 61* are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in *Table 26*. All I/Os are CMOS and TTL compliant.

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>OL</sub> <sup>(1)</sup>	Output low level voltage for an I/O pin	CMOS port <sup>(2)</sup> ,	-	0.4	
V <sub>OH</sub> <sup>(3)</sup>	Output high level voltage for an I/O pin	$1_{O} = +0.01$ A 2.7 V $\leq V_{DD} \leq 3.6$ V	V <sub>DD</sub> -0.4	-	
V <sub>OL</sub> <sup>(1)</sup>	Output low level voltage for an I/O pin	$\begin{array}{c} {\sf TTL \ port}^{(2)}, \\ {\sf I}_{IO} \ \mbox{=+} \ \mbox{8 mA} \\ {\sf 2.7 \ V} \le {\sf V}_{DD} \le \ \mbox{3.6 V} \end{array}$	-	0.4	
V <sub>OH</sub> <sup>(3)(4)</sup>	Output high level voltage for an I/O pin	$\begin{array}{l} \text{TTL port}^{(2)},\\ \text{I}_{\text{IO}} \texttt{=} -\texttt{6} \text{ mA}\\ \textbf{2.7} \text{ V} \leq \text{V}_{\text{DD}} \leq \ \textbf{3.6} \text{ V} \end{array}$	2.4	-	
V <sub>OL</sub> <sup>(1)(4)</sup>	Output low level voltage for an I/O pin	$I_{IO}$ = +15 mA 2.7 V $\leq$ V <sub>DD</sub> $\leq$ 3.6 V	-	1.3	V
V <sub>OH</sub> <sup>(3)(4)</sup>	Output high level voltage for an I/O pin	$\begin{array}{l} \text{I}_{\text{IO}} \text{ = -15 mA} \\ \text{2.7 V} \leq \text{V}_{DD} \leq \ \text{3.6 V} \end{array}$	V <sub>DD</sub> -1.3	-	
V <sub>OL</sub> <sup>(1)(4)</sup>	Output low level voltage for an I/O pin	$I_{IO}$ = +4 mA 1.65 V $\leq$ V <sub>DD</sub> < 3.6 V	-	0.45	
V <sub>OH</sub> <sup>(3)(4)</sup>	Output high level voltage for an I/O pin	$I_{IO}$ = -4 mA 1.65 V $\leq$ V <sub>DD</sub> $\leq$ 3.6 V	V <sub>DD</sub> -0.45	-	
V <sub>OLFM+</sub> <sup>(1)(4)</sup>	Output low level voltage for an FTf	$I_{IO} = 20 \text{ mA} \\ 2.7 \text{ V} \le V_{DD} \le 3.6 \text{ V}$	-	0.4	
	I/O pin in Fm+ mode	$I_{IO} = 10 \text{ mA} \\ 1.65 \text{ V} \le \text{V}_{DD} \le 3.6 \text{ V}$	-	0.4	

Table 61. Output voltage	characteristics
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 The I<sub>IO</sub> current sunk by the device must always respect the absolute maximum rating specified in *Table 24*. The sum of the currents sunk by all the I/Os (I/O ports and control pins) must always be respected and must not exceed ΣI<sub>IO(PIN)</sub>.

2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

3. The I<sub>IO</sub> current sourced by the device must always respect the absolute maximum rating specified in Table 24. The sum of the currents sourced by all the I/Os (I/O ports and control pins) must always be respected and must not exceed  $\Sigma I_{IO(PIN)}$ .

4. Guaranteed by characterization results.



# Equation 1: R<sub>AIN</sub> max formula

$$R_{AIN} < \frac{T_{S}}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The simplified formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

R max for R <sub>AIN</sub> max fo						c for stand	for standard channels (k $\Omega$ )				
T <sub>s</sub> (cycles)	$ \begin{array}{c c} t_{S} \\ (\mu S) \end{array} \begin{pmatrix} t_{AIN} & hax \ tor \\ fast \ channels \\ (k\Omega) \end{pmatrix} & V_{DD} > \\ \hline V_{DD} > \\ 2.7 \ V \\ \hline 2.4 \ V \\ 2.0 \ V \\ 1.8 \ V \\ \hline \end{array} $		V <sub>DD</sub> > 1.75 V	V <sub>DD</sub> > 1.65 V and T <sub>A</sub> > –10 °C	V <sub>DD</sub> > 1.65 V and T <sub>A</sub> > 25 °C						
1.5	0.09	0.5	< 0.1	NA	NA	NA	NA	NA	NA		
3.5	0.22	1	0.2	< 0.1	NA	NA	NA	NA	NA		
7.5	0.47	2.5	1.7	1.5	< 0.1	NA	NA	NA	NA		
12.5	0.78	4	3.2	3	1	NA	NA	NA	NA		
19.5	1.22	6.5	5.7	5.5	3.5	NA	NA	NA	< 0.1		
39.5	2.47	13	12.2	12	10	NA	NA	NA	5		
79.5	4.97	27	26.2	26	24	< 0.1	NA	NA	19		
160.5	10.03	50	49.2	49	47	32	< 0.1	< 0.1	42		

Table 65.  $R_{AIN}$  max for  $f_{ADC}$  = 16 MHz<sup>(1)</sup>

1. Guaranteed by design.

# Table 66. ADC accuracy<sup>(1)(2)(3)</sup>

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
ET	Total unadjusted error		-	2	4	
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	LSB
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.5	
	Effective number of bits	1.65 V < VDDA = VDEE+< 3.6 V.	10.2	11		
ENOB	Effective number of bits (16-bit mode oversampling with ratio =256) <sup>(4)</sup>	range 1/2/3	11.3	12.1	-	bits
SINAD	Signal-to-noise distortion		63	69	-	
	Signal-to-noise ratio		63	69	-	
SNR	Signal-to-noise ratio (16-bit mode oversampling with ratio =256) <sup>(4)</sup>		70	76	-	dB
THD	Total harmonic distortion		-	-85	-73	



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
ET	Total unadjusted error		-	2	5	
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	LSB
EL	Integral linearity error		-	1.5	3	
ED	Differential linearity error	1.65 V < V <sub>REF+</sub> <v<sub>DDA &lt; 3.6 V,</v<sub>		1	2	
ENOB	Effective number of bits		10.0	11.0	-	bits
SINAD	Signal-to-noise distortion		62	69	-	
SNR	Signal-to-noise ratio		61	69	-	dB
THD	Total harmonic distortion		-	-85	-65	

# Table 66. ADC accuracy<sup>(1)(2)(3)</sup> (continued)

1. ADC DC accuracy values are measured after internal calibration.

 ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.

Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in Section 6.3.12 does not affect the ADC accuracy.

3. Better performance may be achieved in restricted V<sub>DDA</sub>, frequency and temperature ranges.

4. This number is obtained by the test board without additional noise, resulting in non-optimized value for oversampling mode.



## Figure 28. ADC accuracy characteristics



The analog spike filter is compliant with  $I^2C$  timings requirements only for the following voltage ranges:

- Fast mode Plus: 2.7 V  $\leq$  V<sub>DD</sub>  $\leq$  3.6 V and voltage scaling Range 1
- Fast mode:
  - 2 V  $\leq$  V\_{DD}  $\leq$  3.6 V and voltage scaling Range 1 or Range 2.
  - V<sub>DD</sub> < 2 V, voltage scaling Range 1 or Range 2, C<sub>load</sub> < 200 pF.</li>

In other ranges, the analog filter should be disabled. The digital filter can be used instead.

Note: In Standard mode, no spike filter is required.

Table 73.	. I2C	analog	filter	characteristics <sup>(1</sup>	I)	
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Symbol	Parameter	Conditions	Min	Мах	Unit
		Range 1		100 <sup>(3)</sup>	
t <sub>AF</sub>	Maximum pulse width of spikes that are suppressed by the analog filter	Range 2	50 <sup>(2)</sup>	-	ns
		Range 3		-	

- 1. Guaranteed by characterization results.
- 2. Spikes with widths below  $t_{\mbox{AF}(\mbox{min})}$  are filtered.
- 3. Spikes with widths above  $t_{AF(max)}$  are not filtered

## **USART/LPUART** characteristics

The parameters given in the following table are guaranteed by design.

Symbol	Parameter	Conditions	Тур	Max	Unit
		Stop mode with main regulator in Run mode, Range 2 or 3	-	8.7	
<sup>t</sup> wuusart	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode	Stop mode with main regulator in Run mode, Range 1	-	8.1	μs
		Stop mode with main regulator in low-power mode, Range 2 or 3	-	12	
		Stop mode with main regulator in low-power mode, Range 1	-	11.4	

#### Table 74. USART/LPUART characteristics





Figure 38. USB timings: definition of data signal rise and fall time

	Table 81.	USB: full	speed	electrical	characteristics
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Driver characteristics <sup>(1)</sup>									
Symbol	Parameter	Conditions	Min	Max	Unit				
t <sub>r</sub>	Rise time <sup>(2)</sup>	C <sub>L</sub> = 50 pF	4	20	ns				
t <sub>f</sub>	Fall Time <sup>(2)</sup>	C <sub>L</sub> = 50 pF	4	20	ns				
t <sub>rfm</sub>	Rise/ fall time matching	t <sub>r</sub> /t <sub>f</sub>	90	110	%				
V <sub>CRS</sub>	Output signal crossover voltage		1.3	2.0	V				

1. Guaranteed by design.

2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

# 6.3.21 LCD controller

The devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the  $V_{DD}$  voltage. An external capacitor  $C_{ext}$  must be connected to the  $V_{LCD}$  pin to decouple this converter.

Symbol	Parameter	Min	Тур	Мах	Unit
V <sub>LCD</sub>	LCD external voltage	-	-	3.6	
V <sub>LCD0</sub>	LCD internal reference voltage 0	-	2.6	-	
V <sub>LCD1</sub>	LCD internal reference voltage 1	-	2.73	-	
V <sub>LCD2</sub>	LCD internal reference voltage 2	-	2.86	-	
V <sub>LCD3</sub>	LCD internal reference voltage 3	-	2.98	-	V
V <sub>LCD4</sub>	LCD internal reference voltage 4	-	3.12	-	
V <sub>LCD5</sub>	LCD internal reference voltage 5	-	3.26	-	
V <sub>LCD6</sub>	LCD internal reference voltage 6	-	3.4	-	
V <sub>LCD7</sub>	LCD internal reference voltage 7	-	3.55	-	
C <sub>ext</sub>	V <sub>LCD</sub> external capacitance	0.1	-	2	μF

Table 82. LCD controller characteristics



# 7.5 LQFP48 package information

Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.



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