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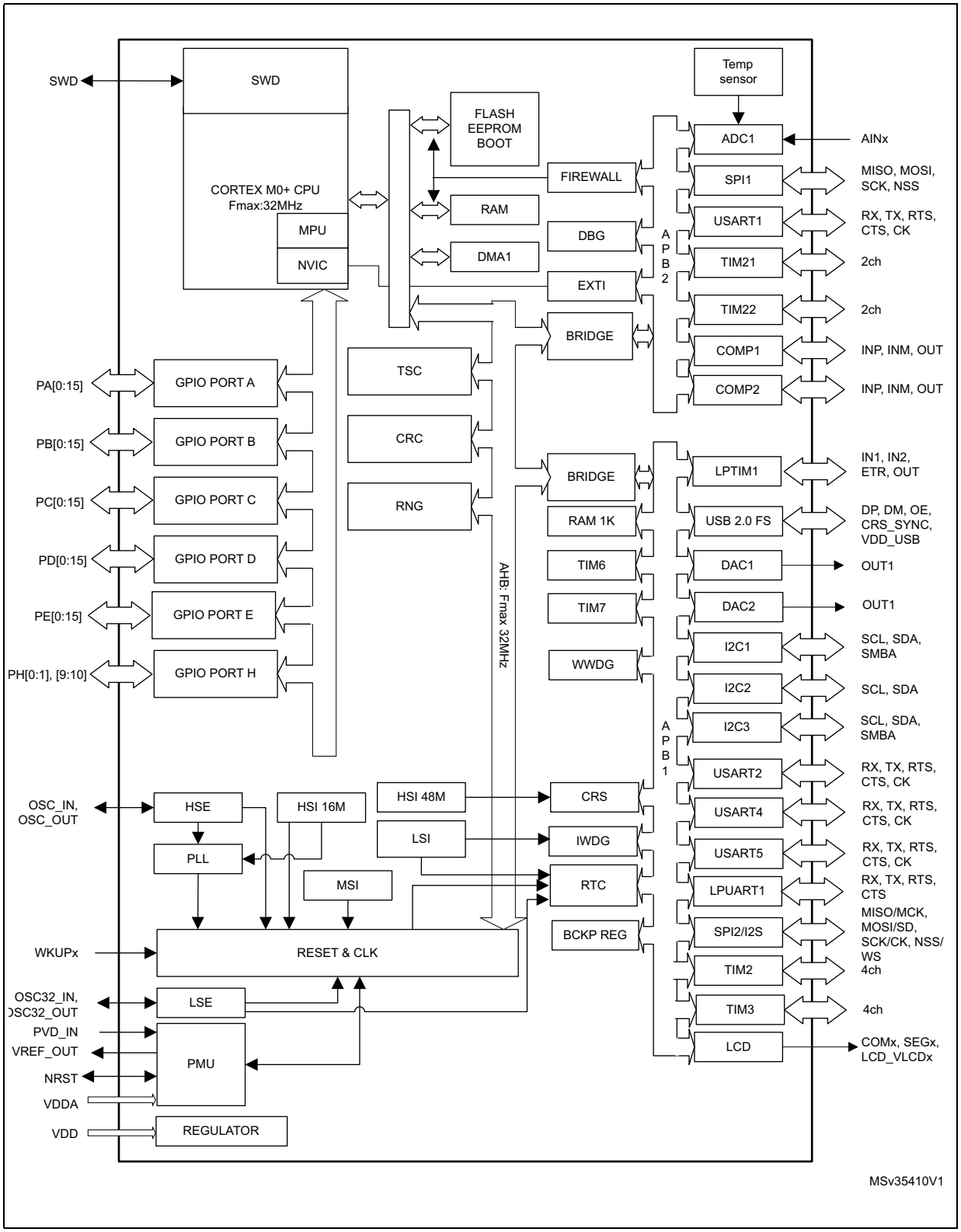
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l073rzt6

Figure 1. STM32L073xx block diagram



- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS)**

  This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

  Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.

- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

3.10 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, LPUART, general-purpose timers, DAC, and ADC.

3.11 Liquid crystal display (LCD)

The LCD drives up to 8 common terminals and 48 segment terminals to drive up to 384 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode
- V_{LCD} rails decoupling capability

3.12 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L073xx device. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference, V_{LCD} voltage measurement). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.

The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 µA at 10 kSPS, ~240 µA at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

3.16 Touch sensing controller (TSC)

The STM32L073xx provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (such as glass, plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 9. Capacitive sensing GPIOs available on STM32L073xx devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PC0
	TSC_G3_IO2	PB0		TSC_G7_IO2	PC1
	TSC_G3_IO3	PB1		TSC_G7_IO3	PC2
	TSC_G3_IO4	PB2		TSC_G7_IO4	PC3
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PC6
	TSC_G4_IO2	PA10		TSC_G8_IO2	PC7
	TSC_G4_IO3	PA11		TSC_G8_IO3	PC8
	TSC_G4_IO4	PA12		TSC_G8_IO4	PC9

3.18.2 Universal synchronous/asynchronous receiver transmitter (USART)

The four USART interfaces (USART1, USART2, USART4 and USART5) are able to communicate at speeds of up to 4 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 and USART2 also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

All USART interfaces can be served by the DMA controller.

Table 13 for the supported modes and features of USART interfaces.

Table 13. USART implementation

USART modes/features(1)	USART1 and USART2	USART4 and USART5
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode(2)	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection (4 modes)	X	-
Driver Enable	X	X

1. X = supported.
2. This mode allows using the USART as an SPI master.

3.18.3 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock. It can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame

Table 16. STM32L073xx pin definition (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100						
-	8	E3	15	H1	PC0	I/O	FTf	-	LPTIM1_IN1, LCD_SEG18, EVENTOUT, TSC_G7_IO1, LPUART1_RX, I2C3_SCL	ADC_IN10
-	9	E2	16	J2	PC1	I/O	FTf	-	LPTIM1_OUT, LCD_SEG19, EVENTOUT, TSC_G7_IO2, LPUART1_TX, I2C3_SDA	ADC_IN11
-	10	F2	17	J3	PC2	I/O	FTf	-	LPTIM1_IN2, LCD_SEG20, SPI2_MISO/I2S2_MCK, TSC_G7_IO3	ADC_IN12
-	11	-	18	K2	PC3	I/O	FT	-	LPTIM1_ETR, LCD_SEG21, SPI2_MOSI/I2S2_SD, TSC_G7_IO4	ADC_IN13
8	12	F1	19	J1	VSSA	S	-	-	-	-
-	-	-	20	K1	VREF-	S	-	-	-	-
-	-	G1	21	L1	VREF+	S	-	-	-	-
9	13	H1	22	M1	VDDA	S	-	-	-	-
10	14	G2	23	L2	PA0	I/O	TC	-	TIM2_CH1, TSC_G1_IO1, USART2_CTS, TIM2_ETR, USART4_TX, COMP1_OUT	COMP1_INM, ADC_IN0, RTC_TAMP2/WKUP1
11	15	H2	24	M2	PA1	I/O	FT	-	EVENTOUT, LCD_SEG0, TIM2_CH2, TSC_G1_IO2, USART2_RTS_DE, TIM21_ETR, USART4_RX	COMP1_INP, ADC_IN1
12	16	F3	25	K3	PA2	I/O	FT	-	TIM21_CH1, LCD_SEG1, TIM2_CH3, TSC_G1_IO3, USART2_TX, LPUART1_TX, COMP2_OUT	COMP2_INM, ADC_IN2
13	17	G3	26	L3	PA3	I/O	FT	-	TIM21_CH2, LCD_SEG2, TIM2_CH4, TSC_G1_IO4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3

Table 16. STM32L073xx pin definition (continued)

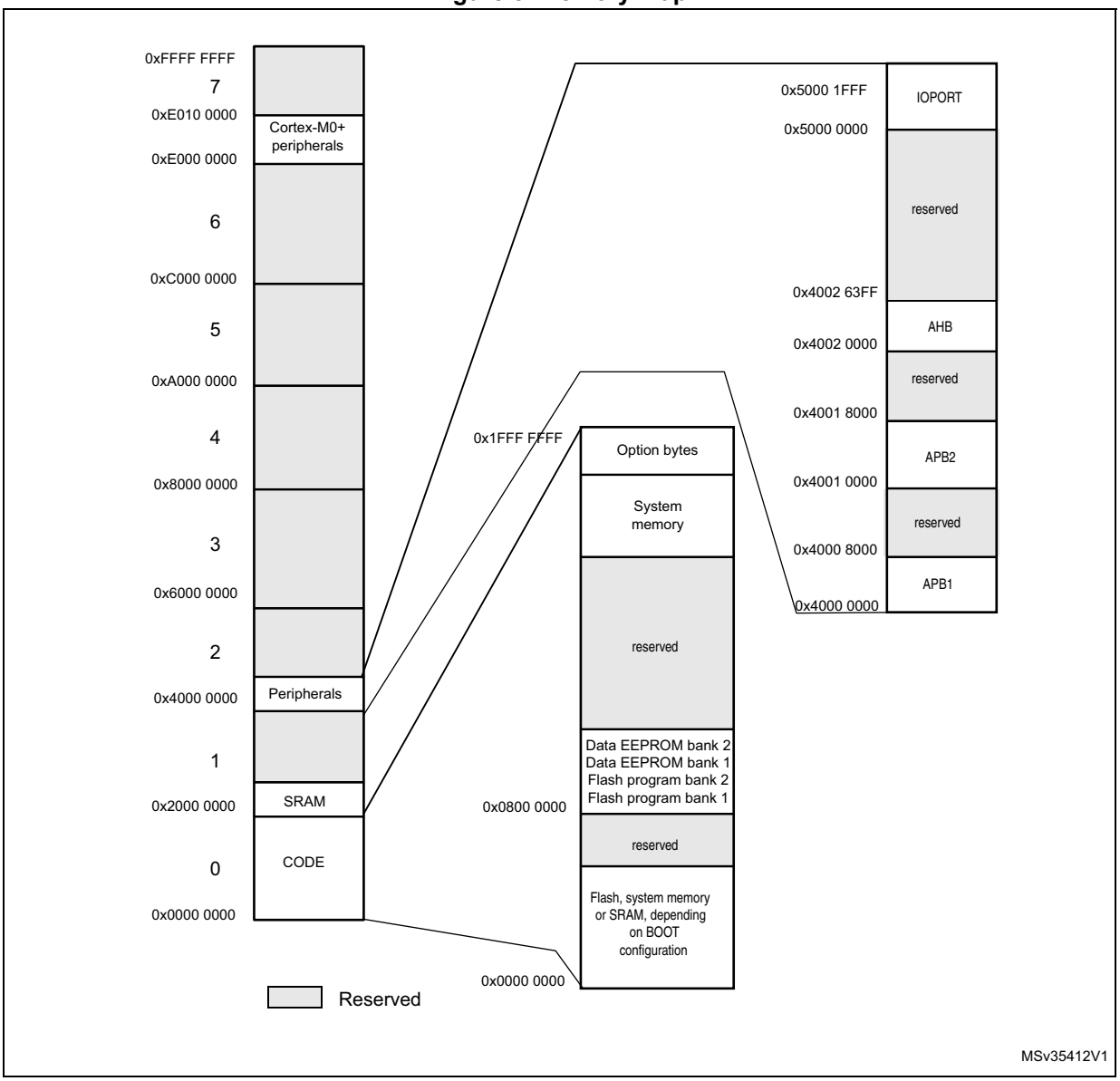
Pin number					Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100						
-	18	C2	27	E3	VSS	S	-	-	-	-
-	19	D2	28	H3	VDD	S	-	-	-	-
14	20	H3	29	M3	PA4	I/O	TC	(1)	SPI1_NSS, TSC_G2_IO1, USART2_CK, TIM22_ETR	COMP1_INM, COMP2_INM, ADC_IN4, DAC_OUT1
15	21	F4	30	K4	PA5	I/O	TC	-	SPI1_SCK, TIM2_ETR, TSC_G2_IO2, TIM2_CH1	COMP1_INM, COMP2_INM, ADC_IN5, DAC_OUT2
16	22	G4	31	L4	PA6	I/O	FT	-	SPI1_MISO, LCD_SEG3, TIM3_CH1, TSC_G2_IO3, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6
17	23	H4	32	M4	PA7	I/O	FT	-	SPI1_MOSI, LCD_SEG4, TIM3_CH2, TSC_G2_IO4, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	24	H5	33	K5	PC4	I/O	FT	-	EVENTOUT, LCD_SEG22, LPUART1_TX	ADC_IN14
-	25	H6	34	L5	PC5	I/O	FT	-	LCD_SEG23, LPUART1_RX, TSC_G3_IO1	ADC_IN15
18	26	F5	35	M5	PB0	I/O	FT	-	EVENTOUT, LCD_SEG5, TIM3_CH3, TSC_G3_IO2	LCD_VLCD3, ADC_IN8, VREF_OUT
19	27	G5	36	M6	PB1	I/O	FT	-	LCD_SEG6, TIM3_CH4, TSC_G3_IO3, LPUART1_RTS_DE	ADC_IN9, VREF_OUT
20	28	G6	37	L6	PB2	I/O	FT	-	LPTIM1_OUT, TSC_G3_IO4, I2C3_SMBA	LCD_VLCD1
-	-	-	38	M7	PE7	I/O	FT	-	LCD_SEG45, USART5_CK/USART5_RTS	-
-	-	-	39	L7	PE8	I/O	FT	-	LCD_SEG46, USART4_TX	-
-	-	-	40	M8	PE9	I/O	FT	-	TIM2_CH1, LCD_SEG47, TIM2_ETR, USART4_RX	-

Table 18. Alternate functions port B

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I 2C1/LCD/ TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/L PTIM1/TIM2/3/E VENTOUT/ SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2/I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/LPUART1/ COMP1/2/ TIM3
Port B	PB0	EVENTOUT	LCD_SEG5	TIM3_CH3	TSC_G3_IO2	-	-	-	-
	PB1	-	LCD_SEG6	TIM3_CH4	TSC_G3_IO3	LPUART1_RTS_DE	-	-	-
	PB2	-	-	LPTIM1_OUT	TSC_G3_IO4	-	-	-	I2C3_SMBA
	PB3	SPI1_SCK	LCD_SEG7	TIM2_CH2	TSC_G5_IO1	EVENTOUT	USART1_RTS_DE	USART5_TX	-
	PB4	SPI1_MISO	LCD_SEG8	TIM3_CH1	TSC_G5_IO2	TIM22_CH1	USART1_CTS	USART5_RX	I2C3_SDA
	PB5	SPI1_MOSI	LCD_SEG9	LPTIM1_IN1	I2C1_SMBA	TIM3_CH2/ TIM22_CH2	USART1_CK	USART5_CK/ USART5_RTS_D E	-
	PB6	USART1_TX	I2C1_SCL	LPTIM1_ETR	TSC_G5_IO3	-	-	-	-
	PB7	USART1_RX	I2C1_SDA	LPTIM1_IN2	TSC_G5_IO4	-	-	USART4_CTS	-
	PB8	-	LCD_SEG16	-	TSC_SYNC	I2C1_SCL	-	-	-
	PB9	-	LCD_COM3	EVENTOUT	-	I2C1_SDA	SPI2_NSS/ I2S2_WS	-	-
	PB10	-	LCD_SEG10	TIM2_CH3	TSC_SYNC	LPUART1_TX	SPI2_SCK	I2C2_SCL	LPUART1_RX
	PB11	EVENTOUT	LCD_SEG11	TIM2_CH4	TSC_G6_IO1	LPUART1_RX	-	I2C2_SDA	LPUART1_TX
	PB12	SPI2_NSS/I2S2_WS	LCD_SEG12	LPUART1_RTS_ DE	TSC_G6_IO2		I2C2_SMBA	EVENTOUT	-
	PB13	SPI2_SCK/I2S2_CK	LCD_SEG13	MCO	TSC_G6_IO3	LPUART1_CTS	I2C2_SCL	TIM21_CH1	-
	PB14	SPI2_MISO/ I2S2_MCK	LCD_SEG14	RTC_OUT	TSC_G6_IO4	LPUART1_RTS_DE	I2C2_SDA	TIM21_CH2	-
	PB15	SPI2_MOSI/ I2S2_SD	LCD_SEG15	RTC_REFIN	-	-	-	-	-

5 Memory mapping

Figure 8. Memory map



1. Refer to the STM32L073xx reference manual for details on the Flash memory organization for each memory size.

Table 24. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD} (2)	Total current into sum of all V_{DD} power lines (source)(1)	105	mA
ΣI_{VSS} (2)	Total current out of sum of all V_{SS} ground lines (sink)(1)	105	
ΣI_{VDD_USB}	Total current into V_{DD_USB} power lines (source)	25	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin except FTf pins	16	
	Output current sunk by FTf pins	22	
	Output current sourced by any I/O and control pin	-16	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins except PA11 and PA12(2)	90	
	Total output current sunk by PA11 and PA12	25	
	Total output current sourced by sum of all IOs and control pins(2)	-90	
$I_{INJ(PIN)}$	Injected current on FT, FFf, RST and B pins	-5/+0(3)	
	Injected current on TC pin	± 5(4)	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 23* for maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 23: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 25. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 26*.

Table 27. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	

Table 34. Current consumption in Sleep mode

Symbol	Parameter	Condition		f_{HCLK} (MHz)	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash memory switched OFF	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range3, Vcore=1.2 V VOS[1:0]=11	1	43,5	110	µA
				2	72	140	
				4	130	200	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	160	220	
				8	305	380	
				16	590	690	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	370	460	
				16	715	840	
				32	1650	2000	
		MSI clock	Range3, Vcore=1.2 V VOS[1:0]=11	0,065	18	93	
				0,524	31,5	110	
				4,2	140	230	
		HSI clock source (16 MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	665	850	
			Range1, Vcore=1.8 V VOS[1:0]=01	32	1750	2100	
	Supply current in Sleep mode, Flash memory switched ON	$f_{HSE} = f_{HCLK}$ up to 16MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range3, Vcore=1.2 V VOS[1:0]=11	1	57,5	130	
				2	84	160	
				4	150	220	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	170	240	
				8	315	400	
				16	605	710	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	380	470	
				16	730	860	
				32	1650	2000	
		MSI clock	Range3, Vcore=1.2 V VOS[1:0]=11	0,065	29,5	110	
				0,524	44,5	120	
				4,2	150	240	
		HSI clock source (16MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	680	930	
			Range1, Vcore=1.8 V VOS[1:0]=01	32	1750	2200	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Figure 16. I_{DD} vs V_{DD}, at T_A= 25 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS

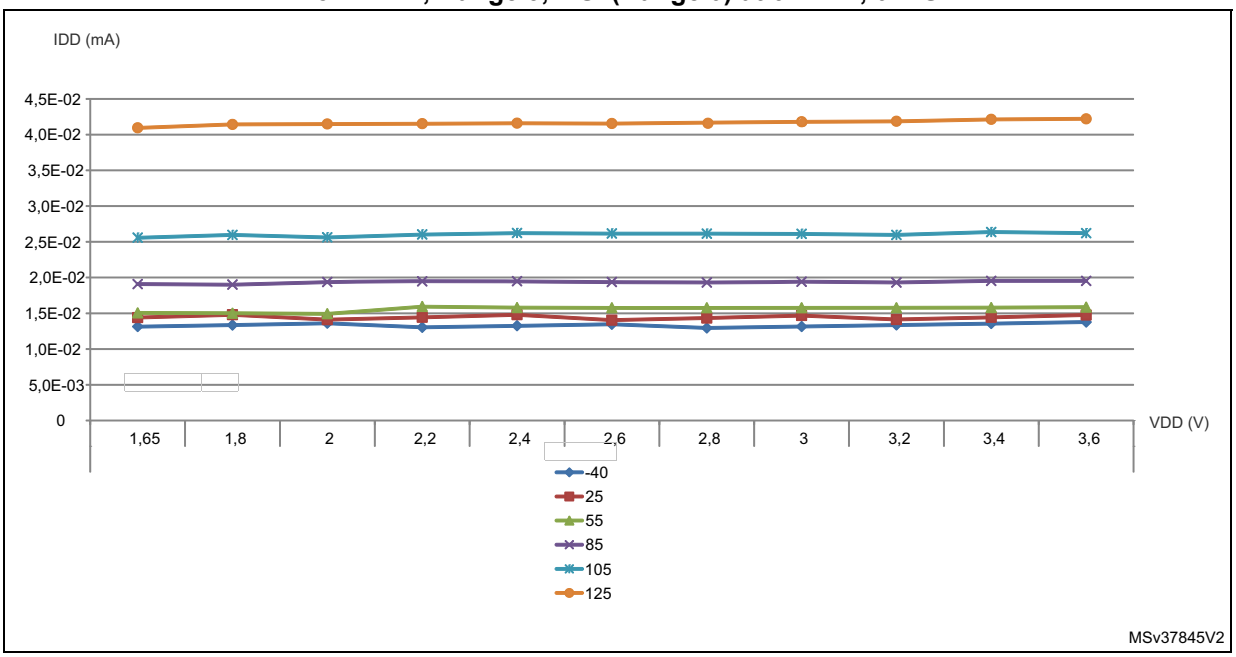


Table 36. Current consumption in Low-power sleep mode

Symbol	Parameter	Condition			Typ	Max (1)	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, code executed from Flash memory, V_{DD} from 1.65 to 3.6 V	MSI clock = 65 kHz, f_{HCLK}= 32 kHz, Flash memory OFF	T_A = −40 to 25°C	4,7	-	µA
			MSI clock = 65 kHz, f_{HCLK}= 32 kHz	T_A = −40 to 25°C	17	24	
				T_A = 85°C	19,5	30	
				T_A= 105°C	23	47	
				T_A= 125°C	32,5	70	
			MSI clock = 65 kHz, f_{HCLK}= 65 kHz	T_A= − 40 to 25°C	17	24	
				T_A= 85°C	20	31	
				T_A = 105°C	23,5	47	
				T_A = 125°C	32,5	70	
			MSI clock = 131kHz, f_{HCLK}= 131 kHz	T_A= − 40 to 25°C	19,5	27	
				T_A = 55°C	20,5	28	
				T_A = 85°C	22,5	33	
				T_A = 105°C	26	50	
				T_A= 125°C	35	73	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

Table 40. Peripheral current consumption in Run or Sleep mode(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB2	ADC1(2)	5.5	5	3.5	4	µA/MHz (f_{HCLK})
	SPI1	4	3	3	2.5	
	USART1	14.5	11.5	9.5	12	
	TIM21	7.5	6	5	5.5	
	TIM22	7	6	5	6	
	FIREWALL	1.5	1	1	0.5	
	DBGMCU	1.5	1	1	0.5	
	SYSCFG	2.5	2	2	1.5	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	µA/MHz (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GPIOD	1	0.5	0.5	0.5	
	GPIOE	8	6	5	6	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	µA/MHz (f_{HCLK})
	FLASH	0(3)	0(3)	0(3)	0(3)	
	DMA1	10	8	6.5	8.5	
	RNG	5.5	1	0.5	0.5	
	TSC	3	2.5	2	3	
All enabled		204	162	130	202	µA/MHz (f_{HCLK})
PWR		2.5	2	2	1	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals off an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is off for this measure.
3. Current consumption is negligible and close to 0 µA.

Table 54. Flash memory and data EEPROM endurance and retention (continued)

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
t_{RET}(2)	Data retention (program memory) after 10 kcycles at T_A = 85 °C	T_{RET} = +85 °C	30	years
	Data retention (EEPROM data memory) after 100 kcycles at T_A = 85 °C		30	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	T_{RET} = +105 °C	10	
	Data retention (EEPROM data memory) after 100 kcycles at T_A = 105 °C			
	Data retention (program memory) after 200 cycles at T_A = 125 °C	T_{RET} = +125 °C		
	Data retention (EEPROM data memory) after 2 kcycles at T_A = 125 °C			

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 55*. They are based on the EMS levels and classes defined in application note AN1709.

Table 55. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 57. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1.	C4	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

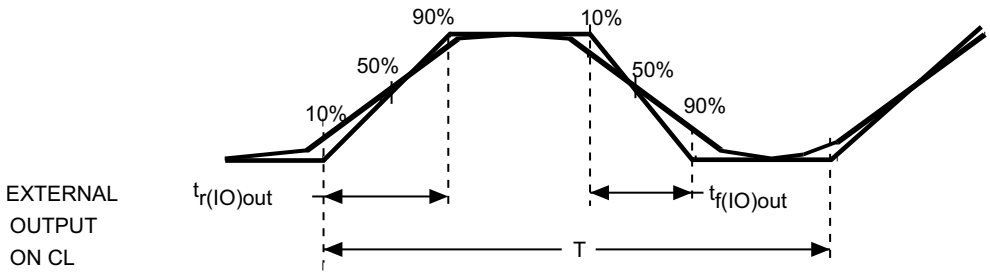
- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 58. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

Figure 26. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} , except when it is internally driven low (see *Table 63*).

Unless otherwise specified, the parameters given in *Table 63* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

Table 63. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$(1)	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V	-	-		
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	10%V_{DD}(2)	-	mV
R_{PU}	Weak pull-up equivalent resistor(3)	V_{IN} = V_{SS}	30	45	60	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design.
2. 200 mV minimum value
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

Table 67. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dOffset/dT(2)	Offset error temperature coefficient (code 0x800)	V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer off	-20	-10	0	µV/°C
		V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer on	0	20	50	
Gain(2)	Gain error(8)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer on	-	+0.1 / -0.2%	+0.2 / -0.5%	%
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer off	-	+0 / -0.2%	+0 / -0.4%	
dGain/dT(2)	Gain error temperature coefficient	V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer off	-10	-2	0	µV/°C
		V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer on	-40	-8	0	
TUE(2)	Total unadjusted error	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer on	-	12	30	LSB
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer off	-	8	12	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)(9)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	9	15	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ	-	-60	-35	dB

1. Guaranteed by characterization results.
2. Guaranteed by design, not tested in production.
3. Connected between DAC_OUT and V_{SSA}.
4. Difference between two consecutive codes - 1 LSB.
5. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.

Figure 38. USB timings: definition of data signal rise and fall time

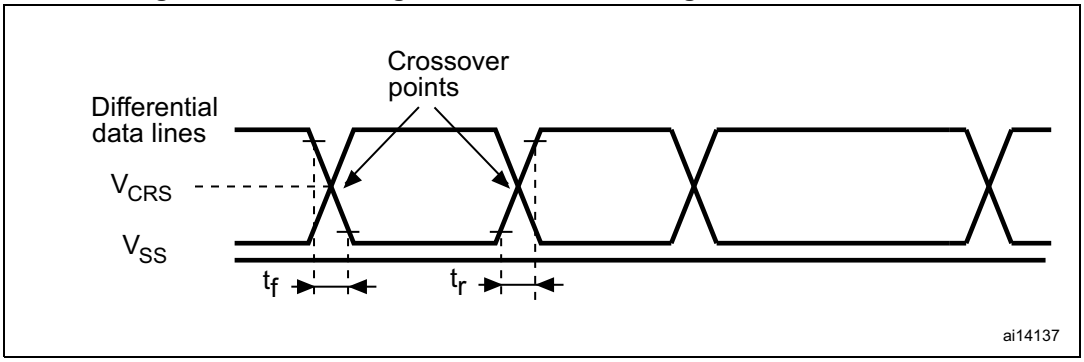


Table 81. USB: full speed electrical characteristics

Driver characteristics[1]					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time[2]	C_L = 50 pF	4	20	ns
t_f	Fall Time[2]	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

6.3.21 LCD controller

The devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

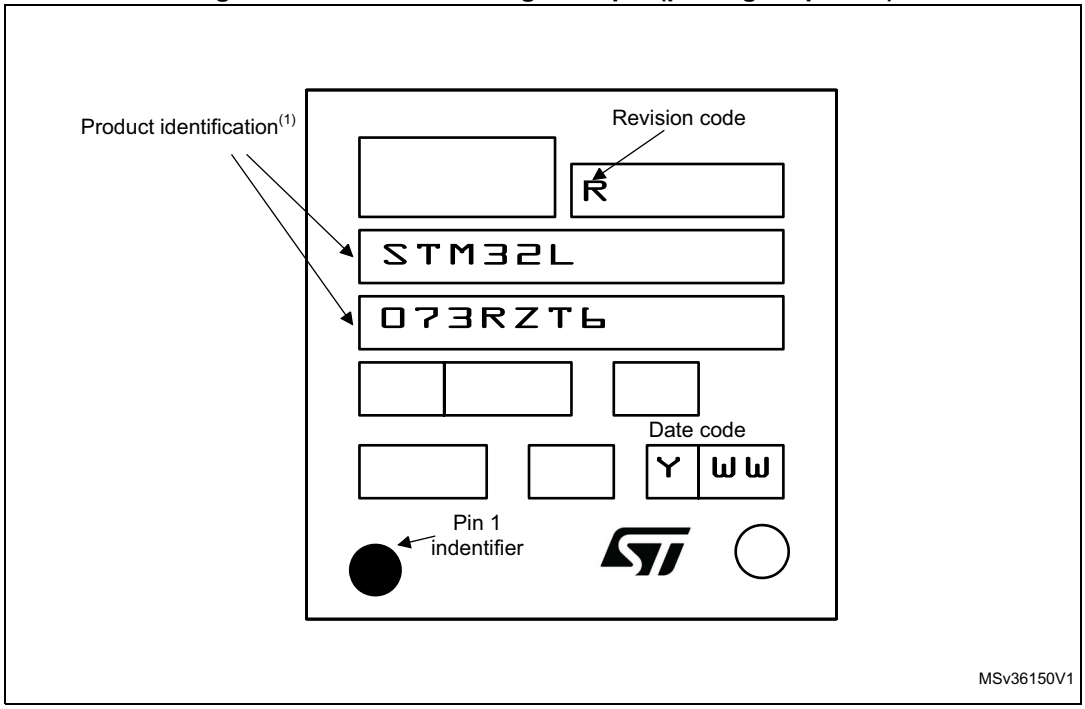
Table 82. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	µF

Device marking for LQFP64

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 47. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.