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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	3K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l073v8t6

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	Dynamic voltage scaling range	I/O operation	USB
V_{DD} = 1.65 to 1.71 V	ADC only, conversion time up to 570 ksps	Range 2 or range 3	Degraded speed performance	Not functional
V_{DD} = 1.71 to 1.8 V(1)	ADC only, conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Degraded speed performance	Functional(2)
V_{DD} = 1.8 to 2.0 V(1)	Conversion time up to 1.14 Msps	Range1, range 2 or range 3	Degraded speed performance	Functional(2)
V_{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional(2)
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional(2)

1. CPU frequency changes from initial to final must respect "fcpu initial <4*fcpu final". It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
2. To be USB compliant from the I/O voltage standpoint, the minimum V_{DD_USB} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (1)(2)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	--	Y	--	--		--	
Flash memory	O	O	O	O	--		--	
RAM	Y	Y	Y	Y	Y		--	
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	O	O	O	O	--		--	
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--		--	
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	(3)		--	
High Speed External (HSE)	O	O	O	O	--		--	
Low Speed Internal (LSI)	O	O	O	O	O		O	
Low Speed External (LSE)	O	O	O	O	O		O	
Multi-Speed Internal (MSI)	O	O	Y	Y	--		--	
Inter-Connect Controller	Y	Y	Y	Y	Y		--	
RTC	O	O	O	O	O	O	O	
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	O	O	O
LCD	O	O	O	O	O		--	
USB	O	O	--	--	--	O	--	
USART	O	O	O	O	O(4)	O	--	
LPUART	O	O	O	O	O(4)	O	--	
SPI	O	O	O	O	--		--	
I2C	O	O	O	O	O(5)	O	--	
ADC	O	O	--	--	--		--	

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)[1][2]

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
DAC	O	O	O	O	O		--	
Temperature sensor	O	O	O	O	O		--	
Comparators	O	O	O	O	O	O	--	
16-bit timers	O	O	O	O	--		--	
LPTIMER	O	O	O	O	O	O		
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	--		--	
Touch sensing controller (TSC)	O	O	--	--	--		--	
SysTick Timer	O	O	O	O			--	
GPIOs	O	O	O	O	O	O		2 pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs	3.5 µs		50 µs	
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 140 µA/MHz (from Flash memory)	Down to 37 µA/MHz (from Flash memory)	Down to 8 µA	Down to 4.5 µA	0.4 µA (No RTC) V_{DD}=1.8 V		0.28 µA (No RTC) V_{DD}=1.8 V	
					0.8 µA (with RTC) V_{DD}=1.8 V		0.65 µA (with RTC) V_{DD}=1.8 V	
					0.4 µA (No RTC) V_{DD}=3.0 V		0.29 µA (No RTC) V_{DD}=3.0 V	
					1 µA (with RTC) V_{DD}=3.0 V		0.85 µA (with RTC) V_{DD}=3.0 V	

1. Legend:
   "Y" = Yes (enable).
   "O" = Optional can be enabled/disabled by software)
   "-" = Not available
2. The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.
3. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
4. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
5. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 6. STM32L0xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2,TIM21, TIM22	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
USB	CRS/HSI48	the clock recovery system trims the HSI48 based on USB SOF	Y	Y	-	-	-
	TIM3	USB_SOF is channel input for calibration	Y	Y	-	-	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC,DAC	Conversion trigger	Y	Y	Y	Y	-

3.17 Timers and watchdogs

The ultra-low-power STM32L073xx devices include three general-purpose timers, one low-power timer (LPTIM), one basic timer, two watchdog timers and the SysTick timer.

Table 10 compares the features of the general-purpose and basic timers.

Table 10. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.17.1 General-purpose timers (TIM2, TIM3, TIM21 and TIM22)

There are four synchronizable general-purpose timers embedded in the STM32L073xx device (see *Table 10* for differences).

TIM2, TIM3

TIM2 and TIM3 are based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2/TIM3 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2/TIM3 have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2/TIM3, full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

Table 16. STM32L073xx pin definition (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100						
-	-	-	85	B7	PD4	I/O	FT	-	USART2_RTS_DE, SPI2_MOSI/I2S2_SD	-
-	-	-	86	A6	PD5	I/O	FT	-	USART2_TX	-
-	-	-	87	B6	PD6	I/O	FT	-	USART2_RX	-
-	-	-	88	A5	PD7	I/O	FT	-	USART2_CK, TIM21_CH2	-
39	55	A5	89	A8	PB3	I/O	FT	-	SPI1_SCK, LCD_SEG7, TIM2_CH2, TSC_G5_IO1, EVENTOUT, USART1_RTS_DE, USART5_TX	COMP2_INM
40	56	A4	90	A7	PB4	I/O	FTf	-	SPI1_MISO, LCD_SEG8, TIM3_CH1, TSC_G5_IO2, TIM22_CH1, USART1_CTS, USART5_RX, I2C3_SDA	COMP2_INP
41	57	C4	91	C5	PB5	I/O	FT	-	SPI1_MOSI, LCD_SEG9, LPTIM1_IN1, I2C1_SMBA, TIM3_CH2/TIM22_CH2, USART1_CK, USART5_CK/USART5_RTS	COMP2_INP
42	58	D3	92	B5	PB6	I/O	FTf	-	USART1_TX, I2C1_SCL, LPTIM1_ETR, TSC_G5_IO3	COMP2_INP
43	59	C3	93	B4	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2, TSC_G5_IO4, USART4_CTS	COMP2_INP, PVD_IN
44	60	B4	94	A4	BOOT0	I		-	-	-
45	61	B3	95	A3	PB8	I/O	FTf	-	LCD_SEG16, TSC_SYNC, I2C1_SCL	-
46	62	A3	96	B3	PB9	I/O	FTf	-	LCD_COM3, EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-
-	-	-	97	C3	PE0	I/O	FT	-	LCD_SEG36, EVENTOUT	-
-	-	-	98	A2	PE1	I/O	FT	-	LCD_SEG37, EVENTOUT	-

Table 18. Alternate functions port B

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I 2C1/LCD/ TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/L PTIM1/TIM2/3/E VENTOUT/ SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2/I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/LPUART1/ COMP1/2/ TIM3
Port B	PB0	EVENTOUT	LCD_SEG5	TIM3_CH3	TSC_G3_IO2	-	-	-	-
	PB1	-	LCD_SEG6	TIM3_CH4	TSC_G3_IO3	LPUART1_RTS_DE	-	-	-
	PB2	-	-	LPTIM1_OUT	TSC_G3_IO4	-	-	-	I2C3_SMBA
	PB3	SPI1_SCK	LCD_SEG7	TIM2_CH2	TSC_G5_IO1	EVENTOUT	USART1_RTS_DE	USART5_TX	-
	PB4	SPI1_MISO	LCD_SEG8	TIM3_CH1	TSC_G5_IO2	TIM22_CH1	USART1_CTS	USART5_RX	I2C3_SDA
	PB5	SPI1_MOSI	LCD_SEG9	LPTIM1_IN1	I2C1_SMBA	TIM3_CH2/ TIM22_CH2	USART1_CK	USART5_CK/ USART5_RTS_D E	-
	PB6	USART1_TX	I2C1_SCL	LPTIM1_ETR	TSC_G5_IO3	-	-	-	-
	PB7	USART1_RX	I2C1_SDA	LPTIM1_IN2	TSC_G5_IO4	-	-	USART4_CTS	-
	PB8	-	LCD_SEG16	-	TSC_SYNC	I2C1_SCL	-	-	-
	PB9	-	LCD_COM3	EVENTOUT	-	I2C1_SDA	SPI2_NSS/ I2S2_WS	-	-
	PB10	-	LCD_SEG10	TIM2_CH3	TSC_SYNC	LPUART1_TX	SPI2_SCK	I2C2_SCL	LPUART1_RX
	PB11	EVENTOUT	LCD_SEG11	TIM2_CH4	TSC_G6_IO1	LPUART1_RX	-	I2C2_SDA	LPUART1_TX
	PB12	SPI2_NSS/I2S2_WS	LCD_SEG12	LPUART1_RTS_ DE	TSC_G6_IO2		I2C2_SMBA	EVENTOUT	-
	PB13	SPI2_SCK/I2S2_CK	LCD_SEG13	MCO	TSC_G6_IO3	LPUART1_CTS	I2C2_SCL	TIM21_CH1	-
	PB14	SPI2_MISO/ I2S2_MCK	LCD_SEG14	RTC_OUT	TSC_G6_IO4	LPUART1_RTS_DE	I2C2_SDA	TIM21_CH2	-
	PB15	SPI2_MOSI/ I2S2_SD	LCD_SEG15	RTC_REFIN	-	-	-	-	-

Table 26. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Temperature range	Maximum power dissipation (range 6)	–40	85	°C
		Maximum power dissipation (range 7)	–40	105	
		Maximum power dissipation (range 3)	–40	125	
T_J	Junction temperature range (range 6)	-40 °C ≤ T_A ≤ 85 °	–40	105	
	Junction temperature range (range 7)	-40 °C ≤ T_A ≤ 105 °C	–40	125	
	Junction temperature range (range 3)	-40 °C ≤ T_A ≤ 125 °C	–40	130	

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and normal operation.
2. V_{DD_USB} must respect the following conditions:

- When V_{DD} is powered on (V_{DD} < V_{DD_min}), V_{DD_USB} should be always lower than V_{DD}.
- When V_{DD} is powered down (V_{DD} < V_{DD_min}), V_{DD_USB} should be always lower than V_{DD}.
- In operating mode, V_{DD_USB} could be lower or higher V_{DD}.
- If the USB is not used, V_{DD_USB} must range from V_{DD_min} to V_{DD_max} to be able to use PA11 and PA12 as standard I/Os.

3. To sustain a voltage higher than V_{DD}+0.3V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 90: Thermal characteristics on page 134*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 26*.

Table 27. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	

Table 29. Embedded internal reference voltage(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LPBUF}(4)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(4)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(4)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(4)	3/4 reference voltage	-	74	75	76	

1. Refer to *Table 41: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption (I_{REFINT}).
2. Guaranteed by test in production.
3. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
4. Guaranteed by design.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is on, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 43: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in *Table 51*, *Table 26* and *Table 27* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

Table 32. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Condition		f_{HCLK} (MHz)	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode code executed from RAM, Flash memory switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range3, Vcore=1.2 V VOS[1:0]=11	1	175	230	µA
				2	315	360	
				4	570	630	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	0,71	0,78	mA
				8	1,35	1,6	
				16	2,7	3	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	1,7	1,9	
				16	3,2	3,7	
				32	6,65	7,1	
		MSI clock	Range3, Vcore=1.2 V VOS[1:0]=11	0,065	38	98	µA
				0,524	105	160	
				4,2	615	710	
		HSI clock source (16 MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	2,85	3	mA
			Range1, Vcore=1.8 V VOS[1:0]=01	32	6,85	7,3	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 33. Current consumption in Run mode vs code type, code with data processing running from RAM(1)

Symbol	Parameter	Conditions			f_{HCLK}	Typ	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash memory switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL on)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	570	µA
				CoreMark		670	
				Fibonacci		410	
				while(1)		375	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	6,65	mA
				CoreMark		6,95	
				Fibonacci		5,9	
				while(1)		5,2	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 42. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	7	8	Number of clock cycles
$t_{WUSLEEP\_LP}$	Wakeup from Low-power sleep mode, f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash memory enabled	7	8	
		f_{HCLK} = 262 kHz Flash memory switched OFF	9	10	
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz	5.0	8	µs
		$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 1	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 2	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 3	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	7.3	13	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	13	23	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	28	38	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	51	65	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	100	120	
		f_{HCLK} = MSI = 65 kHz	190	260	
		$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode, code running from RAM	$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	7.9	10	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz	4.7	8	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	65	130	
	Wakeup from Standby mode FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	2.2	3	ms

Table 54. Flash memory and data EEPROM endurance and retention (continued)

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
t_{RET}(2)	Data retention (program memory) after 10 kcycles at T_A = 85 °C	T_{RET} = +85 °C	30	years
	Data retention (EEPROM data memory) after 100 kcycles at T_A = 85 °C		30	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	T_{RET} = +105 °C	10	
	Data retention (EEPROM data memory) after 100 kcycles at T_A = 105 °C			
	Data retention (program memory) after 200 cycles at T_A = 125 °C	T_{RET} = +125 °C		
	Data retention (EEPROM data memory) after 2 kcycles at T_A = 125 °C			

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 55*. They are based on the EMS levels and classes defined in application note AN1709.

Table 55. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

6.3.16 DAC electrical specifications

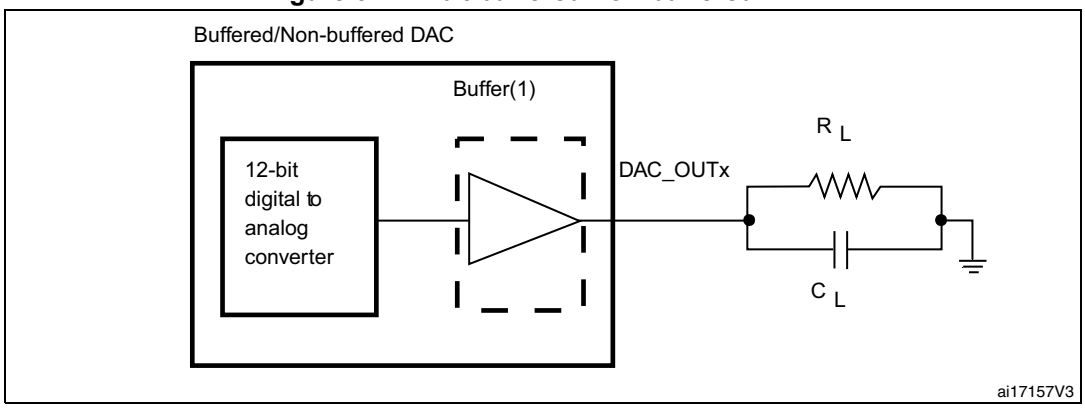
Data guaranteed by design, not tested in production, unless otherwise specified.

Table 67. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}	1.8	-	3.6	V
V_{REF-}	Lower reference voltage	-	V_{SSA}			V
$I_{DDVREF+}$(1)	Current consumption on V_{REF+} supply V_{REF+} = 3.3 V	No load, middle code (0x800)	-	130	220	µA
		No load, worst code (0x000)	-	220	350	
I_{DDA} (2)	Current consumption on V_{DDA} supply, V_{DDA} = 3.3 V	No load, middle code (0x800)	-	210	320	µA
		No load, worst code (0xF1C)	-	320	520	
R_L(3)	Resistive load	DAC output buffer on	5	-	-	kΩ
C_L(3)	Capacitive load		-	-	50	pF
R_O	Output impedance	DAC output buffer off	12	16	20	kΩ
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON	0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF	0.5	-	V_{REF+} – 1LSB	mV
DNL(2)	Differential non linearity(4)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer on	-	1.5	3	LSB
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer off	-	1.5	3	
INL(2)	Integral non linearity(5)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer on	-	2	4	
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer off	-	2	4	
Offset(2)	Offset error at code 0x800 (6)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer on	-	±10	±25	
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer off	-	±5	±8	
Offset1(2)	Offset error at code 0x001(7)	No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer off	-	±1.5	±5	

6. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}/2$.
7. Difference between the value measured at Code (0x001) and the ideal value.
8. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is off, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is on.
9. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 32. 12-bit buffered/non-buffered DAC



6.3.17 Temperature sensor characteristics

Table 68. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C, V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

Table 69. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{130}	Voltage at 130°C ±5°C(2)	640	670	700	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(4)(3)	ADC sampling time when reading the temperature	10	-	-	

1. Guaranteed by characterization results.
2. Measured at V_{DD} = 3 V ±10 mV. V130 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.
4. Shortest sampling time can be determined in the application by multiple iterations.

6.3.19 Timer characteristics

TIM timer characteristics

The parameters given in the *Table 72* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 72. TIMx characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-		16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM6, TIM21, and TIM22 timers.

6.3.20 Communications interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I^2C timing requirements are guaranteed by design when the I^2C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All I^2C SDA and SCL I/Os embed an analog filter (see *Table 73* for the analog filter characteristics).

Table 76. SPI characteristics in voltage Range 2 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	8	MHz
		Slave mode Transmitter $1.65<V_{DD}<3.6V$			8	
		Slave mode Transmitter $2.7<V_{DD}<3.6V$			8(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	11	-	-	
$t_{h(SI)}$		Slave mode	4.5	-	-	
$t_{a(SO}$	Data output access time	Slave mode	18	-	52	
$t_{dis(SO)}$	Data output disable time	Slave mode	12	-	42	
$t_{v(SO)}$	Data output valid time	Slave mode	-	20	56.5	
$t_{v(MO)}$		Master mode	-	5	9	
$t_{h(SO)}$	Data output hold time	Slave mode	13	-	-	
$t_{h(MO)}$		Master mode	3	-	-	

1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 38. USB timings: definition of data signal rise and fall time

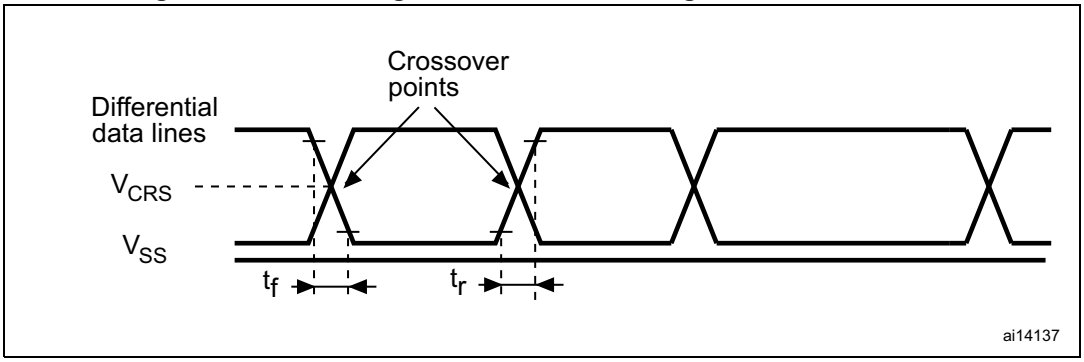


Table 81. USB: full speed electrical characteristics

Driver characteristics[1]					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time[2]	C_L = 50 pF	4	20	ns
t_f	Fall Time[2]	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

6.3.21 LCD controller

The devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 82. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	µF

Table 89. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.