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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l073vbt7tr

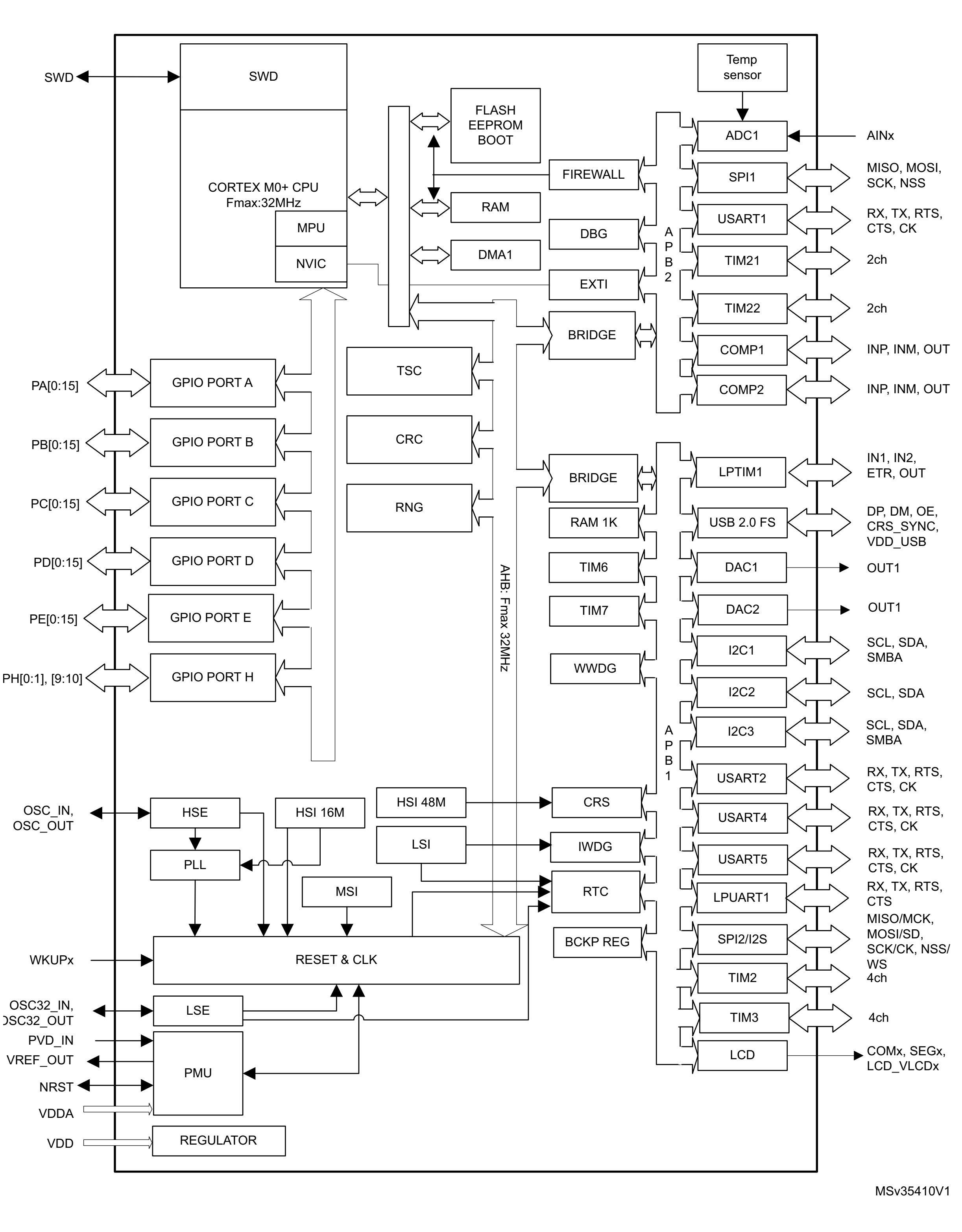
2.1 Device overview

Table 2. Ultra-low-power STM32L073xxx device features and peripheral counts

Peripheral		STM32L073 V8	STM32L073 CB	STM32L073 VB	STM32L073 RB	STM32L073 CZ	STM32L073 VZ	STM32L073 RZ
Flash (Kbytes)		64 Kbytes	128 Kbytes			192 Kbytes		
Data EEPROM (Kbytes)		3 Kbytes	6 Kbytes					
RAM (Kbytes)		20 Kbytes						
Timers	**General-purpose**	4						
	Basic	2						
	LPTIMER	1						
RTC/SYSTICK/IWDG/WWDG		1/1/1/1						
Commu-nication interfaces	**SPI/I2S**	6(4)[1]/1						
	I^2C	3						
	USART	4						
	LPUART	1						
	USB/(VDD_USB)	1/(1)						
GPIOs		84	37	84	51[2]	37	84	51[2]
Clocks: HSE/LSE/HSI/MSI/LSI		1/1/1/1/1						
12-bit synchronized ADC Number of channels		1 16	1 10	1 16[2]		1 10	1 16[2]	
12-bit DAC Number of channels		2 2						
LCD COM x SEG		1 4x52 or 8x48	1 4x18	1 4x52 or 8x48	1 4x32 or 8x28[2]	1 4x18	1 4x52 or 8x48	1 4x32 or 8x28[2]
Comparators		2						
Capacitive sensing channels		24	17	24	24[2]	17	24	24[2]
Max. CPU frequency		32 MHz						
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 to 3.6 V without BOR option						
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C						
Packages		LQFP100 UFBGA100	LQFP48	LQFP100 UFBGA100	LQFP64, TFBGA64	LQFP48	LQFP100 UFBGA100	LQFP64, TFBGA64

1. 4 SPI interfaces are USARTs operating in SPI master mode.
2. TFBGA64 has one GPIO, one ADC input, one capacitive sensing channel and one COMxSEG (4x31 or 8x27) less than LQFP64.

Figure 1. STM32L073xx block diagram



- **Stop mode without RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

  The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode. The LCD is not stopped automatically by entering Stop mode.

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)(1)(2)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
DAC	O	O	O	O	O		--	
Temperature sensor	O	O	O	O	O		--	
Comparators	O	O	O	O	O	O	--	
16-bit timers	O	O	O	O	--		--	
LPTIMER	O	O	O	O	O	O		
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	--		--	
Touch sensing controller (TSC)	O	O	--	--	--		--	
SysTick Timer	O	O	O	O			--	
GPIOs	O	O	O	O	O	O		2 pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs	3.5 µs		50 µs	
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 140 µA/MHz (from Flash memory)	Down to 37 µA/MHz (from Flash memory)	Down to 8 µA	Down to 4.5 µA	0.4 µA (No RTC) V_{DD}=1.8 V		0.28 µA (No RTC) V_{DD}=1.8 V	
					0.8 µA (with RTC) V_{DD}=1.8 V		0.65 µA (with RTC) V_{DD}=1.8 V	
					0.4 µA (No RTC) V_{DD}=3.0 V		0.29 µA (No RTC) V_{DD}=3.0 V	
					1 µA (with RTC) V_{DD}=3.0 V		0.85 µA (with RTC) V_{DD}=3.0 V	

1. Legend:
   "Y" = Yes (enable).
   "O" = Optional can be enabled/disabled by software)
   "-" = Not available
2. The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.
3. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
4. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
5. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.3 ARM® Cortex®-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L073xx are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L073xx embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS)**

  This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

  Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.18.4 Serial peripheral interface (SPI)/Inter-integrated sound (I2S)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The USARTs with synchronous capability can also be used as SPI master.

One standard I2S interfaces (multiplexed with SPI2) is available. It can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When the I2S interfaces is configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The SPIs can be served by the DMA controller.

Refer to *Table 14* for the differences between SPI1 and SPI2.

Table 14. SPI/I2S implementation

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
I2S mode	-	X
TI mode	X	X

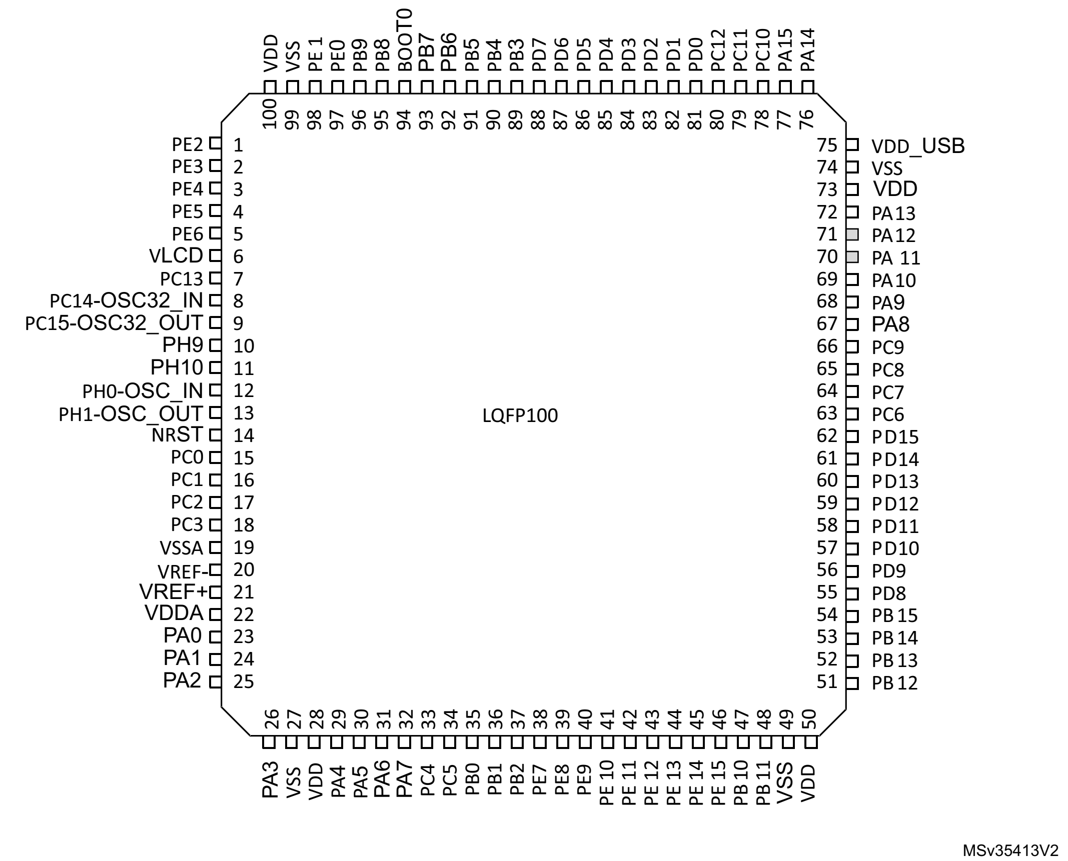
1. X = supported.

3.18.5 Universal serial bus (USB)

The STM32L073xx embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

4 Pin descriptions

Figure 3. STM32L073xx LQFP100 pinout - 14 x 14 mm



1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Table 16. STM32L073xx pin definition (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100						
-	-	-	41	L8	PE10	I/O	FT	-	TIM2_CH2, LCD_SEG40, USART5_TX	-
-	-	-	42	M9	PE11	I/O	FT	-	TIM2_CH3, USART5_RX	LCD_VLCD2
-	-	-	43	L9	PE12	I/O	FT	-	TIM2_CH4, SPI1_NSS	LCD_VLCD3
-	-	-	44	M10	PE13	I/O	FT	-	LCD_SEG41, SPI1_SCK	-
-	-	-	45	M11	PE14	I/O	FT	-	LCD_SEG42, SPI1_MISO	-
-	-	-	46	M12	PE15	I/O	FT	-	LCD_SEG43, SPI1_MOSI	-
21	29	G7	47	L10	PB10	I/O	FT	-	LCD_SEG10, TIM2_CH3, TSC_SYNC, LPUART1_TX, SPI2_SCK, I2C2_SCL, LPUART1_RX	-
22	30	H7	48	L11	PB11	I/O	FT	-	EVENTOUT, LCD_SEG11, TIM2_CH4, TSC_G6_IO1, LPUART1_RX, I2C2_SDA, LPUART1_TX	-
23	31	D6	49	F12	VSS	S		-	-	-
24	32	E5	50	G12	VDD	S		-	-	-
25	33	H8	51	L12	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LCD_SEG12, LPUART1_RTS_DE, TSC_G6_IO2, I2C2_SMBA, EVENTOUT	LCD_VLCD2
26	34	G8	52	K12	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, LCD_SEG13, MCO, TSC_G6_IO3, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
27	35	F8	53	K11	PB14	I/O	FTf	-	SPI2_MISO/I2S2_MCK, LCD_SEG14, RTC_OUT, TSC_G6_IO4, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
28	36	F7	54	K10	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD, LCD_SEG15, RTC_REFIN	-
-	-	-	55	K9	PD8	I/O	FT	-	LPUART1_TX, LCD_SEG28	-

Table 16. STM32L073xx pin definition (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100						
47	63	D4	99	D3	VSS	S	-	-	-	-
48	64	E4	100	C4	VDD	S	-	-	-	-

1. PA4 offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.
2. These pins are powered by VDD_USB. For all characteristics that refer to V_{DD}, V_{DD_USB} must be used instead.

Table 24. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}(2)	Total current into sum of all V_{DD} power lines (source)(1)	105	mA
ΣI_{VSS}(2)	Total current out of sum of all V_{SS} ground lines (sink)(1)	105	mA
ΣI_{VDD_USB}	Total current into V_{DD_USB} power lines (source)	25	mA
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	mA
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	mA
I_{IO}	Output current sunk by any I/O and control pin except FTf pins	16	mA
I_{IO}	Output current sunk by FTf pins	22	mA
I_{IO}	Output current sourced by any I/O and control pin	-16	mA
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins except PA11 and PA12(2)	90	mA
$\Sigma I_{IO(PIN)}$	Total output current sunk by PA11 and PA12	25	mA
$\Sigma I_{IO(PIN)}$	Total output current sourced by sum of all IOs and control pins(2)	-90	mA
$I_{INJ(PIN)}$	Injected current on FT, FFf, RST and B pins	-5/+0(3)	mA
$I_{INJ(PIN)}$	Injected current on TC pin	± 5(4)	mA
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	mA

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 23* for maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 23: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 25. Thermal characteristics

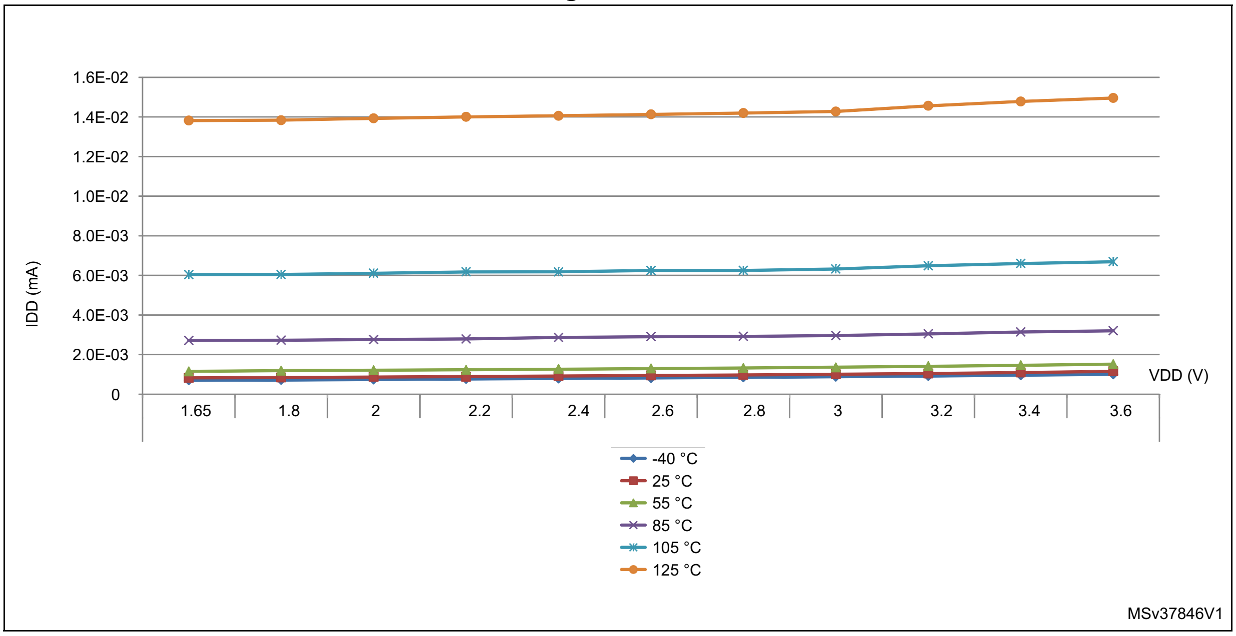
Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 37. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max[1]	Unit
I_{DD} (Stop)	Supply current in Stop mode	T_A = − 40 to 25°C	0,43	1,00	µA
		T_A = 55°C	0,735	2,50	
		T_A= 85°C	2,25	4,90	
		T_A = 105°C	5,3	13,00	
		T_A = 125°C	12,5	28,00	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

Figure 17. I_{DD} vs V_{DD}, at T_A= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive



6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

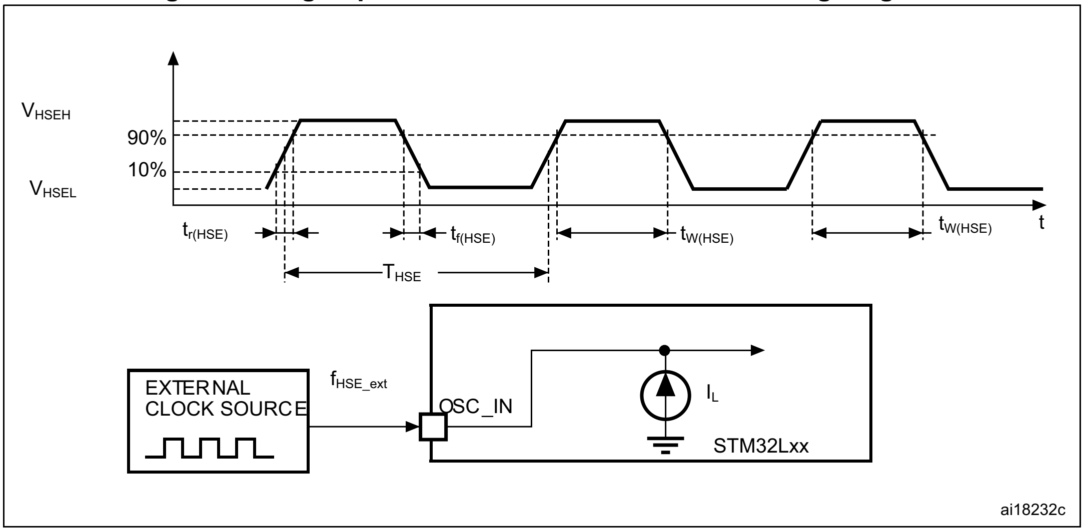
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 19*.

Table 43. High-speed external user clock characteristics[(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance		-	2.6	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 19. High-speed external clock source AC timing diagram



6.3.7 Internal clock source characteristics

The parameters given in *Table 47* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

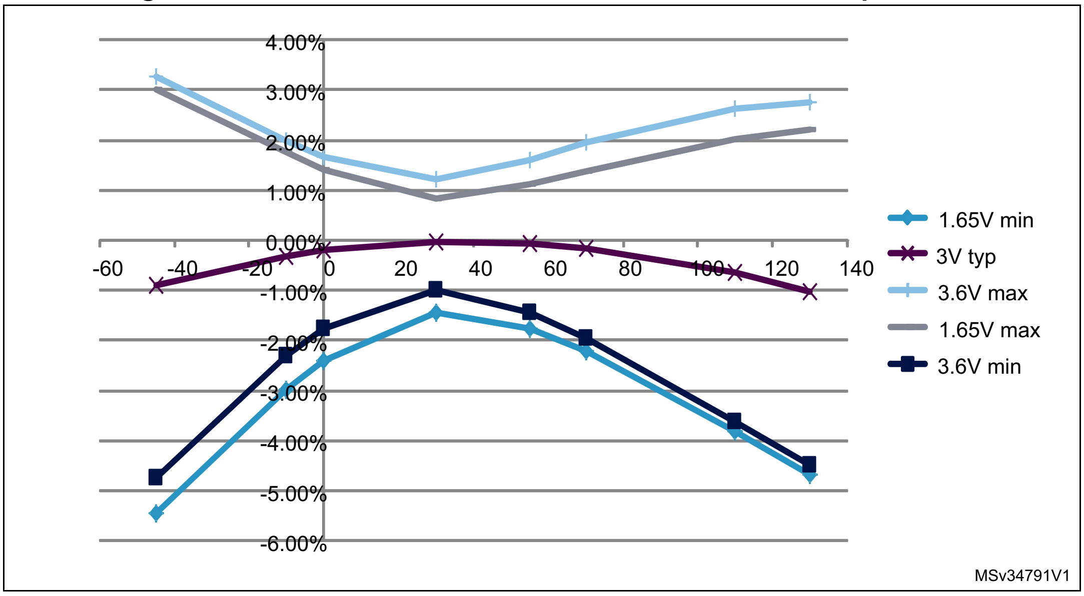
High-speed internal 16 MHz (HSI16) RC oscillator

Table 47. 16 MHz HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
TRIM(1)(2)	HSI16 user-trimmed resolution	Trimming code is not a multiple of 16	-	± 0.4	0.7	%
		Trimming code is a multiple of 16	-	-	± 1.5	%
ACC_{HSI16} (2)	Accuracy of the factory-calibrated HSI16 oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1(3)	-	1(3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = − 40 to 125 °C	-5.45	-	3.25	%
$t_{SU(HSI16)}$(2)	HSI16 oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI16)}$(2)	HSI16 oscillator power consumption	-	-	100	140	µA

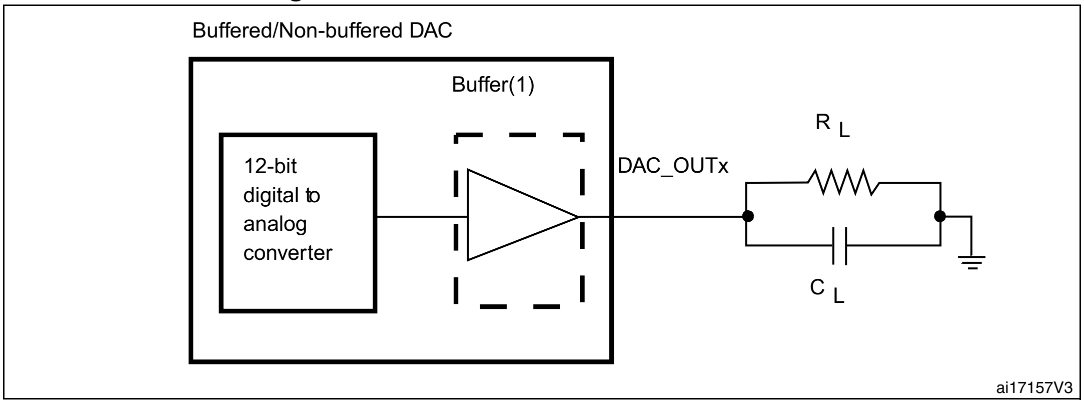
1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Figure 23. HSI16 minimum and maximum value versus temperature



6. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}/2$.
7. Difference between the value measured at Code (0x001) and the ideal value.
8. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is off, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is on.
9. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 32. 12-bit buffered/non-buffered DAC



6.3.17 Temperature sensor characteristics

Table 68. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C, V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

Table 69. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{130}	Voltage at 130°C ±5°C(2)	640	670	700	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(4)(3)	ADC sampling time when reading the temperature	10	-	-	µs

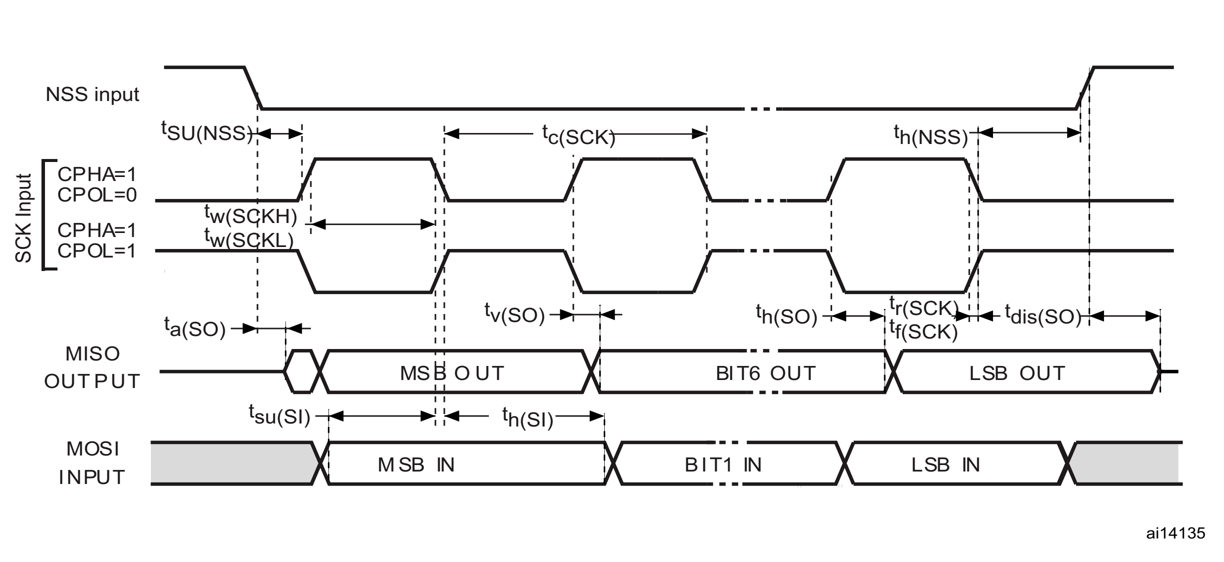
1. Guaranteed by characterization results.
2. Measured at V_{DD} = 3 V ±10 mV. V130 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.
4. Shortest sampling time can be determined in the application by multiple iterations.

Table 76. SPI characteristics in voltage Range 2 [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	8	MHz
		Slave mode Transmitter $1.65<V_{DD}<3.6V$			8	
		Slave mode Transmitter $2.7<V_{DD}<3.6V$			8[2]	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	11	-	-	
$t_{h(SI)}$		Slave mode	4.5	-	-	
$t_{a(SO}$	Data output access time	Slave mode	18	-	52	
$t_{dis(SO)}$	Data output disable time	Slave mode	12	-	42	
$t_{v(SO)}$	Data output valid time	Slave mode	-	20	56.5	
$t_{v(MO)}$		Master mode	-	5	9	
$t_{h(SO)}$	Data output hold time	Slave mode	13	-	-	
$t_{h(MO)}$		Master mode	3	-	-	

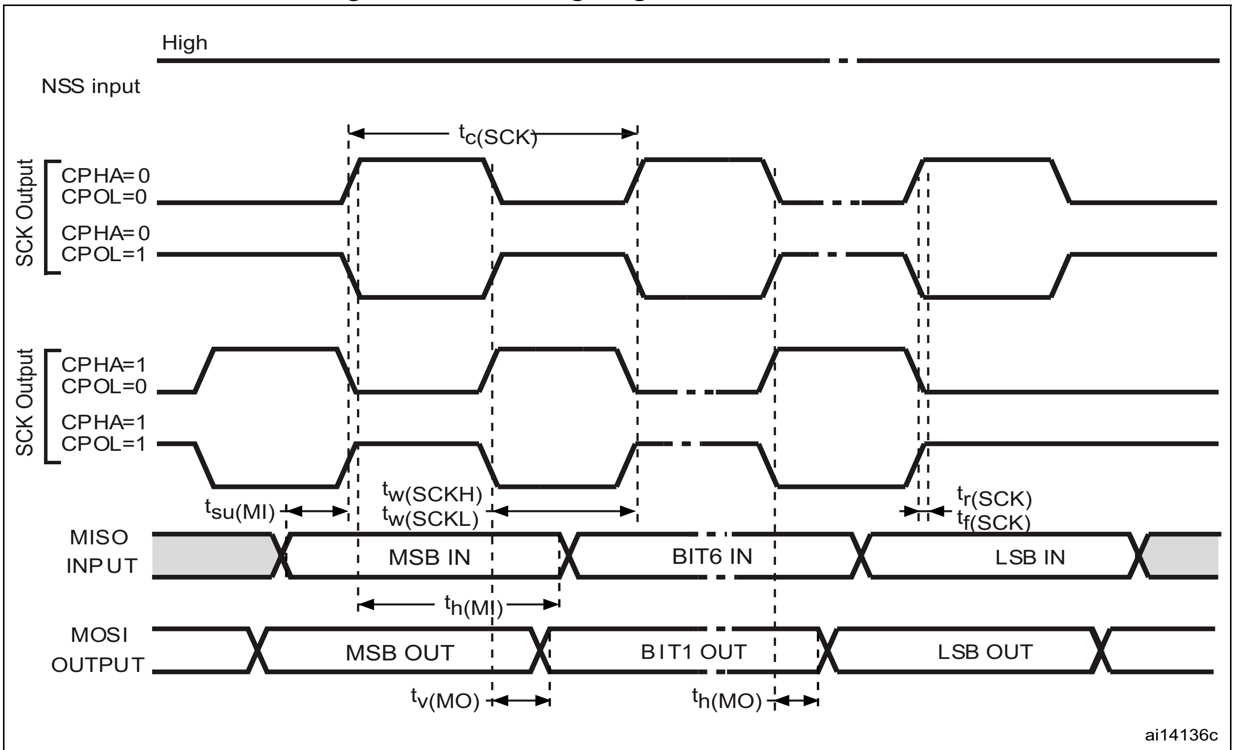
1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

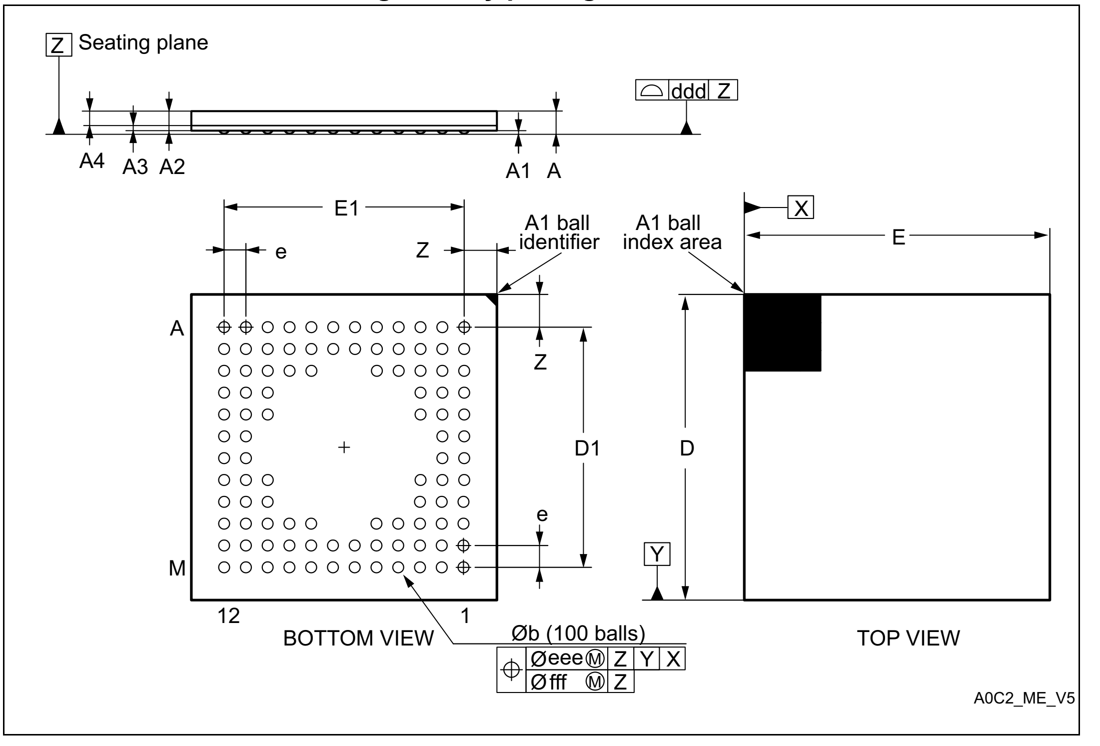
Figure 35. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

7.2 UFBGA100 package information

Figure 42. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



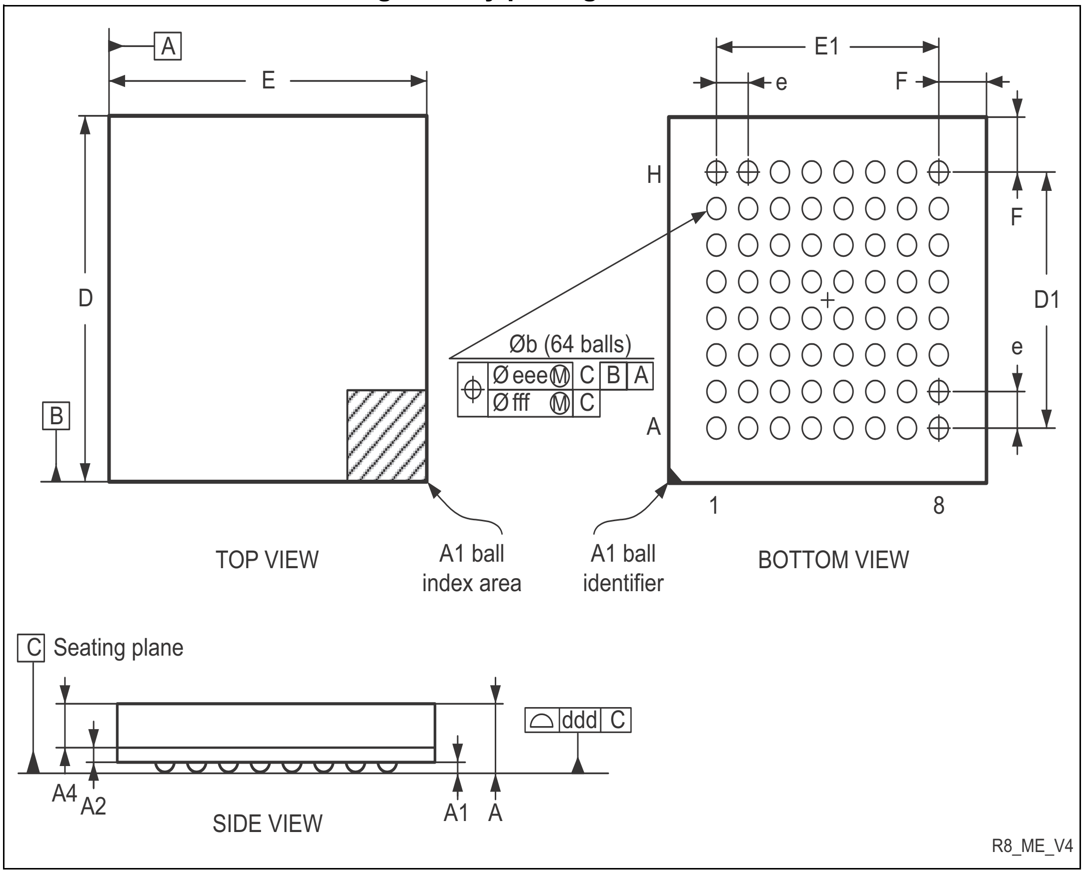
1. Drawing is not to scale.

Table 84. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

7.4 TFBGA64 package information

Figure 48. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 87. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-

9 Revision history

Table 92. Document revision history

Date	Revision	Changes
03-Aug-2015	1	Initial release
26-Oct-2015	2	Changed confidentiality level to public. Updated datasheet status to “production data”. Modified ultra-low-power platform features on cover page. Changed number of GPIOs for LQFP48 for 37 in *Table 2: Ultra-low-power STM32L073xxx device features and peripheral counts*. Changed LCD_VLCD1 into LCD_VLCD2 in *Section 3.13.2: VLCD voltage monitoring*. In *Section 6: Electrical characteristics*, updated notes related to values guaranteed by characterization. Updated $\lvert\Delta V_{SS}\rvert$ definition to include V_{REF-} in *Table 23: Voltage characteristics*. Added ΣV_{DD_USB} and updated $\Sigma I_{IO(PIN)}$ in *Figure 24: Current characteristics*. Updated *Table 56: EMI characteristics*. Updated f_{TRIG} and V_{AIN} maximum value, added V_{REF+} and V_{REF-} in *Table 64: ADC characteristics*. Updated *Section 7.2: UFBGA100 package information*. Updated *Figure 53: LQFP48 marking example (package top view)*.