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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l073vzt3

3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 6. STM32L0xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2,TIM21, TIM22	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
USB	CRS/HSI48	the clock recovery system trims the HSI48 based on USB SOF	Y	Y	-	-	-
	TIM3	USB_SOF is channel input for calibration	Y	Y	-	-	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC,DAC	Conversion trigger	Y	Y	Y	Y	-

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.5 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**

  To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**

  Clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management**

  To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**

  Three different clock sources can be used to drive the master clock SYSCLK:
  - 1-25 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLLMultispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**

  Two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock source**

  The LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source**

  A 48 MHz clock trimmed through the USB SOF or LSE supplies the USB interface.

3.10 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, LPUART, general-purpose timers, DAC, and ADC.

3.11 Liquid crystal display (LCD)

The LCD drives up to 8 common terminals and 48 segment terminals to drive up to 384 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode
- V_{LCD} rails decoupling capability

3.12 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L073xx device. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference, V_{LCD} voltage measurement). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.

The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 µA at 10 kSPS, ~240 µA at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

3.13.2 V_{LCD} voltage monitoring

This embedded hardware feature allows the application to measure the V_{LCD} supply voltage using the internal ADC channel ADC_IN16. As the V_{LCD} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the ADC input is connected to LCD_VLCD2 (which provides $1/3V_{LCD}$ when the LCD is configured 1/3Bias and $1/4V_{LCD}$ when the LCD is configured 1/4Bias or 1/2Bias).

3.14 Digital-to-analog converter (DAC)

Two 12-bit buffered DACs can be used to convert digital signal into analog voltage signal output. An optional amplifier can be used to reduce the output signal impedance.

This digital Interface supports the following features:

- One data holding register (for each channel)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels with independent or simultaneous conversions
- DMA capability (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage V_{REF+}

Six DAC trigger inputs are used in the STM32L073xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.15 Ultra-low-power comparators and reference voltage

The STM32L073xx embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
  - DAC output
  - External I/O pins
  - Internal reference voltage (V_{REFINT})
  - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.18 Communication interfaces

3.18.1 I²C bus

Up to three I²C interfaces (I2C1 and I2C3) can operate in multimaster or slave modes.

Each I²C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask) are also supported as well as programmable analog and digital noise filters.

Table 11. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 and I2C3 provide hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1/I2C3 also have a clock domain independent from the CPU clock, allowing the I2C1/I2C3 to wake up the MCU from Stop mode on address match.

Each I2C interface can be served by the DMA controller.

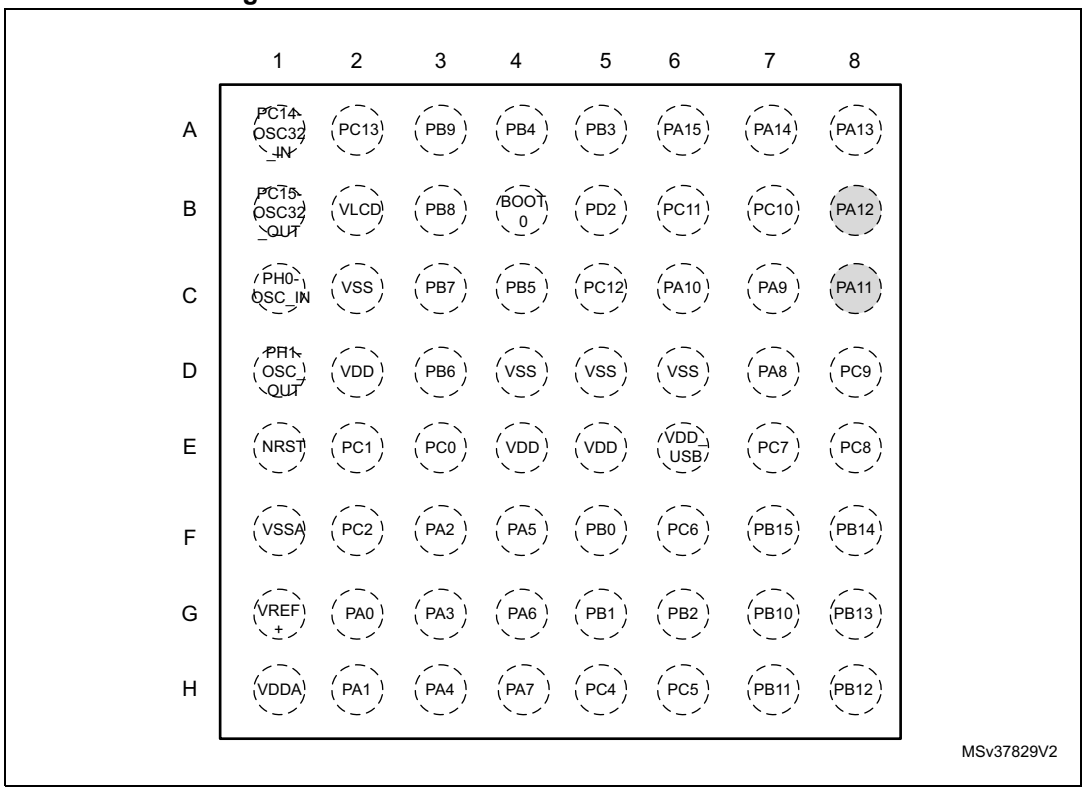
Refer to *Table 12* for an overview of I2C interface features.

Table 12. STM32L073xx I²C implementation

I2C features(1)	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X(2)	X
Independent clock	X	-	X
SMBus	X	-	X
Wakeup from STOP	X	-	X

1. X = supported.
2. See *Table 16: STM32L073xx pin definition on page 42* for the list of I/Os that feature Fast Mode Plus capability

Figure 6. STM32L073xx TFBGA64 ballout - 5x 5 mm



1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Table 16. STM32L073xx pin definition (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100						
-	18	C2	27	E3	VSS	S	-	-	-	-
-	19	D2	28	H3	VDD	S	-	-	-	-
14	20	H3	29	M3	PA4	I/O	TC	(1)	SPI1_NSS, TSC_G2_IO1, USART2_CK, TIM22_ETR	COMP1_INM, COMP2_INM, ADC_IN4, DAC_OUT1
15	21	F4	30	K4	PA5	I/O	TC	-	SPI1_SCK, TIM2_ETR, TSC_G2_IO2, TIM2_CH1	COMP1_INM, COMP2_INM, ADC_IN5, DAC_OUT2
16	22	G4	31	L4	PA6	I/O	FT	-	SPI1_MISO, LCD_SEG3, TIM3_CH1, TSC_G2_IO3, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6
17	23	H4	32	M4	PA7	I/O	FT	-	SPI1_MOSI, LCD_SEG4, TIM3_CH2, TSC_G2_IO4, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	24	H5	33	K5	PC4	I/O	FT	-	EVENTOUT, LCD_SEG22, LPUART1_TX	ADC_IN14
-	25	H6	34	L5	PC5	I/O	FT	-	LCD_SEG23, LPUART1_RX, TSC_G3_IO1	ADC_IN15
18	26	F5	35	M5	PB0	I/O	FT	-	EVENTOUT, LCD_SEG5, TIM3_CH3, TSC_G3_IO2	LCD_VLCD3, ADC_IN8, VREF_OUT
19	27	G5	36	M6	PB1	I/O	FT	-	LCD_SEG6, TIM3_CH4, TSC_G3_IO3, LPUART1_RTS_DE	ADC_IN9, VREF_OUT
20	28	G6	37	L6	PB2	I/O	FT	-	LPTIM1_OUT, TSC_G3_IO4, I2C3_SMBA	LCD_VLCD1
-	-	-	38	M7	PE7	I/O	FT	-	LCD_SEG45, USART5_CK/USART5_RTS	-
-	-	-	39	L7	PE8	I/O	FT	-	LCD_SEG46, USART4_TX	-
-	-	-	40	M8	PE9	I/O	FT	-	TIM2_CH1, LCD_SEG47, TIM2_ETR, USART4_RX	-

Table 16. STM32L073xx pin definition (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100						
-	-	-	41	L8	PE10	I/O	FT	-	TIM2_CH2, LCD_SEG40, USART5_TX	-
-	-	-	42	M9	PE11	I/O	FT	-	TIM2_CH3, USART5_RX	LCD_VLCD2
-	-	-	43	L9	PE12	I/O	FT	-	TIM2_CH4, SPI1_NSS	LCD_VLCD3
-	-	-	44	M10	PE13	I/O	FT	-	LCD_SEG41, SPI1_SCK	-
-	-	-	45	M11	PE14	I/O	FT	-	LCD_SEG42, SPI1_MISO	-
-	-	-	46	M12	PE15	I/O	FT	-	LCD_SEG43, SPI1_MOSI	-
21	29	G7	47	L10	PB10	I/O	FT	-	LCD_SEG10, TIM2_CH3, TSC_SYNC, LPUART1_TX, SPI2_SCK, I2C2_SCL, LPUART1_RX	-
22	30	H7	48	L11	PB11	I/O	FT	-	EVENTOUT, LCD_SEG11, TIM2_CH4, TSC_G6_IO1, LPUART1_RX, I2C2_SDA, LPUART1_TX	-
23	31	D6	49	F12	VSS	S		-	-	-
24	32	E5	50	G12	VDD	S		-	-	-
25	33	H8	51	L12	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LCD_SEG12, LPUART1_RTS_DE, TSC_G6_IO2, I2C2_SMBA, EVENTOUT	LCD_VLCD2
26	34	G8	52	K12	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, LCD_SEG13, MCO, TSC_G6_IO3, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
27	35	F8	53	K11	PB14	I/O	FTf	-	SPI2_MISO/I2S2_MCK, LCD_SEG14, RTC_OUT, TSC_G6_IO4, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
28	36	F7	54	K10	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD, LCD_SEG15, RTC_REFIN	-
-	-	-	55	K9	PD8	I/O	FT	-	LPUART1_TX, LCD_SEG28	-

Table 16. STM32L073xx pin definition (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64	LQFP100	UFBGA100						
-	-	-	56	K8	PD9	I/O	FT	-	LPUART1_RX, LCD_SEG29	-
-	-	-	57	J12	PD10	I/O	FT	-	LCD_SEG30	-
-	-	-	58	J11	PD11	I/O	FT	-	LPUART1_CTS, LCD_SEG31	-
-	-	-	59	J10	PD12	I/O	FT	-	LPUART1_RTS_DE, LCD_SEG32	-
-	-	-	60	H12	PD13	I/O	FT	-	LCD_SEG33	-
-	-	-	61	H11	PD14	I/O	FT	-	LCD_SEG34	-
-	-	-	62	H10	PD15	I/O	FT	-	USB_CRS_SYNC, LCD_SEG35	-
-	37	F6	63	E12	PC6	I/O	FT	-	TIM22_CH1, LCD_SEG24, TIM3_CH1, TSC_G8_IO1	-
-	38	E7	64	E11	PC7	I/O	FT	-	TIM22_CH2, LCD_SEG25, TIM3_CH2, TSC_G8_IO2	-
-	39	E8	65	E10	PC8	I/O	FT	-	TIM22_ETR, LCD_SEG26, TIM3_CH3, TSC_G8_IO3	-
-	40	D8	66	D12	PC9	I/O	FTf	-	TIM21_ETR, LCD_SEG27, USB_OE/TIM3_CH4, TSC_G8_IO4, I2C3_SDA	-
29	41	D7	67	D11	PA8	I/O	FTf	-	MCO, LCD_COM0, USB_CRS_SYNC, EVENTOUT, USART1_CK, I2C3_SCL	-
30	42	C7	68	D10	PA9	I/O	FTf	-	MCO, LCD_COM1, TSC_G4_IO1, USART1_TX, I2C1_SCL, I2C3_SMBA	-
31	43	C6	69	C12	PA10	I/O	FTf	-	LCD_COM2, TSC_G4_IO2, USART1_RX, I2C1_SDA	-
32	44	C8	70	B12	PA11	I/O	FT	(2)	SPI1_MISO, EVENTOUT, TSC_G4_IO3, USART1_CTS, COMP1_OUT	USB_DM

Table 22. Alternate functions port H

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/ I2S2/USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2 /I2C1/LCD/TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/ LPTIM1/TIM2/3/ EVENTOUT/ SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2/I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/ LPUART1/ COMP1/2/ TIM3
Port H	PH0	USB_CRS_SYNC	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH9	-	-	-	-	-	-	-	-
	PH10	-	-	-	-	-	-	-	-

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 26*.

Table 27. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	

Table 27. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	V
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in *Table 29* are based on characterization results, unless otherwise specified.

Table 28. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 29. Embedded internal reference voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$(2)	Internal reference voltage	– 40 °C < T_J < +125 °C	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value(3)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(4)	Temperature coefficient	–40 °C < T_J < +125 °C	-	25	100	ppm/°C
A_{Coeff}(4)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(4)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(4)(5)	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}(4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(4)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(4)	VREF_OUT output current(6)	-	-	-	1	µA
C_{VREF_OUT}(4)	VREF_OUT output load	-	-	-	50	pF

Table 42. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	7	8	Number of clock cycles
$t_{WUSLEEP\_LP}$	Wakeup from Low-power sleep mode, f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash memory enabled	7	8	
		f_{HCLK} = 262 kHz Flash memory switched OFF	9	10	
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz	5.0	8	µs
		$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 1	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 2	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 3	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	7.3	13	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	13	23	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	28	38	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	51	65	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	100	120	
		f_{HCLK} = MSI = 65 kHz	190	260	
		$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode, code running from RAM	$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	7.9	10	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz	4.7	8	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	65	130	
	Wakeup from Standby mode FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	2.2	3	ms

6.3.7 Internal clock source characteristics

The parameters given in *Table 47* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

High-speed internal 16 MHz (HSI16) RC oscillator

Table 47. 16 MHz HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI16 user-trimmed resolution	Trimming code is not a multiple of 16	-	± 0.4	0.7	%
		Trimming code is a multiple of 16	-	-	± 1.5	%
ACC_{HSI16} (2)	Accuracy of the factory-calibrated HSI16 oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1(3)	-	1(3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = − 40 to 125 °C	-5.45	-	3.25	%
$t_{SU(HSI16)}^{(2)}$	HSI16 oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI16)}^{(2)}$	HSI16 oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Figure 23. HSI16 minimum and maximum value versus temperature

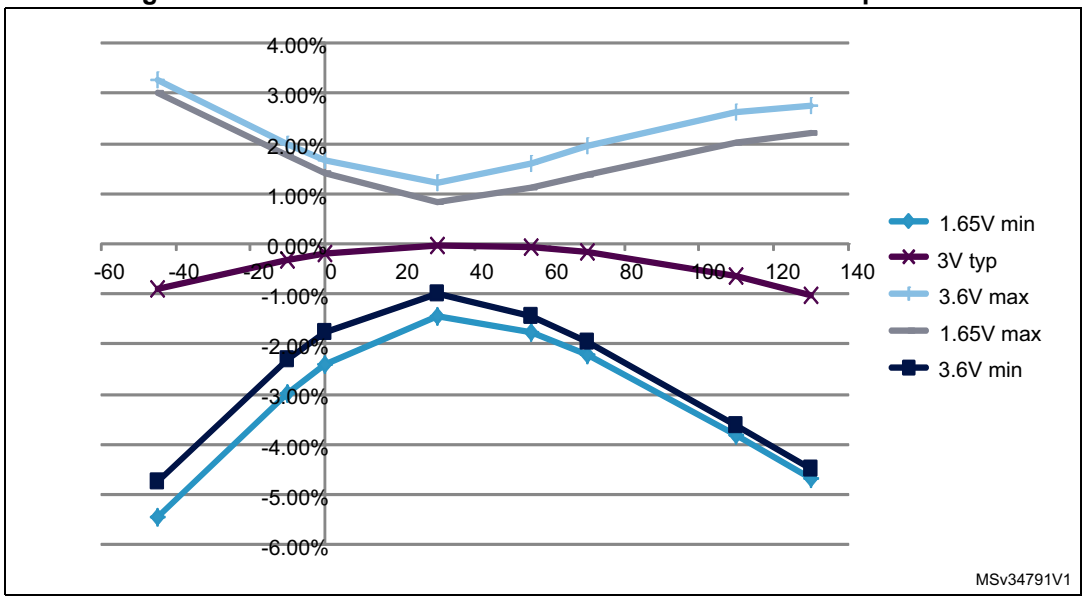
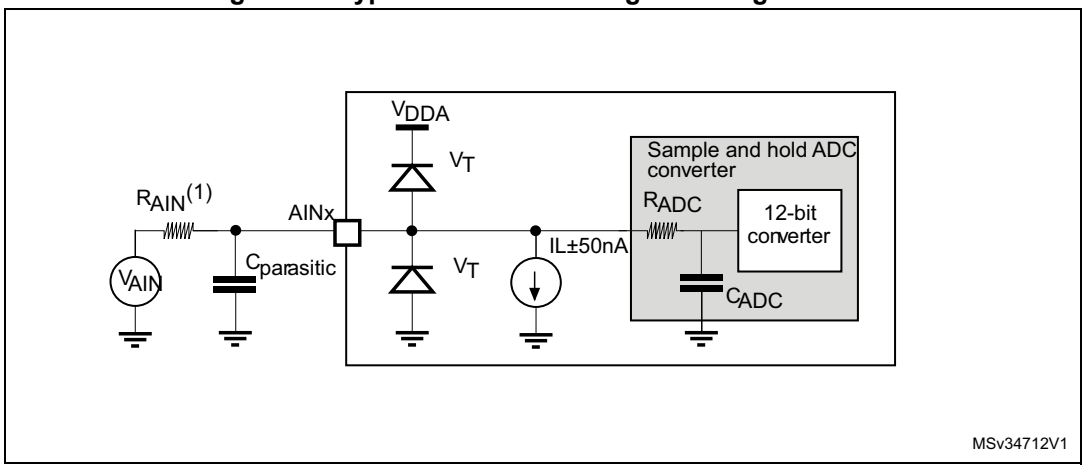


Figure 29. Typical connection diagram using the ADC

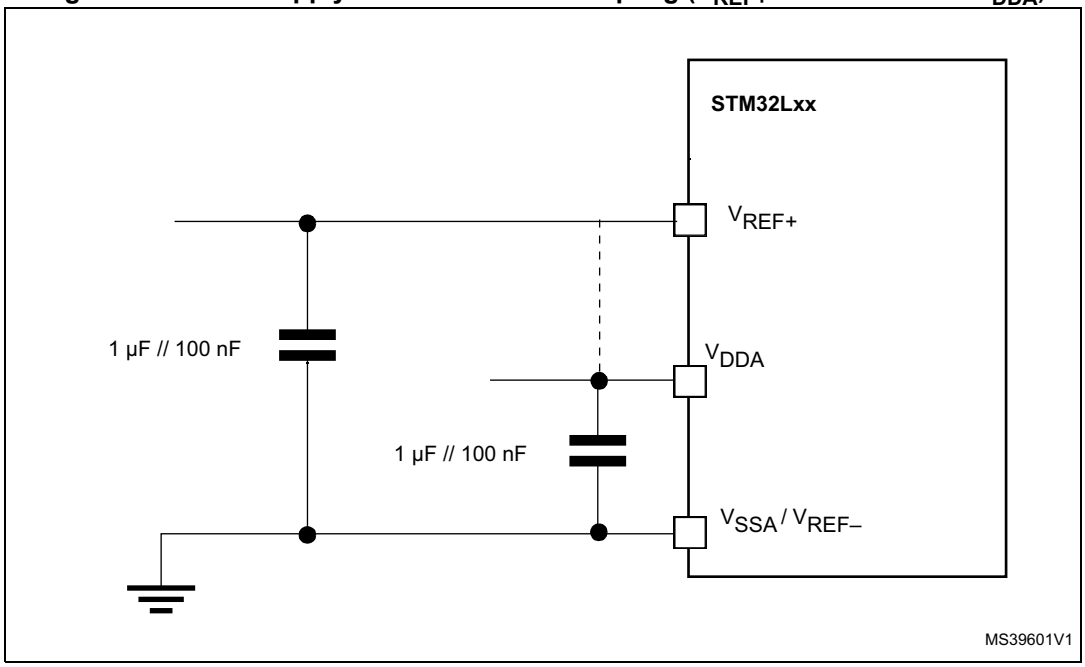


1. Refer to *Table 64: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 30* or *Figure 31*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 30. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



USB characteristics

The USB interface is USB-IF certified (full speed).

Table 79. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

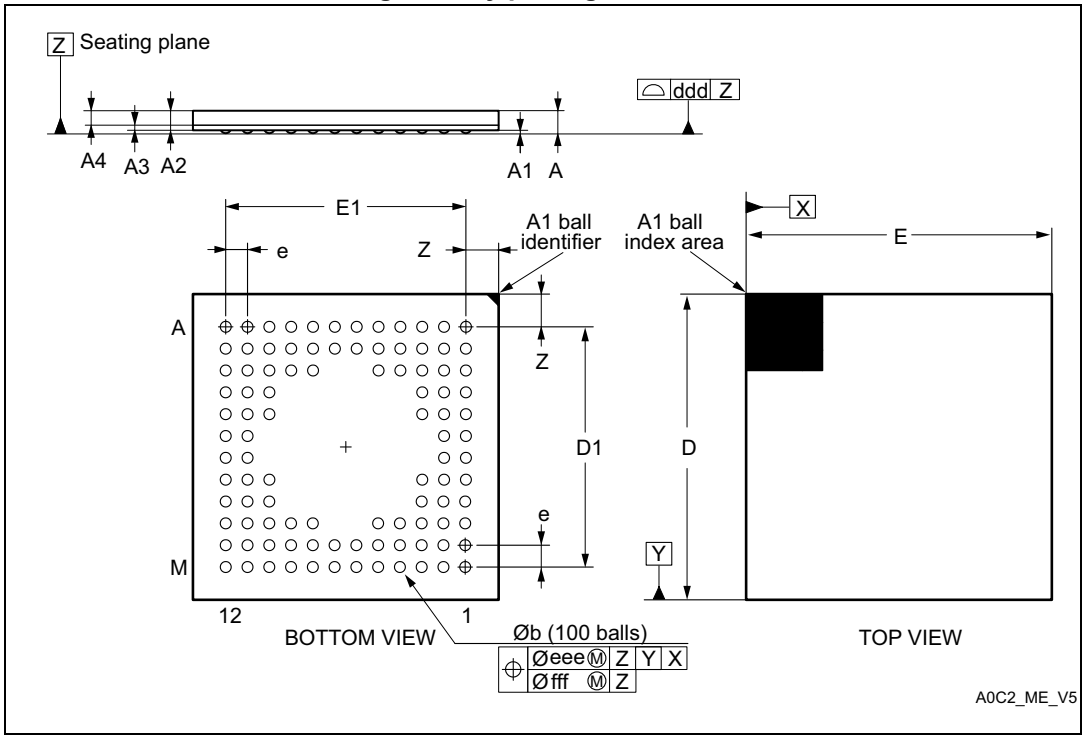
Table 80. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage	-	3.0	3.6	V
V_{DI}(2)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(2)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(2)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}(3)	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	0.3	V
V_{OH}(3)	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.
4. R_L is the load connected on the USB drivers.

7.2 UFBGA100 package information

Figure 42. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



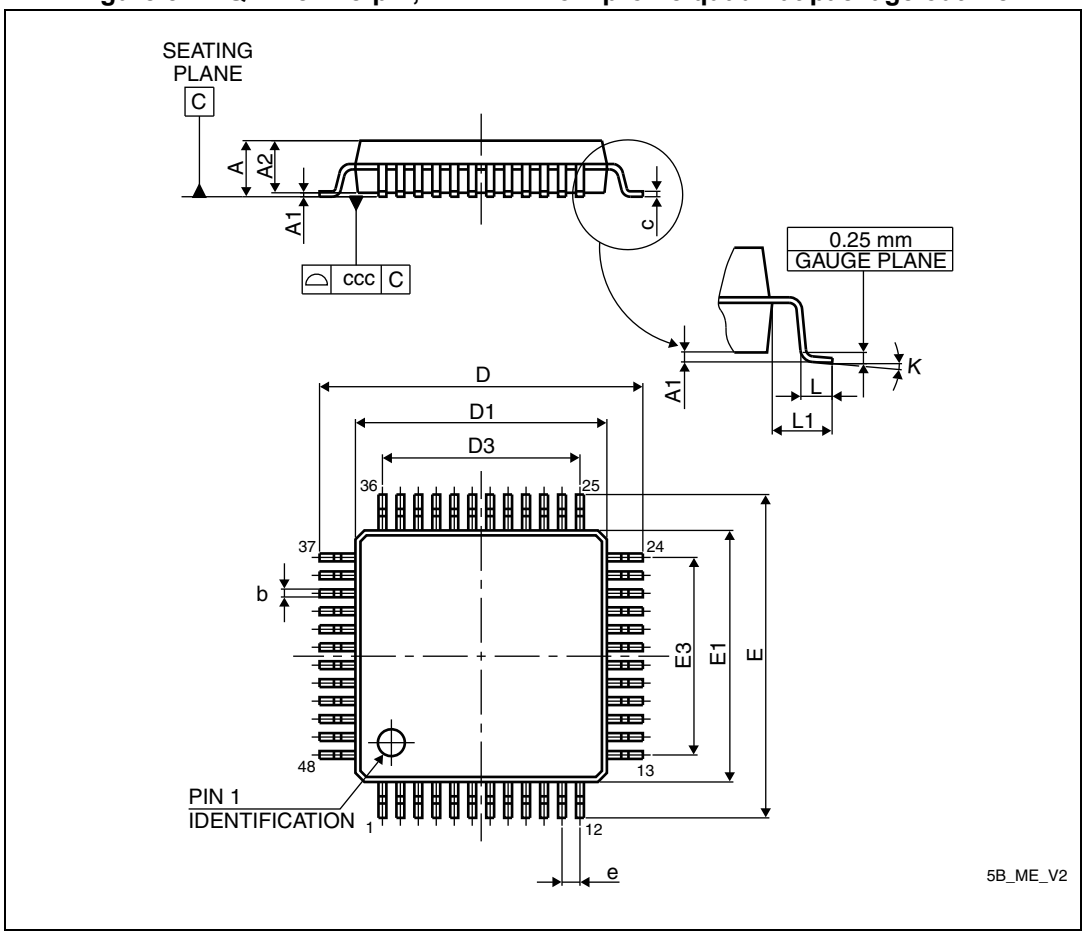
1. Drawing is not to scale.

Table 84. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

7.5 LQFP48 package information

Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

8 Part numbering

Table 91. STM32L073xx ordering information scheme

Example: STM32 L 073 R 8 T 6 D TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

073 = USB + LCD

Pin count

C = 48/49 pins

R = 64 pins

V = 100 pins

Flash memory size

8 = 64 Kbytes

B = 128 Kbytes

Z = 192 Kbytes

Package

T = LQFP

H = TFBGA

I = UFBGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

3 = Industrial temperature range, –40 to 125 °C

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled

D = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.