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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 84 |
| Program Memory Size | 192KB (192K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 6K x 8 |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l073vzt6d |

## 2.1 Device overview

**Table 2. Ultra-low-power STM32L073xxx device features and peripheral counts**

| Peripheral | | STM32L073 V8 | STM32L073 CB | STM32L073 VB | STM32L073 RB | STM32L073 CZ | STM32L073 VZ | STM32L073 RZ |
|---|---|---|---|---|---|---|---|---|
| Flash (Kbytes) | | 64 Kbytes | 128 Kbytes | | | 192 Kbytes | | |
| Data EEPROM (Kbytes) | | 3 Kbytes | 6 Kbytes | | | | | |
| RAM (Kbytes) | | 20 Kbytes | | | | | | |
| Timers | General-purpose | 4 | | | | | | |
| | Basic | 2 | | | | | | |
| | LPTIMER | 1 | | | | | | |
| RTC/SYSTICK/IWDG/WWDG | | 1/1/1/1 | | | | | | |
| Commu-nication interfaces | SPI/I2S | 6(4)[1]/1 | | | | | | |
| | $I^2C$ | 3 | | | | | | |
| | USART | 4 | | | | | | |
| | LPUART | 1 | | | | | | |
| | USB/(VDD_USB) | 1/(1) | | | | | | |
| GPIOs | | 84 | 37 | 84 | 51[2] | 37 | 84 | 51[2] |
| Clocks: HSE/LSE/HSI/MSI/LSI | | 1/1/1/1/1 | | | | | | |
| 12-bit synchronized ADC Number of channels | | 1<br>16 | 1<br>10 | 1<br>16[2] | | 1<br>10 | 1<br>16[2] | |
| 12-bit DAC Number of channels | | 2<br>2 | | | | | | |
| LCD COM x SEG | | 1<br>4x52 or 8x48 | 1<br>4x18 | 1<br>4x52 or 8x48 | 1<br>4x32 or 8x28[2] | 1<br>4x18 | 1<br>4x52 or 8x48 | 1<br>4x32 or 8x28[2] |
| Comparators | | 2 | | | | | | |
| Capacitive sensing channels | | 24 | 17 | 24 | 24[2] | 17 | 24 | 24[2] |
| Max. CPU frequency | | 32 MHz | | | | | | |
| Operating voltage | | 1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 to 3.6 V without BOR option | | | | | | |
| Operating temperatures | | Ambient temperature: –40 to +125 °C<br>Junction temperature: –40 to +130 °C | | | | | | |
| Packages | | LQFP100 UFBGA100 | LQFP48 | LQFP100 UFBGA100 | LQFP64, TFBGA64 | LQFP48 | LQFP100 UFBGA100 | LQFP64, TFBGA64 |

1. 4 SPI interfaces are USARTs operating in SPI master mode.
2. TFBGA64 has one GPIO, one ADC input, one capacitive sensing channel and one COMxSEG (4x31 or 8x27) less than LQFP64.

# 3 Functional overview

## 3.1 Low-power modes

The ultra-low-power STM32L073xx support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 ($V_{DD}$ range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full $V_{DD}$ range), with a maximum CPU frequency of 16 MHz
- Range 3 (full $V_{DD}$ range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

  This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

  **Stop mode with RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the $V_{CORE}$ domain are stopped, the PLL, MSI RC, HSE crystal and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Stop mode without RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

  The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode. The LCD is not stopped automatically by entering Stop mode.*

- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS)**

  This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

  Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.

- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

Table 16. STM32L073xx pin definition (continued)

| Pin number | | | | | Pin name (function after reset) | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | TFBGA64 | LQFP100 | UFBGA100 | | | | | | |
| - | 8 | E3 | 15 | H1 | PC0 | I/O | FTf | - | LPTIM1_IN1, LCD_SEG18, EVENTOUT, TSC_G7_IO1, LPUART1_RX, I2C3_SCL | ADC_IN10 |
| - | 9 | E2 | 16 | J2 | PC1 | I/O | FTf | - | LPTIM1_OUT, LCD_SEG19, EVENTOUT, TSC_G7_IO2, LPUART1_TX, I2C3_SDA | ADC_IN11 |
| - | 10 | F2 | 17 | J3 | PC2 | I/O | FTf | - | LPTIM1_IN2, LCD_SEG20, SPI2_MISO/I2S2_MCK, TSC_G7_IO3 | ADC_IN12 |
| - | 11 | - | 18 | K2 | PC3 | I/O | FT | - | LPTIM1_ETR, LCD_SEG21, SPI2_MOSI/I2S2_SD, TSC_G7_IO4 | ADC_IN13 |
| 8 | 12 | F1 | 19 | J1 | VSSA | S | - | - | - | - |
| - | - | - | 20 | K1 | VREF- | S | - | - | - | - |
| - | - | G1 | 21 | L1 | VREF+ | S | - | - | - | - |
| 9 | 13 | H1 | 22 | M1 | VDDA | S | - | - | - | - |
| 10 | 14 | G2 | 23 | L2 | PA0 | I/O | TC | - | TIM2_CH1, TSC_G1_IO1, USART2_CTS, TIM2_ETR, USART4_TX, COMP1_OUT | COMP1_INM, ADC_IN0, RTC_TAMP2/WKUP1 |
| 11 | 15 | H2 | 24 | M2 | PA1 | I/O | FT | - | EVENTOUT, LCD_SEG0, TIM2_CH2, TSC_G1_IO2, USART2_RTS_DE, TIM21_ETR, USART4_RX | COMP1_INP, ADC_IN1 |
| 12 | 16 | F3 | 25 | K3 | PA2 | I/O | FT | - | TIM21_CH1, LCD_SEG1, TIM2_CH3, TSC_G1_IO3, USART2_TX, LPUART1_TX, COMP2_OUT | COMP2_INM, ADC_IN2 |
| 13 | 17 | G3 | 26 | L3 | PA3 | I/O | FT | - | TIM21_CH2, LCD_SEG2, TIM2_CH4, TSC_G1_IO4, USART2_RX, LPUART1_RX | COMP2_INP, ADC_IN3 |

Table 16. STM32L073xx pin definition (continued)

| Pin number | | | | | Pin name (function after reset) | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | TFBGA64 | LQFP100 | UFBGA100 | | | | | | |
| - | 18 | C2 | 27 | E3 | VSS | S | - | - | - | - |
| - | 19 | D2 | 28 | H3 | VDD | S | - | - | - | - |
| 14 | 20 | H3 | 29 | M3 | PA4 | I/O | TC | (1) | SPI1_NSS, TSC_G2_IO1, USART2_CK, TIM22_ETR | COMP1_INM, COMP2_INM, ADC_IN4, DAC_OUT1 |
| 15 | 21 | F4 | 30 | K4 | PA5 | I/O | TC | - | SPI1_SCK, TIM2_ETR, TSC_G2_IO2, TIM2_CH1 | COMP1_INM, COMP2_INM, ADC_IN5, DAC_OUT2 |
| 16 | 22 | G4 | 31 | L4 | PA6 | I/O | FT | - | SPI1_MISO, LCD_SEG3, TIM3_CH1, TSC_G2_IO3, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT | ADC_IN6 |
| 17 | 23 | H4 | 32 | M4 | PA7 | I/O | FT | - | SPI1_MOSI, LCD_SEG4, TIM3_CH2, TSC_G2_IO4, TIM22_CH2, EVENTOUT, COMP2_OUT | ADC_IN7 |
| - | 24 | H5 | 33 | K5 | PC4 | I/O | FT | - | EVENTOUT, LCD_SEG22, LPUART1_TX | ADC_IN14 |
| - | 25 | H6 | 34 | L5 | PC5 | I/O | FT | - | LCD_SEG23, LPUART1_RX, TSC_G3_IO1 | ADC_IN15 |
| 18 | 26 | F5 | 35 | M5 | PB0 | I/O | FT | - | EVENTOUT, LCD_SEG5, TIM3_CH3, TSC_G3_IO2 | LCD_VLCD3, ADC_IN8, VREF_OUT |
| 19 | 27 | G5 | 36 | M6 | PB1 | I/O | FT | - | LCD_SEG6, TIM3_CH4, TSC_G3_IO3, LPUART1_RTS_DE | ADC_IN9, VREF_OUT |
| 20 | 28 | G6 | 37 | L6 | PB2 | I/O | FT | - | LPTIM1_OUT, TSC_G3_IO4, I2C3_SMBA | LCD_VLCD1 |
| - | - | - | 38 | M7 | PE7 | I/O | FT | - | LCD_SEG45, USART5_CK/USART5_RTS | - |
| - | - | - | 39 | L7 | PE8 | I/O | FT | - | LCD_SEG46, USART4_TX | - |
| - | - | - | 40 | M8 | PE9 | I/O | FT | - | TIM2_CH1, LCD_SEG47, TIM2_ETR, USART4_RX | - |

**Table 22. Alternate functions port H**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI1/SPI2/ I2S2/USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF | SPI1/SPI2/I2S2 /I2C1/LCD/TIM2/21 | SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/ LPTIM1/TIM2/3/ EVENTOUT/ SYS_AF | I2C1/TSC/ EVENTOUT | I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT | SPI2/I2S2/I2C2/ USART1/ TIM2/21/22 | I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT | I2C3/ LPUART1/ COMP1/2/ TIM3 |
| Port H | PH0 | USB_CRS_SYNC | - | - | - | - | - | - | - |
| | PH1 | - | - | - | - | - | - | - | - |
| | PH9 | - | - | - | - | - | - | - | - |
| | PH10 | - | - | - | - | - | - | - | - |

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.6 V (for the 1.65 V ≤ $V_{DD}$ ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

**Figure 9. Pin loading conditions**

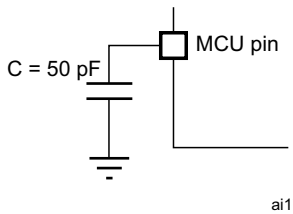



**Figure 10. Pin input voltage**

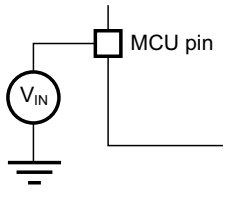


**Table 26. General operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_A$ | Temperature range | Maximum power dissipation (range 6) | –40 | 85 | °C |
| | | Maximum power dissipation (range 7) | –40 | 105 | |
| | | Maximum power dissipation (range 3) | –40 | 125 | |
| $T_J$ | Junction temperature range (range 6) | -40 °C ≤ $T_A$ ≤ 85 ° | –40 | 105 | |
| | Junction temperature range (range 7) | -40 °C ≤ $T_A$ ≤ 105 °C | –40 | 125 | |
| | Junction temperature range (range 3) | -40 °C ≤ $T_A$ ≤ 125 °C | –40 | 130 | |

1. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and normal operation.
2. $V_{DD\_USB}$ must respect the following conditions:

- When $V_{DD}$ is powered on ($V_{DD}$ < $V_{DD\_min}$), $V_{DD\_USB}$ should be always lower than $V_{DD}$.
- When $V_{DD}$ is powered down ($V_{DD}$ < $V_{DD\_min}$), $V_{DD\_USB}$ should be always lower than $V_{DD}$.
- In operating mode, $V_{DD\_USB}$ could be lower or higher $V_{DD}$.
- If the USB is not used, $V_{DD\_USB}$ must range from $V_{DD\_min}$ to $V_{DD\_max}$ to be able to use PA11 and PA12 as standard I/Os.

3. To sustain a voltage higher than $V_{DD}$+0.3V, the internal pull-up/pull-down resistors must be disabled.
4. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_J$ max (see *Table 90: Thermal characteristics on page 134*).

**Table 34. Current consumption in Sleep mode**

| Symbol | Parameter | Condition | | $f_{HCLK}$ (MHz) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Sleep) | Supply current in Sleep mode, Flash memory switched OFF | $f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2) | Range3, Vcore=1.2 V VOS[1:0]=11 | 1 | 43,5 | 110 | µA |
| | | | | 2 | 72 | 140 | |
| | | | | 4 | 130 | 200 | |
| | | | Range2, Vcore=1.5 V VOS[1:0]=10 | 4 | 160 | 220 | |
| | | | | 8 | 305 | 380 | |
| | | | | 16 | 590 | 690 | |
| | | | Range1, Vcore=1.8 V VOS[1:0]=01 | 8 | 370 | 460 | |
| | | | | 16 | 715 | 840 | |
| | | | | 32 | 1650 | 2000 | |
| | | MSI clock | Range3, Vcore=1.2 V VOS[1:0]=11 | 0,065 | 18 | 93 | |
| | | | | 0,524 | 31,5 | 110 | |
| | | | | 4,2 | 140 | 230 | |
| | | HSI clock source (16 MHz) | Range2, Vcore=1.5 V VOS[1:0]=10 | 16 | 665 | 850 | |
| | | | Range1, Vcore=1.8 V VOS[1:0]=01 | 32 | 1750 | 2100 | |
| | Supply current in Sleep mode, Flash memory switched ON | $f_{HSE} = f_{HCLK}$ up to 16MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2) | Range3, Vcore=1.2 V VOS[1:0]=11 | 1 | 57,5 | 130 | |
| | | | | 2 | 84 | 160 | |
| | | | | 4 | 150 | 220 | |
| | | | Range2, Vcore=1.5 V VOS[1:0]=10 | 4 | 170 | 240 | |
| | | | | 8 | 315 | 400 | |
| | | | | 16 | 605 | 710 | |
| | | | Range1, Vcore=1.8 V VOS[1:0]=01 | 8 | 380 | 470 | |
| | | | | 16 | 730 | 860 | |
| | | | | 32 | 1650 | 2000 | |
| | | MSI clock | Range3, Vcore=1.2 V VOS[1:0]=11 | 0,065 | 29,5 | 110 | |
| | | | | 0,524 | 44,5 | 120 | |
| | | | | 4,2 | 150 | 240 | |
| | | HSI clock source (16MHz) | Range2, Vcore=1.5 V VOS[1:0]=10 | 16 | 680 | 930 | |
| | | | Range1, Vcore=1.8 V VOS[1:0]=01 | 32 | 1750 | 2200 | |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Figure 16. $I_{DD}$ vs $V_{DD}$, at $T_A$= 25 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS**

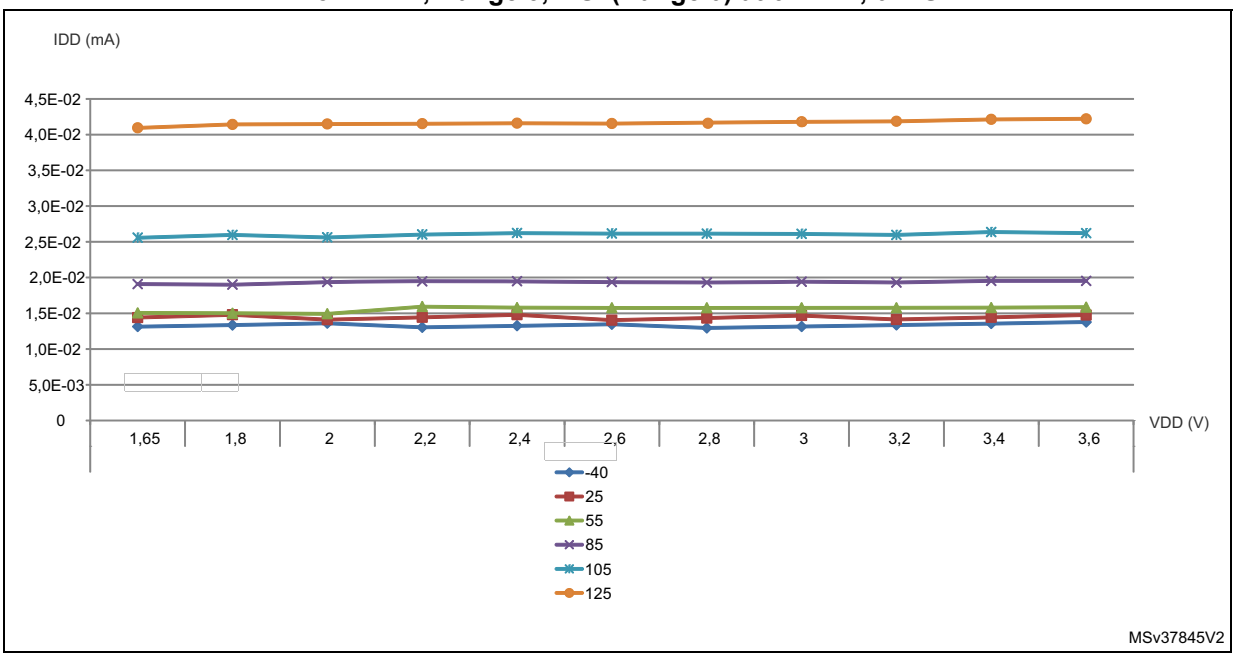



**Table 36. Current consumption in Low-power sleep mode**

| Symbol | Parameter | Condition | | | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (LP Sleep) | Supply current in Low-power sleep mode | All peripherals OFF, code executed from Flash memory, $V_{DD}$ from 1.65 to 3.6 V | MSI clock = 65 kHz, $f_{HCLK}$= 32 kHz, Flash memory OFF | $T_A$ = −40 to 25°C | 4,7 | - | µA |
| | | | MSI clock = 65 kHz, $f_{HCLK}$= 32 kHz | $T_A$ = −40 to 25°C | 17 | 24 | |
| | | | | $T_A$ = 85°C | 19,5 | 30 | |
| | | | | $T_A$= 105°C | 23 | 47 | |
| | | | | $T_A$= 125°C | 32,5 | 70 | |
| | | | MSI clock = 65 kHz, $f_{HCLK}$= 65 kHz | $T_A$= − 40 to 25°C | 17 | 24 | |
| | | | | $T_A$= 85°C | 20 | 31 | |
| | | | | $T_A$ = 105°C | 23,5 | 47 | |
| | | | | $T_A$ = 125°C | 32,5 | 70 | |
| | | | MSI clock = 131kHz, $f_{HCLK}$= 131 kHz | $T_A$= − 40 to 25°C | 19,5 | 27 | |
| | | | | $T_A$ = 55°C | 20,5 | 28 | |
| | | | | $T_A$ = 85°C | 22,5 | 33 | |
| | | | | $T_A$ = 105°C | 26 | 50 | |
| | | | | $T_A$= 125°C | 35 | 73 | |

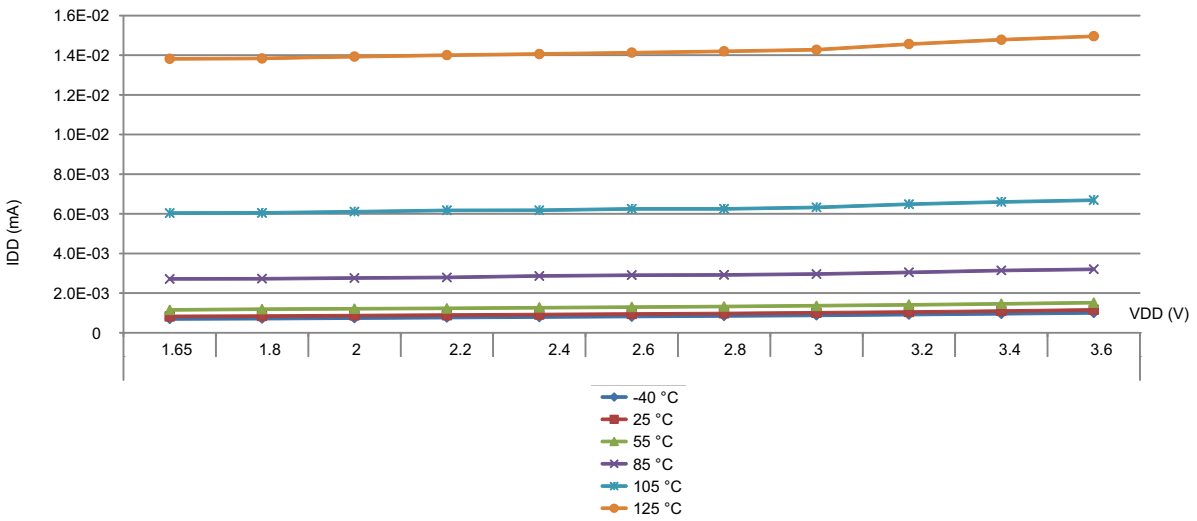
1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

**Table 37. Typical and maximum current consumptions in Stop mode**

| Symbol | Parameter | Conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ (Stop) | Supply current in Stop mode | $T_A$ = − 40 to 25°C | 0,43 | 1,00 | µA |
| | | $T_A$ = 55°C | 0,735 | 2,50 | |
| | | $T_A$= 85°C | 2,25 | 4,90 | |
| | | $T_A$ = 105°C | 5,3 | 13,00 | |
| | | $T_A$ = 125°C | 12,5 | 28,00 | |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

**Figure 17. $I_{DD}$ vs $V_{DD}$, at $T_A$= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive**



### High-speed internal 48 MHz (HSI48) RC oscillator

**Table 48. HSI48 oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI48}$ | Frequency | | - | 48 | - | MHz |
| TRIM | HSI48 user-trimming step | | 0.09(2) | 0.14 | 0.2(2) | % |
| $DuCy_{(HSI48)}$ | Duty cycle | | 45(2) | - | 55(2) | % |
| $ACC_{HSI48}$ | Accuracy of the HSI48 oscillator (factory calibrated before CRS calibration) | $T_A$ = 25 °C | -4(3) | - | 4(3) | % |
| $t_{su(HSI48)}$ | HSI48 oscillator startup time | | - | - | 6(2) | µs |
| $I_{DDA(HSI48)}$ | HSI48 oscillator power consumption | | - | 330 | 380(2) | µA |

1. $V_{DDA}$ = 3.3 V, $T_A$ = –40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.

### Low-speed internal (LSI) RC oscillator

**Table 49. LSI oscillator characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$(1) | LSI frequency | 26 | 38 | 56 | kHz |
| $D_{LSI}$(2) | LSI oscillator frequency drift $0°C \le T_A \le 85°C$ | -10 | - | 4 | % |
| $t_{su(LSI)}$(3) | LSI oscillator startup time | - | - | 200 | µs |
| $I_{DD(LSI)}$(3) | LSI oscillator power consumption | - | 400 | 510 | nA |

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

### Multi-speed internal (MSI) RC oscillator

**Table 50. MSI oscillator characteristics**

| Symbol | Parameter | Condition | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{MSI}$ | Frequency after factory calibration, done at $V_{DD}$= 3.3 V and $T_A$ = 25 °C | MSI range 0 | 65.5 | - | kHz |
| | | MSI range 1 | 131 | - | |
| | | MSI range 2 | 262 | - | |
| | | MSI range 3 | 524 | - | |
| | | MSI range 4 | 1.05 | - | MHz |
| | | MSI range 5 | 2.1 | - | |
| | | MSI range 6 | 4.2 | - | |

## 6.3.13 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 60* are derived from tests performed under the conditions summarized in *Table 26*. All I/Os are CMOS and TTL compliant.

**Table 60. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | TC, FT, FTf, RST I/Os | - | - | $0.3V_{DD}$ | V |
| | | BOOT0 pin | - | - | $0.14V_{DD}$ (1) | |
| $V_{IH}$ | Input high level voltage | All I/Os | $0.7\ V_{DD}$ | - | - | |
| $V_{hys}$ | I/O Schmitt trigger voltage hysteresis (2) | Standard I/Os | - | $10\%\ V_{DD}$ (3) | - | |
| | | BOOT0 pin | - | 0.01 | - | |
| $I_{lkg}$ | Input leakage current (4) | $V_{SS} \le V_{IN} \le V_{DD}$ All I/Os except for PA11, PA12, BOOT0 and FTf I/Os | - | - | ±50 | nA |
| | | $V_{SS} \le V_{IN} \le V_{DD}$, PA11 and PA12 I/Os | - | - | -50/+250 | |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ FTf I/Os | - | - | ±100 | |
| | | $V_{DD} \le V_{IN} \le 5$ V All I/Os except for PA11, PA12, BOOT0 and FTf I/Os | - | - | 200 | nA |
| | | $V_{DD} \le V_{IN} \le 5$ V FTf I/Os | - | - | 500 | |
| | | $V_{DD} \le V_{IN} \le 5$ V PA11, PA12 and BOOT0 | - | - | 10 | µA |
| $R_{PU}$ | Weak pull-up equivalent resistor(5) | $V_{IN} = V_{SS}$ | 30 | 45 | 60 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor(5) | $V_{IN} = V_{DD}$ | 30 | 45 | 60 | kΩ |
| $C_{IO}$ | I/O pin capacitance | - | - | 5 | - | pF |

1. Guaranteed by characterization.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
3. With a minimum of 200 mV. Guaranteed by characterization results.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

### 6.3.18 Comparators

**Table 70. Comparator 1 characteristics**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.65 | | 3.6 | V |
| $R_{400K}$ | $R_{400K}$ value | - | - | 400 | - | kΩ |
| $R_{10K}$ | $R_{10K}$ value | - | - | 10 | - | |
| $V_{IN}$ | Comparator 1 input voltage range | - | 0.6 | - | $V_{DDA}$ | V |
| $t_{START}$ | Comparator startup time | - | - | 7 | 10 | µs |
| td | Propagation delay(2) | - | - | 3 | 10 | |
| Voffset | Comparator offset | - | - | ±3 | ±10 | mV |
| $d_{Voffset}/dt$ | Comparator offset variation in worst voltage stress conditions | $V_{DDA}$ = 3.6 V, $V_{IN+}$ = 0 V, $V_{IN-}$ = $V_{REFINT}$, $T_A$ = 25 °C | 0 | 1.5 | 10 | mV/1000 h |
| $I_{COMP1}$ | Current consumption(3) | - | - | 160 | 260 | nA |

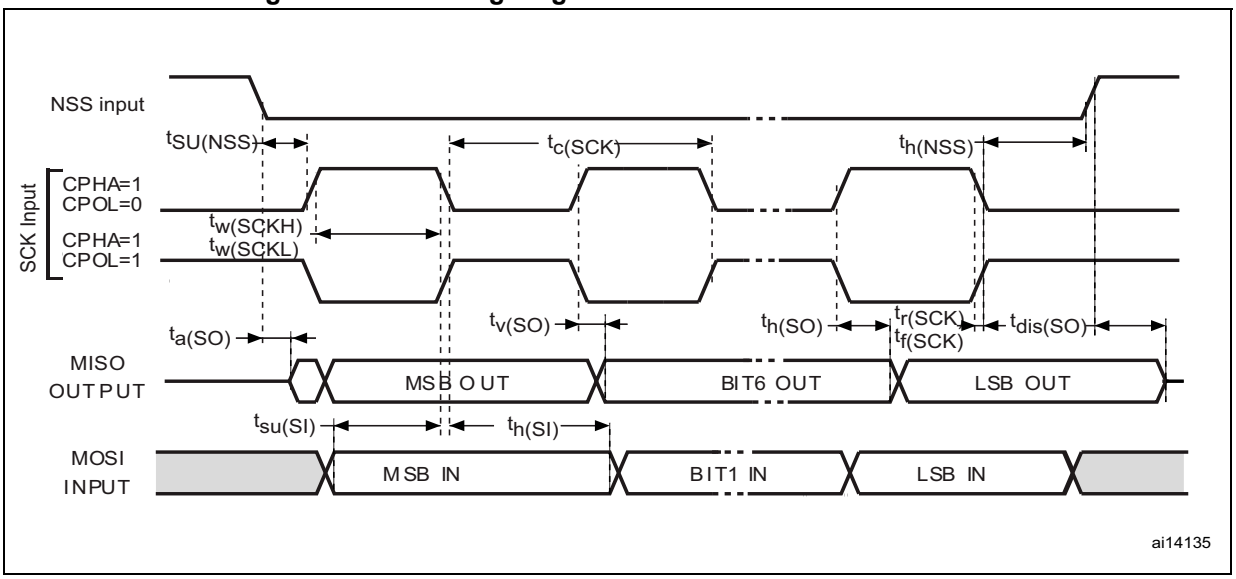
1. Guaranteed by characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

**Table 71. Comparator 2 characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.65 | - | 3.6 | V |
| $V_{IN}$ | Comparator 2 input voltage range | - | 0 | - | $V_{DDA}$ | V |
| $t_{START}$ | Comparator startup time | Fast mode | - | 15 | 20 | µs |
| | | Slow mode | - | 20 | 25 | |
| $t_{d\ slow}$ | Propagation delay(2) in slow mode | 1.65 V ≤ $V_{DDA}$ ≤ 2.7 V | - | 1.8 | 3.5 | |
| | | 2.7 V ≤ $V_{DDA}$ ≤ 3.6 V | - | 2.5 | 6 | |
| $t_{d\ fast}$ | Propagation delay(2) in fast mode | 1.65 V ≤ $V_{DDA}$ ≤ 2.7 V | - | 0.8 | 2 | |
| | | 2.7 V ≤ $V_{DDA}$ ≤ 3.6 V | - | 1.2 | 4 | |
| $V_{offset}$ | Comparator offset error | | - | ±4 | ±20 | mV |
| dThreshold/ dt | Threshold voltage temperature coefficient | $V_{DDA}$ = 3.3V, $T_A$ = 0 to 50 °C, V- = $V_{REFINT}$, 3/4 $V_{REFINT}$, 1/2 $V_{REFINT}$, 1/4 $V_{REFINT}$. | - | 15 | 30 | ppm /°C |
| $I_{COMP2}$ | Current consumption(3) | Fast mode | - | 3.5 | 5 | µA |
| | | Slow mode | - | 0.5 | 2 | |

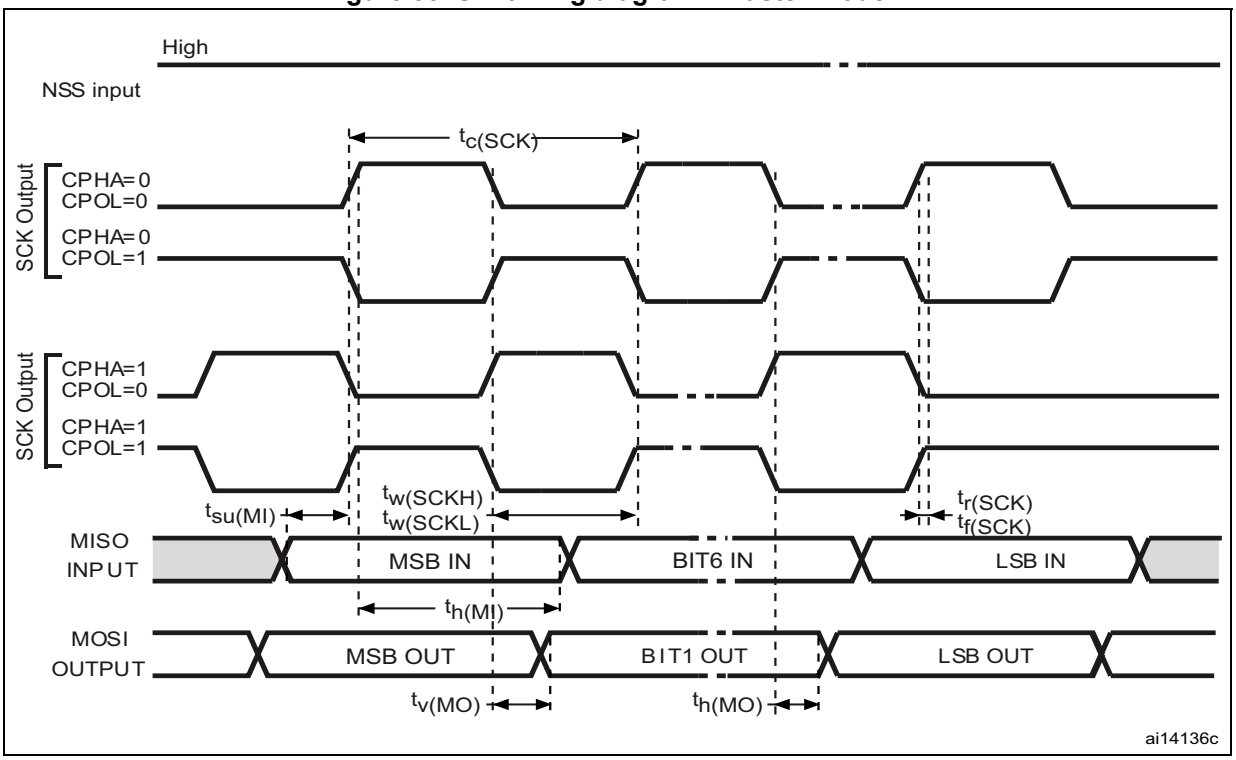
1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (required for comparator operation) is not included.

**Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 35. SPI timing diagram - master mode(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 38. USB timings: definition of data signal rise and fall time**

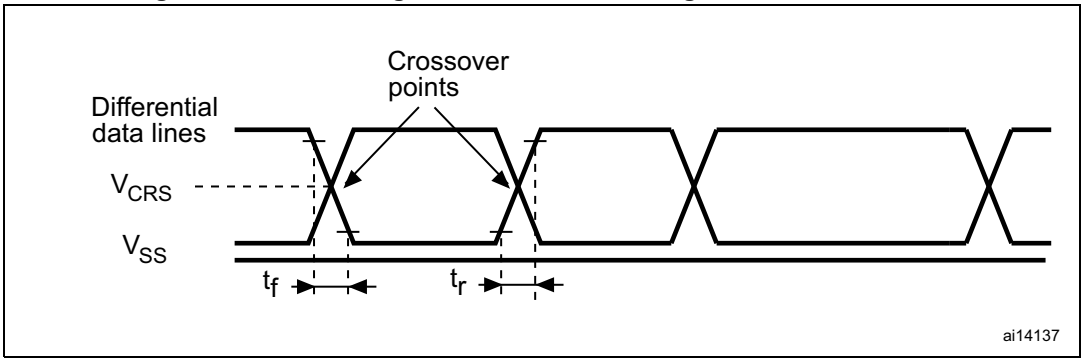



**Table 81. USB: full speed electrical characteristics**

| Driver characteristics[1] | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_r$ | Rise time[2] | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall Time[2] | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | | 1.3 | 2.0 | V |

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

## 6.3.21 LCD controller

The devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the $V_{DD}$ voltage. An external capacitor $C_{ext}$ must be connected to the $V_{LCD}$ pin to decouple this converter.

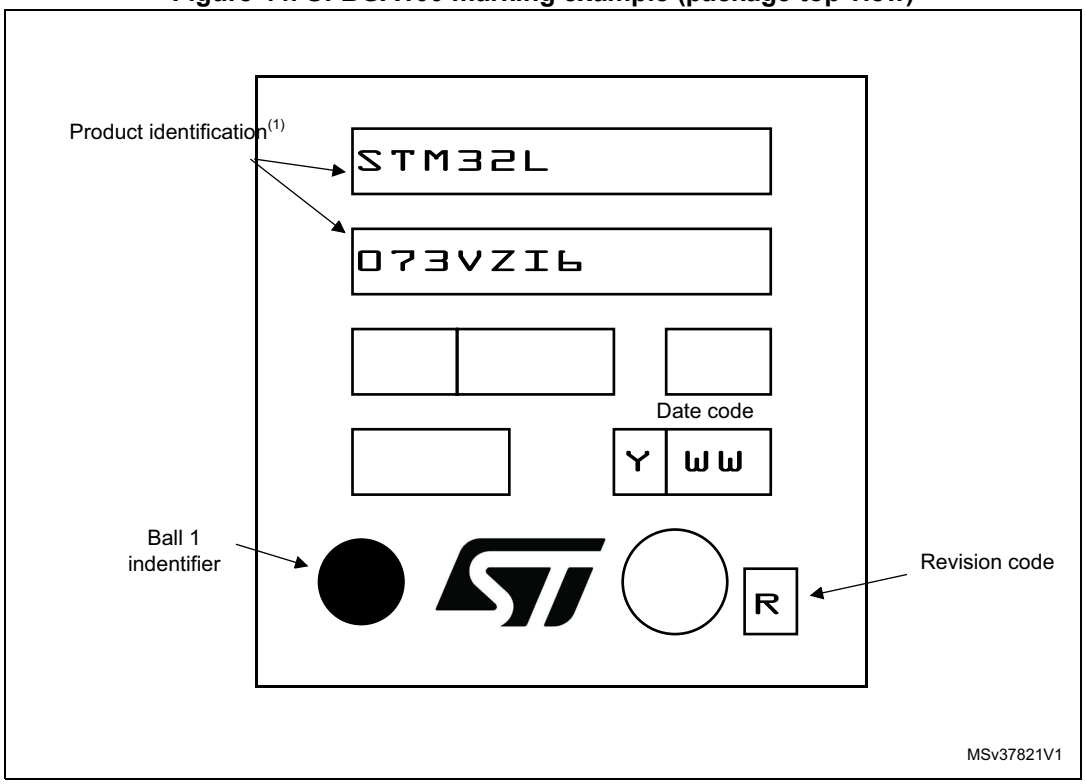
**Table 82. LCD controller characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{LCD}$ | LCD external voltage | - | - | 3.6 | V |
| $V_{LCD0}$ | LCD internal reference voltage 0 | - | 2.6 | - | |
| $V_{LCD1}$ | LCD internal reference voltage 1 | - | 2.73 | - | |
| $V_{LCD2}$ | LCD internal reference voltage 2 | - | 2.86 | - | |
| $V_{LCD3}$ | LCD internal reference voltage 3 | - | 2.98 | - | |
| $V_{LCD4}$ | LCD internal reference voltage 4 | - | 3.12 | - | |
| $V_{LCD5}$ | LCD internal reference voltage 5 | - | 3.26 | - | |
| $V_{LCD6}$ | LCD internal reference voltage 6 | - | 3.4 | - | |
| $V_{LCD7}$ | LCD internal reference voltage 7 | - | 3.55 | - | |
| $C_{ext}$ | $V_{LCD}$ external capacitance | 0.1 | - | 2 | µF |

### Device marking for UFBGA100

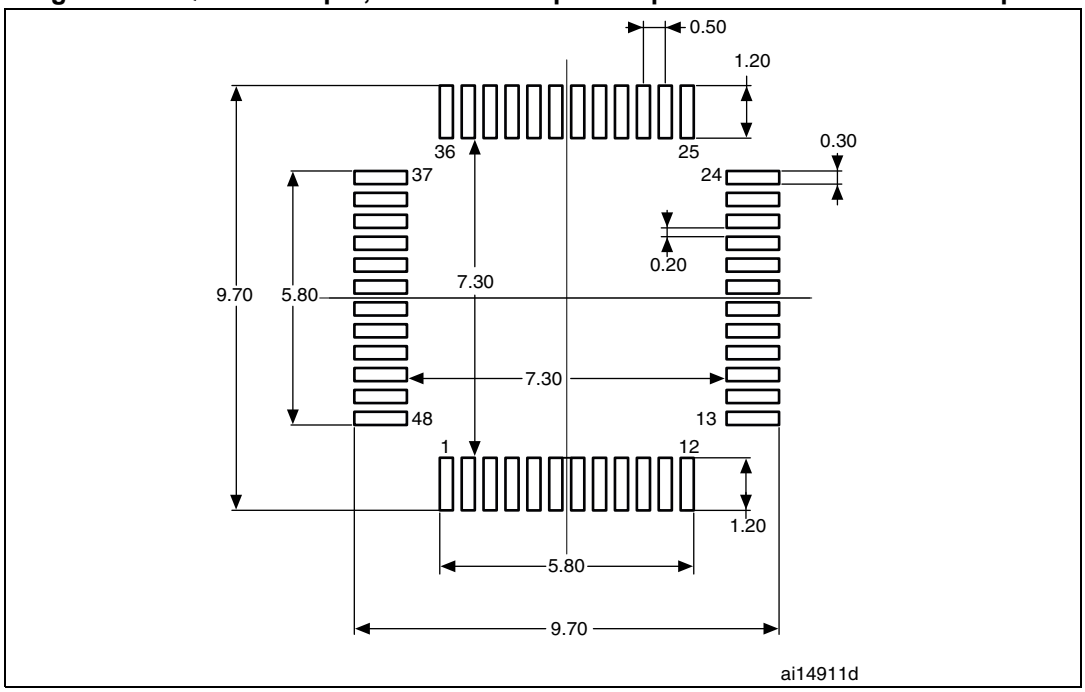
The following figure gives an example of topside marking versus ball A 1 position identifier location.

**Figure 44. UFBGA100 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

**Figure 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint**

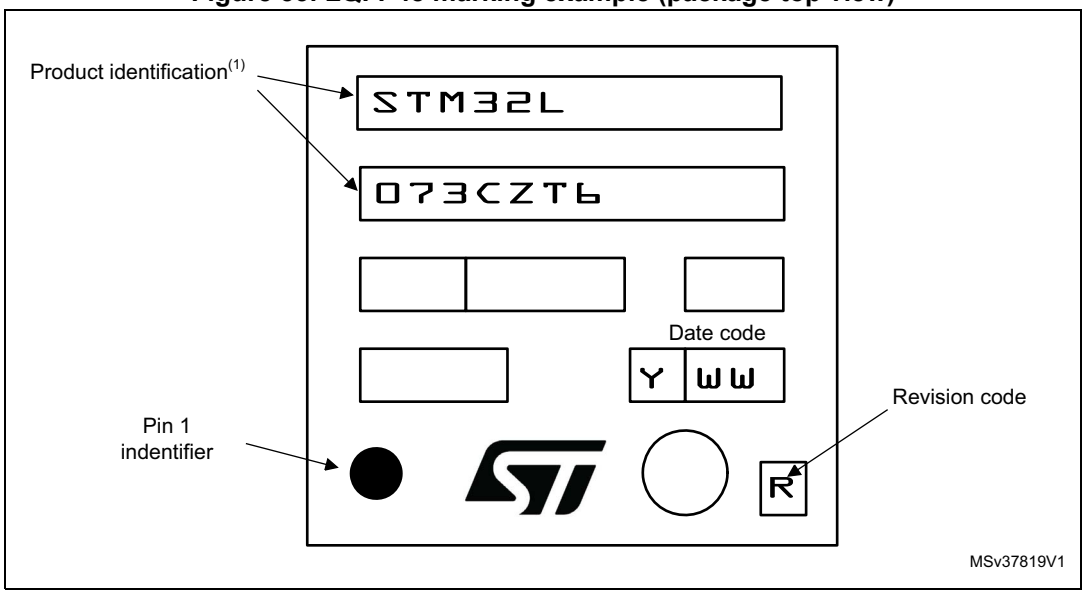



1. Dimensions are expressed in millimeters.

## Device marking for LQFP48

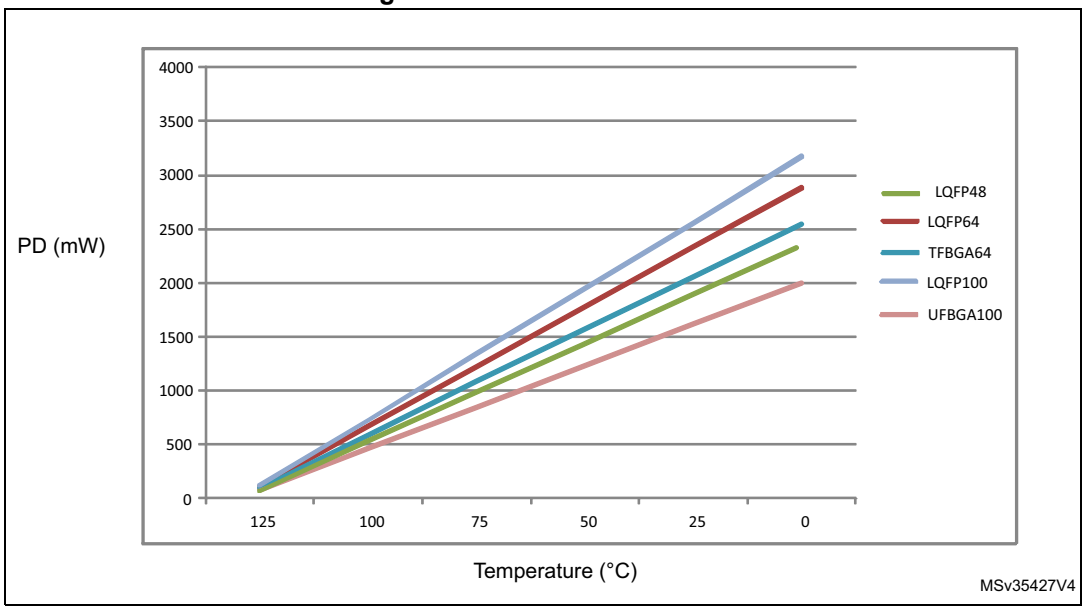
The following figure gives an example of topside marking versus pin 1 position identifier location.

**Figure 53. LQFP48 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

**Figure 54. Thermal resistance**




### 7.6.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.