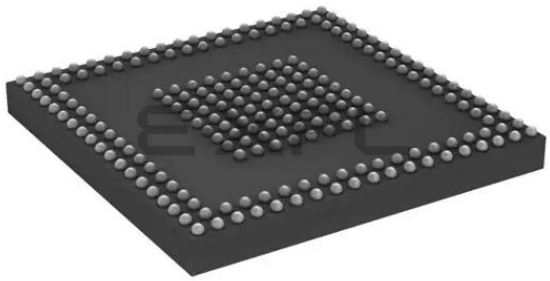

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	XCore
Core Size	32-Bit 8-Core
Speed	1000MIPS
Connectivity	Configurable
Peripherals	-
Number of I/O	73
Program Memory Size	128KB (32K x 32)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	217-LFBGA
Supplier Device Package	217-FBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xs1-u8a-128-fb217-c10

- **Channels and channel ends** Tasks running on logical cores communicate using channels formed between two channel ends. Data can be passed synchronously or asynchronously between the channel ends assigned to the communicating tasks. Section 7.5
- **xCONNECT Switch and Links** Between tiles, channel communications are implemented over a high performance network of xCONNECT Links and routed through a hardware xCONNECT Switch. Section 7.6
- **Ports** The I/O pins are connected to the processing cores by Hardware Response ports. The port logic can drive its pins high and low, or it can sample the value on its pins optionally waiting for a particular condition. Section 7.3
- **Clock blocks** xCORE devices include a set of programmable clock blocks that can be used to govern the rate at which ports execute. Section 7.4
- **Memory** Each xCORE Tile integrates a bank of SRAM for instructions and data, and a block of one-time programmable (OTP) memory that can be configured for system wide security features. Section 10
- **PLL** The PLL is used to create a high-speed processor clock given a low speed external oscillator. Section 8
- **USB** The USB PHY provides High-Speed and Full-Speed, device, host, and on-the-go functionality. Data is communicated through ports on the digital node. A library is provided to implement USB device functionality. Section 11
- **JTAG** The JTAG module can be used for loading programs, boundary scan testing, in-circuit source-level debugging and programming the OTP memory. Section 15

1.1 Software

Devices are programmed using C, C++ or xC (C with multicore extensions). XMOS provides tested and proven software libraries, which allow you to quickly add interface and processor functionality such as USB, Ethernet, PWM, graphics driver, and audio EQ to your applications.

1.2 xTIMEcomposer Studio

The xTIMEcomposer Studio development environment provides all the tools you need to write and debug your programs, profile your application, and write images into flash memory or OTP memory on the device. Because xCORE devices operate deterministically, they can be simulated like hardware within xTIMEcomposer: uniquely in the embedded world, xTIMEcomposer Studio therefore includes a static timing analyzer, cycle-accurate simulator, and high-speed in-circuit instrumentation.

xTIMEcomposer can be driven from either a graphical development environment, or the command line. The tools are supported on Windows, Linux and MacOS X and available at no cost from xmos.com/downloads. Information on using the tools is provided in the xTIMEcomposer User Guide, X3766.

Signal	Function	Type	Properties
USB_DP	USB Serial Data	I/O	
USB_ID	USB Device ID (OTG) - Reserved	Output	
USB_VBUS	USB Power Detect Pin	Input	

Clocks pins (4)			
Signal	**Function**	**Type**	**Properties**
MODE[4:0]	Boot mode select	Input	PU, ST
OSC_EXT_N	Use Silicon Oscillator	Input	ST
XI/CLK	Crystal Oscillator/Clock Input	Input	
XO	Crystal Oscillator Output	Output	

JTAG pins (5)			
Signal	**Function**	**Type**	**Properties**
DEBUG_N	Multi-chip debug	I/O	PU
TCK	Test clock	Input	PU, ST
TDI	Test data input	Input	PU, ST
TDO	Test data output	Output	PD, OT
TMS	Test mode select	Input	PU, ST

Misc pins (1)			
Signal	**Function**	**Type**	**Properties**
RST_N	Global reset input	Input	PU, ST

I/O pins (74)			
Signal	**Function**	**Type**	**Properties**
X0D00	$1A^{0}$	I/O	PD_S, R_S
X0D01	$1B^{0}$	I/O	PD_S, R_S
X0D10	$1C^{0}$	I/O	PD_S, R_S
X0D11	$1D^{0}$	I/O	PD_S, R_S
X0D12	$1E^{0}$	I/O	PD_S
X0D13	XLB^{4}_{out} $1F^{0}$	I/O	PD_S
X0D14	XLB^{3}_{out} $4C^{0}$ $8B^{0}$ $16A^{8}$ $32A^{28}$	I/O	PD_S
X0D15	XLB^{2}_{out} $4C^{1}$ $8B^{1}$ $16A^{9}$ $32A^{29}$	I/O	PD_S
X0D16	XLB^{1}_{out} $4D^{0}$ $8B^{2}$ $16A^{10}$	I/O	PD_S
X0D17	XLB^{0}_{out} $4D^{1}$ $8B^{3}$ $16A^{11}$	I/O	PD_S
X0D18	XLB^{0}_{in} $4D^{2}$ $8B^{4}$ $16A^{12}$	I/O	PD_S
X0D19	XLB^{1}_{in} $4D^{3}$ $8B^{5}$ $16A^{13}$	I/O	PD_S
X0D20	XLB^{2}_{in} $4C^{2}$ $8B^{6}$ $16A^{14}$ $32A^{30}$	I/O	PD_S

(continued)

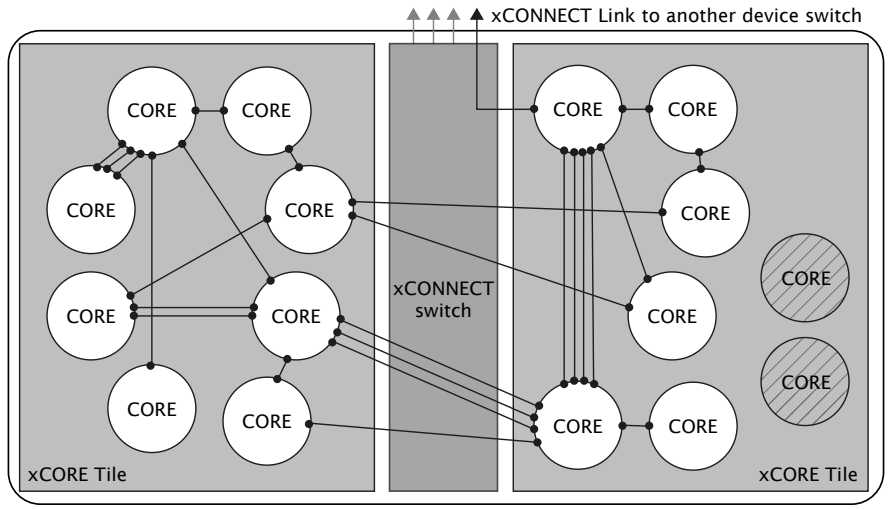

Figure 7: Switch, links and channel ends

between two switches. The switch has a routing algorithm that supports many different topologies, including lines, meshes, trees, and hypercubes.

The links operate in either 2 wires per direction or 5 wires per direction mode, depending on the amount of bandwidth required. Circuit switched, streaming and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between tiles (up to 313 MBit/s), but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-L Link Performance and Design Guide, X2999.

8 Oscillator

The oscillator block provides:

- An oscillator circuit. Together with an external resonator (crystal or ceramic), the oscillator circuit can provide a clock-source for both the real-time counter and the xCORE Tile. The external resonator can be chosen by the designer to have the appropriate frequency and accuracy. If desired, an external oscillator can be used on the XI/CLK input pin, this must be a 1.8 V oscillator.
- A 20 MHz silicon oscillator. This enables the device to boot and execute code without requiring an external crystal. The silicon oscillator is not as accurate as an external crystal.

9 Boot Procedure

The device is kept in reset by driving RST_N low. When in reset, all GPIO pins are high impedance. When the device is taken out of reset by releasing RST_N the processor starts its internal reset process. After approximately 750,000 input clocks, all GPIO pins have their internal pull-resistor enabled, and the processor boots at a clock speed that depends on MODE0 and MODE1.

The processor boot procedure is illustrated in Figure 9. In normal usage, MODE[4:2] controls the boot source according to the table in Figure 10. If bit 5 of the security register (*see* §10.1) is set, the device boots from OTP.

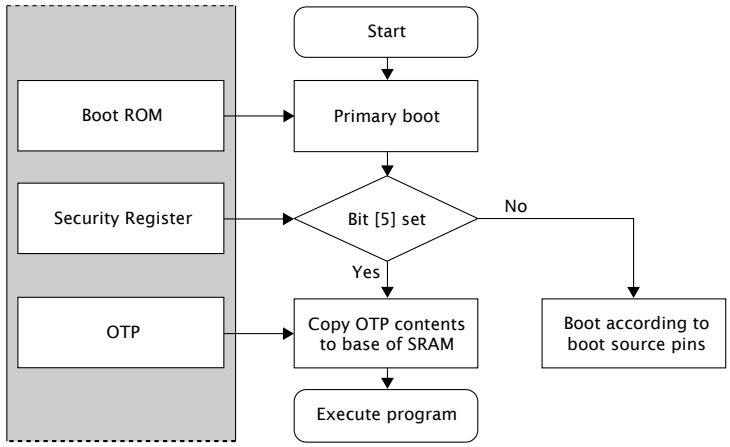

Figure 9: Boot procedure

MODE [4]	MODE [3]	MODE [2]	Boot Source
X	0	0	None: Device waits to be booted via JTAG
X	0	1	Reserved
0	1	0	Tile0 boots from link B, Tile1 from channel end 0 via Tile0
0	1	1	Tile0 boots from SPI, Tile1 from channel end 0 via Tile0
1	1	0	Tile0 and Tile1 independently enable link B and internal links (E, F, G, H), and boot from channel end 0
1	1	1	Tile0 and Tile 1 boot from SPI independently

Figure 10: Boot source pins

The boot image has the following format:

- A 32-bit program size s in words.
- Program consisting of $s \times 4$ bytes.
- A 32-bit CRC, or the value 0x0D15AB1E to indicate that no CRC check should be performed.

4. Input an END control token.
5. Output an END control token to the channel-end received in step 2.
6. Free channel-end 0.
7. Jump to the loaded code.

9.3 Boot from OTP

If an xCORE tile is set to use secure boot (see Figure 9), the boot image is read from address 0 of the OTP memory in the tile's security module.

This feature can be used to implement a secure bootloader which loads an encrypted image from external flash, decrypts and CRC checks it with the processor, and discontinues the boot process if the decryption or CRC check fails. XMOS provides a default secure bootloader that can be written to the OTP along with secret decryption keys.

Each tile has its own individual OTP memory, and hence some tiles can be booted from OTP while others are booted from SPI or the channel interface. This enables systems to be partially programmed, dedicating one or more tiles to perform a particular function, leaving the other tiles user-programmable.

9.4 Security register

The security register enables security features on the xCORE tile. The features shown in Figure 12 provide a strong level of protection and are sufficient for providing strong IP security.

10 Memory

10.1 OTP

Each xCORE Tile integrates 8 KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds data in four sectors each containing 512 rows of 32 bits which can be used to implement secure bootloaders and store encryption keys. Data for the security register is loaded from the OTP on power up. All additional data in OTP is copied from the OTP to SRAM and executed first on the processor.

The OTP memory is programmed using three special I/O ports: the OTP address port is a 16-bit port with resource ID 0x100200, the OTP data is written via a 32-bit port with resource ID 0x200100, and the OTP control is on a 16-bit port with ID 0x100300. Programming is performed through `libotp` and `xburn`.

10.2 SRAM

Each xCORE Tile integrates a single 64KB SRAM bank for both instructions and data. All internal memory is 32 bits wide, and instructions are either 16-bit or

Feature	Bit	Description
Disable JTAG	0	The JTAG interface is disabled, making it impossible for the tile state or memory content to be accessed via the JTAG interface.
Disable Link access	1	Other tiles are forbidden access to the processor state via the system switch. Disabling both JTAG and Link access transforms an xCORE Tile into a “secure island” with other tiles free for non-secure user application code.
Secure Boot	5	The processor is forced to boot from address 0 of the OTP, allowing the processor boot ROM to be bypassed (*see* §9).
Redundant rows	7	Enables redundant rows in OTP.
Sector Lock 0	8	Disable programming of OTP sector 0.
Sector Lock 1	9	Disable programming of OTP sector 1.
Sector Lock 2	10	Disable programming of OTP sector 2.
Sector Lock 3	11	Disable programming of OTP sector 3.
OTP Master Lock	12	Disable OTP programming completely: disables updates to all sectors and security register.
Disable JTAG-OTP	13	Disable all (read & write) access from the JTAG interface to this OTP.
Disable Global Debug	14	Disables access to the DEBUG_N pin.
	21..15	General purpose software accessable security register available to end-users.
	31..22	General purpose user programmable JTAG UserID code extension.

Figure 12: Security register features

32-bit. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one tile clock cycle. There is no dedicated external memory interface, although data memory can be expanded through appropriate use of the ports.

10.3 Deep Sleep Memory

The XS1-U8A-128-FB217 device includes 128 bytes of deep sleep memory for state storage during sleep mode. Deep sleep memory is volatile and if device input power is remove, the data will be lost.

11 USB PHY

The USB PHY provides High-Speed and Full-Speed, device, host, and on-the-go functionality. The PHY is configured through a set of peripheral registers (Appendix F), and data is communicated through ports on the digital node. A library, libxud_s.a, is provided to implement USB device functionality.

16 Board Integration

XS1-U8A-128-FB217 devices are optimized for layout on low cost PCBs using standard design rules. Careful layout is required to maximize the device performance. XMOS therefore recommends that the guidelines in this section are followed when laying out boards using the device.

The XS1-U8A-128-FB217 includes two DC-DC buck converters that take input voltages between 3.3-5V and output the 1.8V and 1.0V circuits required by the digital core and analogue peripherals. The DC-DC converters should have a 4.7uF X5R or X7R ceramic capacitor and a 100nF X5R or X7R ceramic capacitor on the VSUP input pins V7 and W7. These capacitors must be placed as close as possible to the those pins (within a maximum of 5mm), with the routing optimized to minimize the inductance and resistance of the traces.

The SW output pin must have an LC filter on the output with a 4.7uH inductor and 22uF X5R capacitor. The capacitor must have maximum ESR value of 0.015R, and the inductor should have a maximum DCR value of 0.07R. A list of suggested inductors is in Figure 19.

Figure 19: Example 4.7 μH inductors

	Part number	Current	Max DCR	Package
Wurth	744043004	1550 mA	70 $m\Omega$	4.8 x 4.8 mm
Murata	LQH55DN4R7M03L	2700 mA	57 $m\Omega$	5750 (2220)

The traces from the SW output pins to the inductor and from the output capacitor back to the VDD pins must be routed to minimize the coupling between them.

The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

The VDDIO supply to the XS1-U8A-128-FB217 requires a 100nF X5R or X7R ceramic decoupling capacitor placed as close as possible to the supply pins. VDDIO_OUT is the switched IO supply; it is only supplied when the chip is AWAKE. This pin can be used to provide extra decoupling, or it can be used to switch other devices off during sleep mode, for example a SPI flash. No more than 240 mA should be drawn on VDDIO at any time: this includes any supply sourced statically (e.g., driving a LED from a GPIO pin), any dynamic power consumption (e.g., toggling a GPIO pin at a high frequency) and any devices powered through VDDIO_OUT.

If the ADC Is used, it requires a 100nF X5R or X7R ceramic decoupling capacitor placed as close as possible to the AVDD pin. Care should be taken to minimize noise on these inputs, and if necessary an extra 10uF decoupling capacitor and ferrite bead can be used to remove noise from this supply.

The crystal oscillator requires careful routing of the XI / XO nodes as these are high impedance and very noise sensitive. Hence, the traces should be as wide and short as possible, and routed over a continuous ground plane. They should not be routed near noisy supply lines or clocks. The device has a load capacitance of

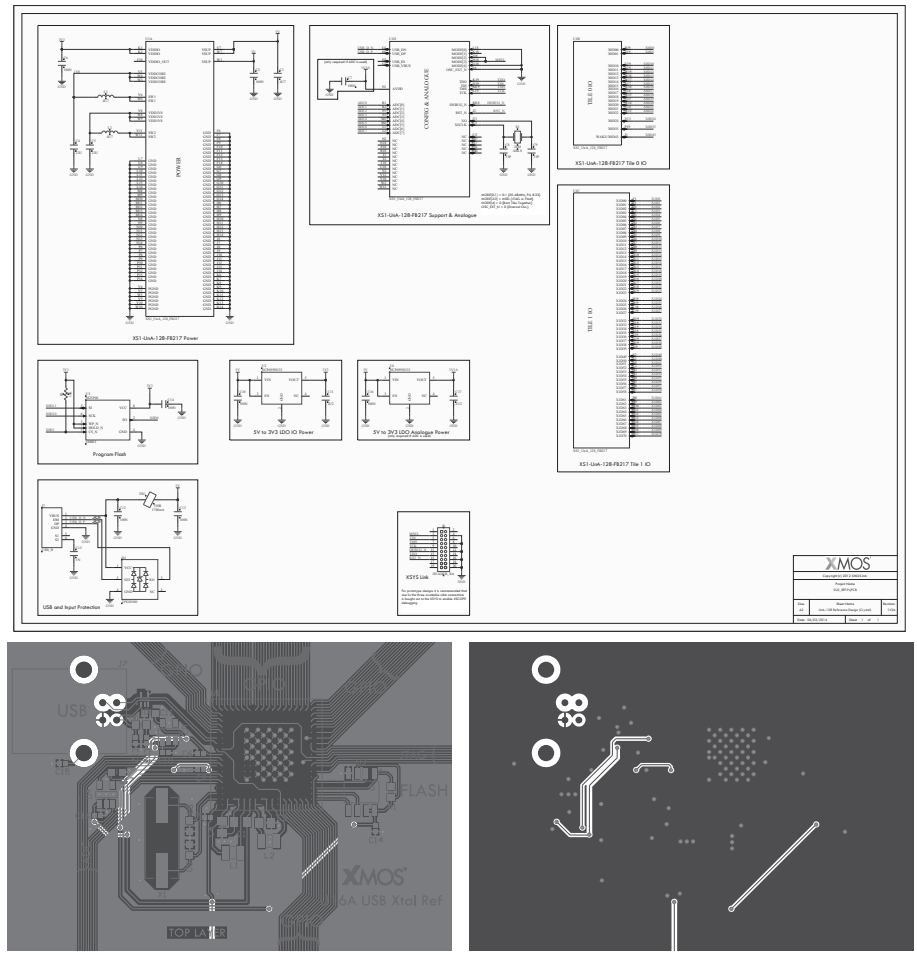

Figure 23: Example XTAL schematic, with top and bottom layout of a 2-layer PCB

18 DC and Switching Characteristics

18.1 Operating Conditions

Figure 26: Operating conditions

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VSUP	Power Supply (3.3V Mode)	3.00	3.30	3.60	V	
	Power Supply (5V Mode)	4.50	5.00	5.50	V	
VDDIO	I/O supply voltage	3.00	3.30	3.60	V	
AVDD	Analog Supply and Reference Voltage	3.00	3.30	3.60	V	
Cl	xCORE Tile I/O load capacitance			25	pF	
Ta	Ambient operating temperature (Commercial)	0		70	°C	
	Ambient operating temperature (Industrial)	-40		85	°C	
Tj	Junction temperature			125	°C	
Tstg	Storage temperature	-65		150	°C	

18.2 DC1 Characteristics

Figure 27: DC1 characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDDCORE	Tile Supply Voltage	0.95	1.00	1.05	V	
V(RIPPLE)	Ripple Voltage (peak to peak)		10	40	mV	
V(ACC)	Voltage Accuracy	-5		5	%	A
F(S)	Switching Frequency		1		MHz	
F(SVAR)	Variation in Switching Frequency	-10		10	%	
Effic	Efficiency		80		%	
PGT(HIGH)	Powergood Threshold (High)		95		%/VDDCORE	
PGT(LOW)	Powergood Threshold (Low)		80		%/VDDCORE	

A If supplied externally.

18.3 DC2 Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDD1V8	1V8 Supply Voltage		1.80		V	
V(RIPPLE)	Ripple Voltage (peak to peak)		10	40	mV	
V(ACC)	Voltage Accuracy	-5		5	%	A
F(S)	Switching Frequency		1		MHz	
F(SVAR)	Variation in Switching Frequency	-10		10	%	
Effic	Efficiency		80		%	
PGT(HIGH)	Powergood Threshold (High)		95		%/VDD1V8	
PGT(LOW)	Powergood Threshold (Low)		80		%/VDD1V8	

Figure 28: DC2 characteristics

A If supplied externally.

18.4 ADC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
N	Resolution		12		bits	
Fs	Conversion Speed			1	MSPS	
Nch	Number of Channels		8			
Vin	Input Range	0		AVDD	V	
DNL	Differential Non Linearity	-1		1.5	LSB	
INL	Integral Non Linearity	-4		4	LSB	
E(GAIN)	Gain Error	-10		10	LSB	
E(OFFSET)	Offset Error	-3		3	mV	
T(PWRUP)	Power time for ADC Clock Fclk			7	1/Fclk	
ENOB	Effective Number of bits		10			

Figure 29: ADC characteristics

18.5 USB Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VBUS	Power supply	0	5	5.25	V	A
ID	Device ID (OTG)	0		3.3	V	
DP	Data positive	0		3.3	V	
DN	Data negative (inverted)	0		3.3	V	

Figure 30: USB characteristics

A The VBUS pin is used for measuring the VBUS voltage only.

Contact XMOS for further details on USB characteristics.

18.14 xConnect Link Performance

Figure 39: Link performance

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
B(2blinkP)	2b link bandwidth (packetized)			103	MBit/s	A, B
B(5blinkP)	5b link bandwidth (packetized)			271	MBit/s	A, B
B(2blinkS)	2b link bandwidth (streaming)			125	MBit/s	B
B(5blinkS)	5b link bandwidth (streaming)			313	MBit/s	B

A Assumes 32-byte packet in 3-byte header mode. Actual performance depends on size of the header and payload.

B 7.5 ns symbol time.

The asynchronous nature of links means that the relative phasing of CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

18.15 JTAG Timing

Figure 40: JTAG timing

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f(TCK_D)	TCK frequency (debug)			TBC	MHz	
f(TCK_B)	TCK frequency (boundary scan)			TBC	MHz	
T(SETUP)	TDO to TCK setup time	TBC			ns	A
T(HOLD)	TDO to TCK hold time	TBC			ns	A
T(DELAY)	TCK to output delay			TBC	ns	B

A Timing applies to TMS and TDI inputs.

B Timing applies to TDO output from negative edge of TCK.

All JTAG operations are synchronous to TCK.

B.1 RAM base address: 0x00

This register contains the base address of the RAM. It is initialized to 0x00010000.

0x00: RAM base address

Bits	Perm	Init	Description
31:2	RW		Most significant 16 bits of all addresses.
1:0	RO	-	Reserved

B.2 Vector base address: 0x01

Base address of event vectors in each resource. On an interrupt or event, the 16 most significant bits of the destination address are provided by this register; the least significant 16 bits come from the event vector.

0x01: Vector base address

Bits	Perm	Init	Description
31:16	RW		The most significant bits for all event and interrupt vectors.
15:0	RO	-	Reserved

B.3 xCORE Tile control: 0x02

Register to control features in the xCORE tile

0x02: xCORE Tile control

Bits	Perm	Init	Description
31:6	RO	-	Reserved
5	RW	0	Set to 1 to select the dynamic mode for the clock divider when the clock divider is enabled. In dynamic mode the clock divider is only activated when all active logical cores are paused. In static mode the clock divider is always enabled.
4	RW	0	Set to 1 to enable the clock divider. This slows down the xCORE tile clock in order to use less power.
3:0	RO	-	Reserved

B.4 xCORE Tile boot status: 0x03

This read-only register describes the boot status of the xCORE tile.

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:24	RO		00 - ChannelEnd, 01 - ERROR, 10 - PSCTL, 11 - Idle.
23:16	RO		Based on SRC_TARGET_TYPE value, it represents channelEnd ID or Idle status.
15:6	RO	-	Reserved
5:4	RO		Two-bit network identifier
3	RO	-	Reserved
2	RO		1 when the current packet is considered junk and will be thrown away.
1	RO	0	Set to 1 if the switch is routing data into the link, and if a route exists from another link.
0	RO	0	Set to 1 if the link is routing data into the switch, and if a route is created to another link on the switch.

0x10 .. 0x13: PLink status

C.9 Debug scratch: 0x20 .. 0x27

A set of registers used by the debug ROM to communicate with an external debugger, for example over the switch. This is the same set of registers as the Debug Scratch registers in the processor status.

0x20 .. 0x27: Debug scratch

Bits	Perm	Init	Description
31:0	CRW		Value.

C.10 PC of logical core 0: 0x40

Value of the PC of logical core 0.

0x40: PC of logical core 0

Bits	Perm	Init	Description
31:0	RO		Value.

0x04: Node configuration register

Bits	Perm	Init	Description
31	RW	0	Set to 1 to disable further updates to the node configuration and link control and status registers.
30:1	RO	-	Reserved
0	RW	0	Header mode. 0: 3-byte headers; 1: 1-byte headers.

E.3 Node identifier: 0x05

0x05: Node identifier

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RW	0	16-bit node identifier. This does not need to be set, and is present for compatibility with XS1-switches.

E.4 Reset and Mode Control: 0x50

The XS1-S has two main reset signals: a system-reset and an xCORE Tile-reset. System-reset resets the whole system including external devices, whilst xCORE Tile-reset resets the xCORE Tile(s) only. The resets are induced either by software (by a write to the register below) or by one of the following:

* External reset on RST_N (System reset)

* Brown out on one of the power supplies (System reset)

* Watchdog timer (System reset)

* Sleep sequence (xCORE Tile reset)

* Clock source change (xCORE Tile reset)

The minimum system reset duration is achieved when the fastest permissible clock is used. The reset durations will be proportionately longer when a slower clock is used. Note that the minimum system reset duration allows for all power rails except the VOUT2 to turn off, and decay.

The length of the system reset comes from an internal counter, counting 524,288 oscillator clock cycles which gives the maximum time allowable for the supply rails to discharge. The system reset duration is a balance between leaving a long time for the supply rails to discharge, and a short time for the system to boot. Example reset times are 44 ms with a 12 MHz oscillator or 5.5 ms with a 96 MHz oscillator.

0x2C: UIFM PID

Bits	Perm	Init	Description
31:4	RO	-	Reserved
3:0	RO	0	Value of the last received PID.

F.13 UIFM Endpoint: 0x30

The last endpoint seen

0x30: UIFM Endpoint

Bits	Perm	Init	Description
31:5	RO	-	Reserved
4	RO	0	1 if endpoint contains a valid value.
3:0	RO	0	A copy of the last received endpoint.

F.14 UIFM Endpoint match: 0x34

This register can be used to mark UIFM endpoints as special.

0x34: UIFM Endpoint match

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RW	0	This register contains a bit for each endpoint. If its bit is set, the endpoint will be supplied on the RX port when ORed with 0x10.

F.15 UIFM power signalling: 0x38

0x38: UIFM power signalling

Bits	Perm	Init	Description
31:9	RO	-	Reserved
8	RW	0	Valid
7:0	RW	0	Data

Bits	Perm	Init	Description
31:25	RO	-	Reserved
24	RO	1	Indicates that an ADC sample has been dropped. This bit is cleared on a read.
23:18	RO	-	Reserved
17:16	RW	1	Number of bits per ADC sample. The ADC values are always left aligned: 0: 8 bits samples - the least significant four bits of each sample are discarded. 1: 16 bits samples - the sample is padded with four zero bits in bits 3..0. The most significant byte is transmitted first. 2: reserved 3: 32 bits samples - the sample is padded with 20 zero bits in bits 19..0. The most significant byte is transmitted first, hence the word can be input with a single 32-bit IN instruction.
15:8	RW	1	Number of samples to be transmitted per packet. The value 0 indicates that the packet will not be terminated until interrupted by an ADC control register access.
7:2	RO	-	Reserved
1	RW	0	Set to 1 to switch the ADC to sample a 0.8V signal rather than the external voltage. This can be used to calibrate the ADC. When switching to and from calibration mode, one sample value should be discarded. If a sample value `x` is measured in calibration mode, then a scale factor `800000/x` can be used to translate subsequent measurements into microvolts (using integer arithmetic).
0	RW	0	Set to 1 to enable the ADC. Note that when enabled, the ADC control registers above are read-only. The ADC must be disabled whilst setting up the per-input-pin control. On enabling the ADC, six pulses must be generated to calibrate the ADC. These pulses will not generate packets on the selected channel-end. The seventh and further pulses will deliver samples to the selected channel-end. These six pulses have to be issued every time that this bit is changed from 0 to 1.

0x20: ADC General Control

H Deep sleep memory Configuration

This peripheral contains a 128 byte RAM that retains state whilst the main processor is put to sleep.

The *Deep sleep memory* is peripheral 3. The control registers are accessed using 8-bit reads and writes (use `write_periph_8(device, 3, ...)` and `read_periph_8 ↪ (device, 3, ...)` for reads and writes).

0x00: General control

Bits	Perm	Init	Description
31:10	RO	-	Reserved
9	RW	0	Set to 1 to switch USB suspend controller to USB power up enable.
8	RW	0	Set to 1 to switch USB suspend controller to power down enable.
7	RW	0	By default, when waking up, the voltage levels stored in the LEVEL CONTROL registers are used. Set to 1 to use the power-on voltage levels.
6	WO		Set to 1 to re-apply the current contents of the AWAKE state. Use this when the program has changed the contents of the AWAKE state register. Self clearing.
5	RW	0	Set to 1 to use a 64-bit timer.
4	RW	0	Set to 1 to wake-up on the timer.
3	RW	1	If waking on the WAKE pin is enabled (see above), then by default the device wakes up when the WAKE pin is pulled high. Set to 0 to wake-up when the WAKE pin is pulled low.
2	RW	0	Set to 1 to wake-up when the WAKE pin is at the right level.
1	RW	0	Set to 1 to initiate sleep sequence - self clearing. Only set this bit when in AWAKE state.
0	RW	0	Sleep clock select. Set to 1 to use the default clock rather than the internal 31.25 kHz oscillator. Note: this bit is only effective in the ASLEEP state.

K.2 Time to wake-up, least significant 32 bits: 0x04

This register stores the time to wake-up. The value is only used if wake-up from the real-time clock is enabled, and the device is asleep.

0x04: Time to wake-up, least significant 32 bits

Bits	Perm	Init	Description
31:0	RW	0	Least significant 32 bits of time to wake-up.

K.3 Time to wake-up, most significant 32 bits: 0x08

This register stores the time to wake-up. The value is only used if wake-up from the real-time clock is enabled, if 64-bit comparisons are enabled, and the device is asleep. In most cases, 32-bit comparisons suffice.

0x18: Power supply states whilst AWAKE

Bits	Perm	Init	Description
31:15	RO	-	Reserved
14	RW	0	Set to 1 to disable clock to the xCORE Tile.
13:10	RO	-	Reserved
9	RW	0	Sets modulation used by DCDC2: 0: PWM modulation (max 475 mA) 1: PFM modulation (max 50 mA)
8	RW	0	Sets modulation used by DCDC1: 0: PWM modulation (max 700 mA) 1: PFM modulation (max 50 mA)
7:6	RO	-	Reserved
5	RW	1	Set to 1 to enable VOUT6 (IO supply).
4	RW	1	Set to 1 to enable LDO5 (core PLL supply).
3:2	RO	-	Reserved
1	RO	1	Set to 1 to enable DCDC2 (analogue supply).
0	RW	1	Set to 1 to enable DCDC1 (core supply).

K.8 Power supply states whilst SLEEPING1: 0x1C

This register controls what state the power control block should be in when in the SLEEPING1 state. It also defines the time that the system shall stay in this state.

Bits	Perm	Init	Description
31:30	RO	-	Reserved
29	RO	0	1 if VOUT6 was enabled in the previous state.
28	RO	0	1 if LDO5 was enabled in the previous state.
27:26	RO	-	Reserved
25	RO	1	1 if DCDC2 was enabled in the previous state.
24	RO	0	1 if DCDC1 was enabled in the previous state.
23:19	RO	-	Reserved
18:16	RO		Current state of the power sequence state machine 0: Reset 1: Asleep 2: Waking 1 3: Waking 2 4: Awake Wait 5: Awake 6: Sleeping 1 7: Sleeping 2
15	RO	-	Reserved
14	RO	0	Set to 1 to disable clock to the xCORE Tile.
13:10	RO	-	Reserved
9	RO	0	Sets modulation used by DCDC2: 0: PWM modulation (max 475 mA) 1: PFM modulation (max 50 mA)
8	RO	0	Sets modulation used by DCDC1: 0: PWM modulation (max 700 mA) 1: PFM modulation (max 50 mA)
7:6	RO	-	Reserved
5	RO	0	Set to 1 to enable VOUT6 (IO supply).
4	RO	0	Set to 1 to enable LDO5 (core PLL supply).
3:2	RO	-	Reserved
1	RO	0	Set to 1 to enable DCDC2 (analogue supply).
0	RO	0	Set to 1 to enable DCDC1 (core supply).

0x24: Power sequence status

K.11 DCDC control: 0x2C

This register controls the two DC-DC converters.

R Revision History

Date	Description
2013-01-30	New datasheet - revised part numbering
2013-02-26	New multicore microcontroller introduction Moved configuration sections to appendices
2013-03-27	Added connection details for USB_VBUS/USB_ID - Section 11 VDDCORE parameters - Section 18.2
2013-04-04	Added ADC control pin configuration details 4-7 - Section G
2013-04-16	OSC_REF_EXT_N Properties - Section 4 Sleep mode requirements include JTAG - Section 14.4
2013-07-19	Updated Features list with available ports and links - Section 2 Simplified link bits in Signal Description - Section 4 New JTAG, xSCOPE and Debugging appendix - Section M New Schematics Design Check List - Section N New PCB Layout Design Check List - Section O Updated USB_VBUS pin connection - Section 11
2013-09-16	Pitch 0.8mm - Section 2
2013-12-09	Added Industrial Ambient Temperature - Section 18.1 Annotated V(ACC) parameter - Section 18.2 Updated V(IH) parameter - Section 18.10 Updated V(OH) parameter - Section 18.6
2014-03-07	VSUP input pins corrected to V7 and W7 - Section 16 USB_D_P/N corrected in example schematics and board layout - Section 17
2014-03-25	Added footnotes to DC and Switching Characteristics - Section 18
2014-06-25	New PCB guidelines for high-speed USB designs - Section 16.2
2014-08-29	Moved USB pin data to Section 16.1; added additional PHY information Added USB characterisation data - Section 18.5
2015-04-14	Updated Introduction - Section 1; Pin Configuration - Section 3; Signal Description - Section 4