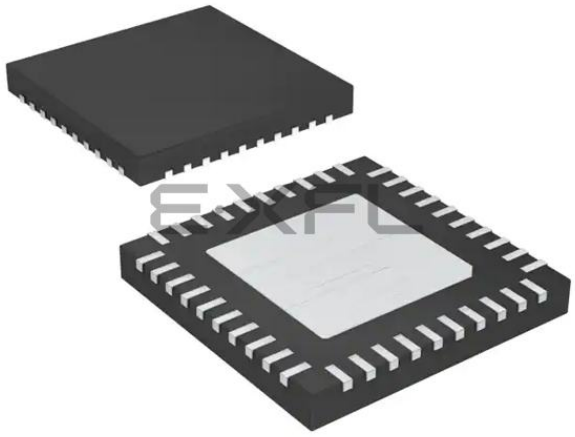
Analog Devices Inc./Maxim Integrated - MAXQ7670ATL+T Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	7
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-TQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq7670atl-t

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

ABSOLUTE MAXIMUM RATINGS

DVDD to DGND .....-0.3V to +3V
DVDDIO to GNDIO .....-0.3V to +5.5V
AVDD to AGND .....-0.3V to +4V
DGND to GNDIO. .....-0.3V to +0.3V
GNDIO to AGND. .....-0.3V to +0.3V
AGND to DGND.....-0.3V to +0.3V
Analog Inputs to AGND.....-0.3V to (V_{AVDD} + 0.3V)
$\overline{RESET}$, Digital Inputs/Outputs to GNDIO .....-0.3V to (V_{DVDDIO} + 0.3V)
XIN, XOUT to DGND .....-0.3V to (V_{DVDD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 36mW/°C above +70°C) 2857mW
Continuous Current into Any Pin.....±50mA
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage Ranges	DVDD	$\overline{REGEN2}$ = DVDDIO, $DV_{DD} \le AV_{DD}$, $DV_{DD} \le DV_{DDIO}$	2.25	2.5	2.75	V
	AVDD	LRAPD = 1, $AV_{DD} \le DV_{DDIO}$	3.0	3.3	3.6	
	DVDDIO		4.5	5.0	5.25	
AVDD Supply Current	I_{AVDD}	Shutdown (Note 2)		3	10	µA
		All analog functions enabled		6	7	mA
Analog Module Incremental Subfunction Supply Current	ΔI_{AVDD}	ADC, 50ksps, 4MHz ADCCLK		5200		µA
		ADC, 250ksps, 4MHz ADCCLK		5600		
		AVDD brownout interrupt monitor		3		
		PGA enabled		5500		
DVDD Supply Current	I_{DVDD}	CPU in stop mode, all peripherals disabled		25	200	µA
		High speed/2MHz mode (Note 3)		2.0	2.5	mA
		High speed/16MHz mode (Note 4)		11.3		
		Low speed/625kHz mode (Note 5)		0.95		
		Program flash erase or write		14	23	
Digital Peripheral Incremental Subfunction Supply Current	ΔI_{DVDD}	DVDDIO brownout reset monitor		1		µA
		HF crystal oscillator		60		
		Internal fixed-frequency oscillator		50		
DVDDIO Supply Current	I_{DVDDIO}	All digital I/Os static at GNDIO or DV_{DDIO}		2	20	µA
		CAN transmitting, timer output switching (Note 6)		0.2	0.3	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MEMORY SECTION						
Flash Memory Size		Program or data storage		64		KB
Flash Page Size		16-bit word size		256		Words
Flash Erase/Write Endurance		Program or data (Note 7)	10,000			Cycles
Flash Data Retention (Note 7)		All flash, T_A = +25°C	100			Years
		All flash, T_A = +85°C	15			
Flash Erase Time		Flash page erase	20		50	ms
		Entire flash mass erase	200		500	
Flash Programming Time		Flash single word programming	20		40	µs
		Entire flash programming	0.66		1.31	s
RAM Memory Size				2		KB
Utility ROM Size		16-bit word size		4		KWords
ANALOG SENSE PATH (Includes PGA and ADC)						
Resolution	N_{ADC}	No missing codes	10			Bits
Integral Nonlinearity	INL_{ADC}	PGA gain = 16V/V, bipolar mode, V_{IN} = ±100mV, 150.9ksps		±0.5	±1	LSB_{10}
		PGA gain = 1V/V, unipolar mode, V_{IN} = +1.0V, 250ksps		±0.4	±1	
Differential Nonlinearity	DNL_{ADC}	PGA gain = 1V/V or 16V/V		±0.4	±1	LSB_{10}
Input-Referred Offset Error		Test at T_A = +25°C, PGA gain = 1V/V or 16V/V		±1	±10	mV
Offset-Error Temperature Coefficient		PGA gain = 16V/V, bipolar mode		±2		µV/°C
Gain Error		PGA gain = 16V/V, bipolar mode, excludes offset and reference error, test at T_A = +25°C	-2		+2	%
Gain-Error Temperature Coefficient		PGA gain = 16V/V, bipolar mode		±5		ppm/°C
Conversion Clock Frequency	f_{ADCCLK}	f_{SYSCLK} = 8MHz or 16MHz	0.5		4.0	MHz
Sample Rate	f_{SAMPLE}	PGA gain = 16V/V, f_{ADCCLK} = 4MHz			150.9	ksps
		PGA gain = 1V/V, f_{ADCCLK} = 4MHz			250	
Channel Select, Track-and-Hold Acquisition Time	t_{ACQ}	PGA gain = 16V/V, 13.5 ADCCLK cycles at 4MHz		3.375		µs
		PGA gain = 1V/V, three ADCCLK cycles at 4MHz		0.75		
Conversion Time	t_{CONV}	13 ADCCLK cycles at 4MHz		3.25		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Capacitance		I/O pins three-state		15		pF
Maximum Output Impedance		PD0._ = 0		880		Ω
		PD0._ = 1		450		
SYSTEM CLOCK						
System Clock Frequency	f_{SYSCLK}	From any clock source	0		16.67	MHz
SPI INTERFACE TIMING						
SPI Master Operating Frequency	f_{MCLK}	0.5 x f_{SYSCLK}			8	MHz
SPI Slave Mode Operating Frequency	f_{SCLK}				$f_{SYSCLK}/8$	MHz
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		t_{SYSCLK} - 25			ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}		t_{SYSCLK}			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		t_{SYSCLK} - 25			ns
MOSI Output Setup Time to SCLK Sample Edge	t_{MOS}		t_{SYSCLK} - 25			ns
MISO Input Setup Time to SCLK Sample Edge	t_{MIS}		30			ns
MISO Input Hold Time After SCLK Sample Edge	t_{MIH}		0			ns
SCLK Inactive to MOSI Inactive	t_{MLH}		t_{SYSCLK} - 25			ns
MOSI Input Setup Time to SCLK Sample Edge	t_{SIS}		30			ns
MOSI Input Hold Time After SCLK Sample Edge	t_{SIH}		t_{SYSCLK} + 25			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				3 t_{SYSCLK} + 25	ns
MISO Output Disabled After $\overline{SS}$ Edge Rise	t_{SLH}				2 t_{SYSCLK} + 50	ns
$\overline{SS}$ Falling Edge to MISO Active	t_{SOE}		2 t_{SYSCLK} + 2.5			ns

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SS}$ Falling Edge to First SCLK Sample Edge	t_{SSE}		2 t_{SYSCLK} + 5			ns
SCLK Inactive to $\overline{SS}$ Rising Edge	t_{SD}		t_{SYSCLK} + 10			ns
Minimum $\overline{CS}$ Pulse Width	t_{SCW}		t_{SYSCLK} + 10			ns

Note 1: All devices are 100% production tested at T_A = +25°C and +125°C. Temperature limits to T_A = -40°C are guaranteed by design.

Note 2: All analog functions disabled and all digital inputs connected to supply or ground.

Note 3: High-speed/8 mode without CAN; V_{DVDD} = +2.5V, CPU and 16-bit timer running at 2MHz from an external, 16MHz crystal oscillator; all other peripherals disabled; all digital I/Os static at V_{DVDDIO} or GNDIO; T_A = T_{MIN} to T_{MAX}.

Note 4: High-speed/1 mode with CAN; V_{DVDD} = +2.5V, CPU and 16-bit timer running at 16MHz from an external, 16MHz crystal oscillator; CAN enabled and communicating at 500kbps; all other peripherals disabled, all digital I/Os (except CANTXD and CANRXD) static at V_{DVDDIO} or GNDIO, T_A = T_{MIN} to T_{MAX}.

Note 5: Low speed, PMM1 mode without CAN; V_{DVDD} = +2.5V, CPU and one timer running from an external, 16MHz crystal oscillator in PMM1 mode; all other peripherals disabled; all digital I/Os static at V_{DVDDIO} or GNDIO, T_A = T_{MIN} to T_{MAX}.

Note 6: CAN transmitting at 500kbps; 16-bit timer output switching at 500kHz; all active I/Os are loaded with a 20pF capacitor; all remaining digital I/Os are static at V_{DVDDIO} or GNDIO, T_A = T_{MIN} to T_{MAX}.

Note 7: Guaranteed by design and characterization.

Note 8: This is not a static capacitance. It is the capacitance presented to the analog input when the T/H amplifier is in sample mode.

Note 9: The switched capacitor on the REFADC input can disturb the reference voltage. To reduce this disturbance, place a 0.1µF capacitor from REFADC to AGND as close as possible to REFADC.

Note 10: The digital design is fully static. However, the lower clock limit is set by a clock detect circuit. The MAXQ7670 switches to the internal RC clock if the external input goes below 166kHz. This clock detect circuit also acts to detect a crystal failure when a crystal is used.

Table 5. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM	—	—	—	—	CRTMS	CRTM	TESTCAN	—	DCW	FTEST	DOFF	—	SRT	—	SCANMODE	TME
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0C	—	—	—	—	—	—	—	—	ERIE	STIE	PDE	SIESTA	CRST	AUTOB	ERCS	SWINT
	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
C0S	—	—	—	—	—	—	—	—	BSS	EC96/128	WKS	RXS	TXS	ER2	ER1	ER0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0IR	—	—	—	—	—	—	—	—	INTIN7	INTIN6	INTIN5	INTIN4	INTIN3	INTIN2	INTIN1	INTIN0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0TE	—	—	—	—	—	—	—	—	C0TE.7	C0TE.6	C0TE.5	C0TE.4	C0TE.3	C0TE.2	C0TE.1	C0TE.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0RE	—	—	—	—	—	—	—	—	C0RE.7	C0RE.6	C0RE.5	C0RE.4	C0RE.3	C0RE.2	C0RE.1	C0RE.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0R	—	—	—	—	—	—	—	—	CAN0BA	INCDEC	AID	C0BPR7	C0BPR6	—	C0BIE	C0IE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0DP	C0DP.15	C0DP.14	C0DP.13	C0DP.12	C0DP.11	C0DP.10	C0DP.9	C0DP.8	C0DP.7	C0DP.6	C0DP.5	C0DP.4	C0DP.3	C0DP.2	C0DP.1	C0DP.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0DB	C0DB.15	C0DB.14	C0DB.13	C0DB.12	C0DB.11	C0DB.10	C0DB.9	C0DB.8	C0DB.7	C0DB.6	C0DB.5	C0DB.4	C0DB.3	C0DB.2	C0DB.1	C0DB.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0RMS	—	C0RMS.15	C0RMS.14	C0RMS.13	C0RMS.12	C0RMS.11	C0RMS.10	C0RMS.9	C0RMS.8	C0RMS.7	C0RMS.6	C0RMS.5	C0RMS.4	C0RMS.3	C0RMS.2	C0RMS.1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0TMA	—	C0TMA.15	C0TMA.14	C0TMA.13	C0TMA.12	C0TMA.11	C0TMA.10	C0TMA.9	C0TMA.8	C0TMA.7	C0TMA.6	C0TMA.5	C0TMA.4	C0TMA.3	C0TMA.2	C0TMA.1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M1C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M2C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M3C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M4C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M5C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M6C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M7C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M8C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M9C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M10C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M11C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M12C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0