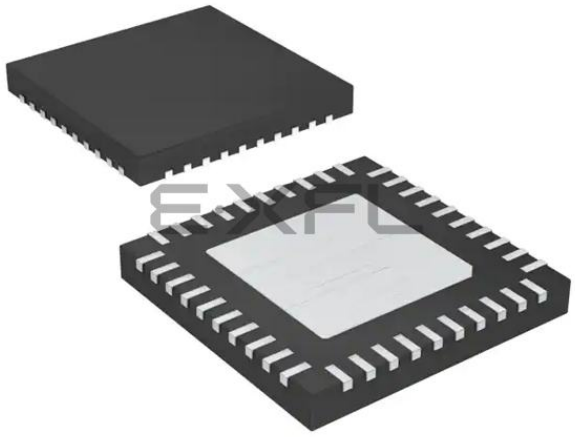
Analog Devices Inc./Maxim Integrated - MAXQ7670ATL/V+T Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	7
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-TQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq7670atl-v-t

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MEMORY SECTION						
Flash Memory Size		Program or data storage		64		KB
Flash Page Size		16-bit word size		256		Words
Flash Erase/Write Endurance		Program or data (Note 7)	10,000			Cycles
Flash Data Retention (Note 7)		All flash, T_A = +25°C	100			Years
		All flash, T_A = +85°C	15			
Flash Erase Time		Flash page erase	20		50	ms
		Entire flash mass erase	200		500	
Flash Programming Time		Flash single word programming	20		40	µs
		Entire flash programming	0.66		1.31	s
RAM Memory Size				2		KB
Utility ROM Size		16-bit word size		4		KWords
ANALOG SENSE PATH (Includes PGA and ADC)						
Resolution	N_{ADC}	No missing codes	10			Bits
Integral Nonlinearity	INL_{ADC}	PGA gain = 16V/V, bipolar mode, V_{IN} = ±100mV, 150.9ksps		±0.5	±1	LSB_{10}
		PGA gain = 1V/V, unipolar mode, V_{IN} = +1.0V, 250ksps		±0.4	±1	
Differential Nonlinearity	DNL_{ADC}	PGA gain = 1V/V or 16V/V		±0.4	±1	LSB_{10}
Input-Referred Offset Error		Test at T_A = +25°C, PGA gain = 1V/V or 16V/V		±1	±10	mV
Offset-Error Temperature Coefficient		PGA gain = 16V/V, bipolar mode		±2		µV/°C
Gain Error		PGA gain = 16V/V, bipolar mode, excludes offset and reference error, test at T_A = +25°C	-2		+2	%
Gain-Error Temperature Coefficient		PGA gain = 16V/V, bipolar mode		±5		ppm/°C
Conversion Clock Frequency	f_{ADCCLK}	f_{SYSCLK} = 8MHz or 16MHz	0.5		4.0	MHz
Sample Rate	f_{SAMPLE}	PGA gain = 16V/V, f_{ADCCLK} = 4MHz			150.9	ksps
		PGA gain = 1V/V, f_{ADCCLK} = 4MHz			250	
Channel Select, Track-and-Hold Acquisition Time	t_{ACQ}	PGA gain = 16V/V, 13.5 ADCCLK cycles at 4MHz		3.375		µs
		PGA gain = 1V/V, three ADCCLK cycles at 4MHz		0.75		
Conversion Time	t_{CONV}	13 ADCCLK cycles at 4MHz		3.25		µs

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Channel Select Plus Conversion Time	t_{ACQ} + t_{CONV}	PGA gain = 16V/V, 26.5 ADCCLK cycles at 4MHz		6.625		µs
		PGA gain = 1V/V, 16 ADCCLK cycles at 4MHz		4		
Turn-On Time	t_{RECOV}			10		µs
Aperture Delay				60		ns
Aperture Jitter				100		ps_{P-P}
Differential Input Voltage Range		At AIN0–AIN7, unipolar mode, PGA gain = 1V/V	0		V_{REFADC}	V
		At AIN0–AIN7, unipolar mode, PGA gain = 16V/V	0		0.125	
		At AIN0–AIN7, bipolar mode, PGA gain = 1V/V	$-V_{REFADC}$ /2		$+V_{REFADC}$ /2	
		At AIN0–AIN7, bipolar mode, PGA gain = 16V/V	$-V_{REFADC}$ /32		$+V_{REFADC}$ /32	
Absolute Input Voltage Range		At AIN0–AIN7	0		V_{AVDD}	V
Input Leakage Current		At AIN0–AIN7		±0.1		µA
Input-Referred Noise		At AIN0–AIN7, PGA gain = 16V/V		50		$µV_{RMS}$
		At AIN0–AIN7, PGA gain = 1V/V		400		
Small-Signal Bandwidth (-3dB)		V_{IN} = 12mV_{P-P}, PGA gain = 16V/V		33		MHz
		V_{IN} = 200mV_{P-P}, PGA gain = 1V/V		23		
Large-Signal Bandwidth (-3dB)		V_{IN} = 150mV_{P-P}, PGA gain =16V/V		33		MHz
		V_{IN} = 2.5V_{P-P}, PGA gain = 1V/V		19		
Input Capacitance (Note 8)		Single-ended, any AIN0–AIN7, PGA gain = 16V/V		16		pF
		Single-ended, any AIN0–AIN7, PGA gain = 1V/V		13		
Input Common-Mode Rejection Ratio	CMRR	AIN0–AIN7, V_{CM} = differential input range		75		dB
Power-Supply Rejection Ratio	PSRR	AV_{DD} = 3.0V to 3.6V		90		dB
EXTERNAL REFERENCE INPUTS						
REFADC Input Voltage Range			1.0	3.3	V_{AVDD}	V
REFADC Leakage Current		ADC disabled		1		µA
Input Capacitance		(Note 9)		20		pF
+3.3V (AVDD) LINEAR REGULATOR						
AVDD Output Voltage		LRAPD = 0	3.15	3.3	3.45	V
No-Load Quiescent Current		LRAPD = 0, all internal analog peripherals disabled		10		µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-FREQUENCY CRYSTAL OSCILLATOR						
Clock Frequency		Using external crystal		8 or 16	16	MHz
		External input (Note 10)	0.166		16.67	
Stability		Excluding crystal drift		25		ppm
Startup Time		f_{SYSCLK} cycles		65,535		Cycles
XIN Input Low Voltage		Driven with external clock source			0.3 x V_{DVDD}	V
XIN Input High Voltage		Driven with external clock source	0.7 x V_{DVDD}			V
INTERNAL FIXED-FREQUENCY OSCILLATOR						
Frequency	f_{IFFCLK}	T_A = T_{MIN} to T_{MAX}	13.8	15	16.35	MHz
Tolerance		T_A = +25°C		±0.4		%
Temperature Drift		T_A = T_{MIN} to T_{MAX}		5		%
Power-Supply Rejection		T_A = +25°C, DV_{DD} = 2.25V to 2.75V		±1.5		%
RESET ($\overline{RESET}$)						
$\overline{RESET}$ Internal Pullup Resistance		Pulled up to DVDDIO		55		kΩ
$\overline{RESET}$ Output Low Voltage		$\overline{RESET}$ asserted, no external load			0.4	V
$\overline{RESET}$ Output High Voltage		$\overline{RESET}$ deasserted, no external load	0.9 x V_{DVDDIO}			V
$\overline{RESET}$ Input Low Voltage		Driven with external clock source			0.3 x V_{DVDD}	V
$\overline{RESET}$ Input High Voltage		Driven with external clock source	0.7 x V_{DVDDIO}			V
DIGITAL INPUTS (P0._, CANRXD, MISO, MOSI, $\overline{SS}$, SCLK, TCK, TDI, TMS)						
Input Low Voltage					0.8	V
Input High Voltage			2.1			V
Input Hysteresis				500		mV
Input Leakage Current		V_{IN} = GNDIO or V_{DVDDIO}, pullup disabled	-10	±0.01	+10	µA
Input Pullup Resistance				55		kΩ
Input Pulldown Resistance				55		kΩ
Input Capacitance				15		pF
DIGITAL OUTPUTS (P0._, CANTXD, MOSI, SCLK, $\overline{SS}$, TDO)						
Output Low Voltage		I_{SINK} = 0.5mA			0.4	V
Output High Voltage		I_{SOURCE} = 0.5mA	V_{DVDDIO} - 0.5			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Capacitance		I/O pins three-state		15		pF
Maximum Output Impedance		PD0._ = 0		880		Ω
		PD0._ = 1		450		
SYSTEM CLOCK						
System Clock Frequency	f_{SYSCLK}	From any clock source	0		16.67	MHz
SPI INTERFACE TIMING						
SPI Master Operating Frequency	f_{MCLK}	0.5 x f_{SYSCLK}			8	MHz
SPI Slave Mode Operating Frequency	f_{SCLK}				$f_{SYSCLK}/8$	MHz
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		t_{SYSCLK} - 25			ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}		t_{SYSCLK}			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		t_{SYSCLK} - 25			ns
MOSI Output Setup Time to SCLK Sample Edge	t_{MOS}		t_{SYSCLK} - 25			ns
MISO Input Setup Time to SCLK Sample Edge	t_{MIS}		30			ns
MISO Input Hold Time After SCLK Sample Edge	t_{MIH}		0			ns
SCLK Inactive to MOSI Inactive	t_{MLH}		t_{SYSCLK} - 25			ns
MOSI Input Setup Time to SCLK Sample Edge	t_{SIS}		30			ns
MOSI Input Hold Time After SCLK Sample Edge	t_{SIH}		t_{SYSCLK} + 25			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				3 t_{SYSCLK} + 25	ns
MISO Output Disabled After $\overline{SS}$ Edge Rise	t_{SLH}				2 t_{SYSCLK} + 50	ns
$\overline{SS}$ Falling Edge to MISO Active	t_{SOE}		2 t_{SYSCLK} + 2.5			ns

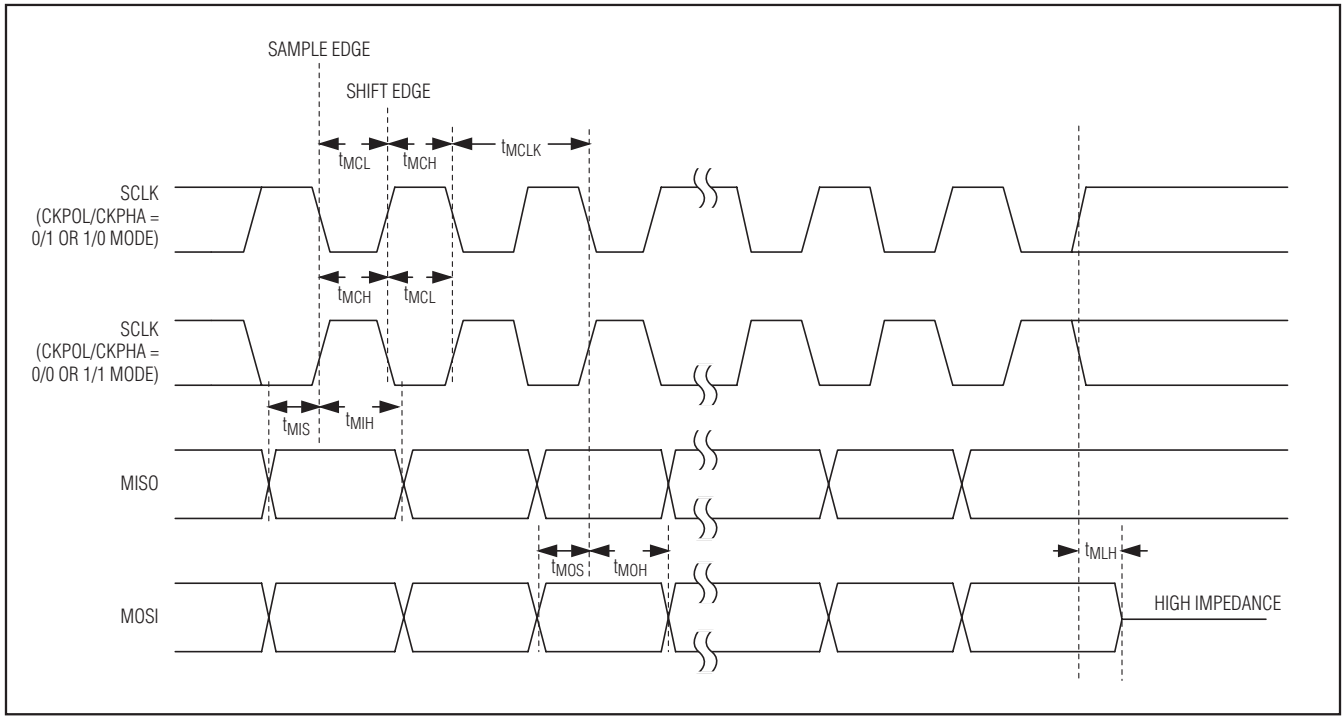


Figure 1. SPI Timing Diagram in Master Mode

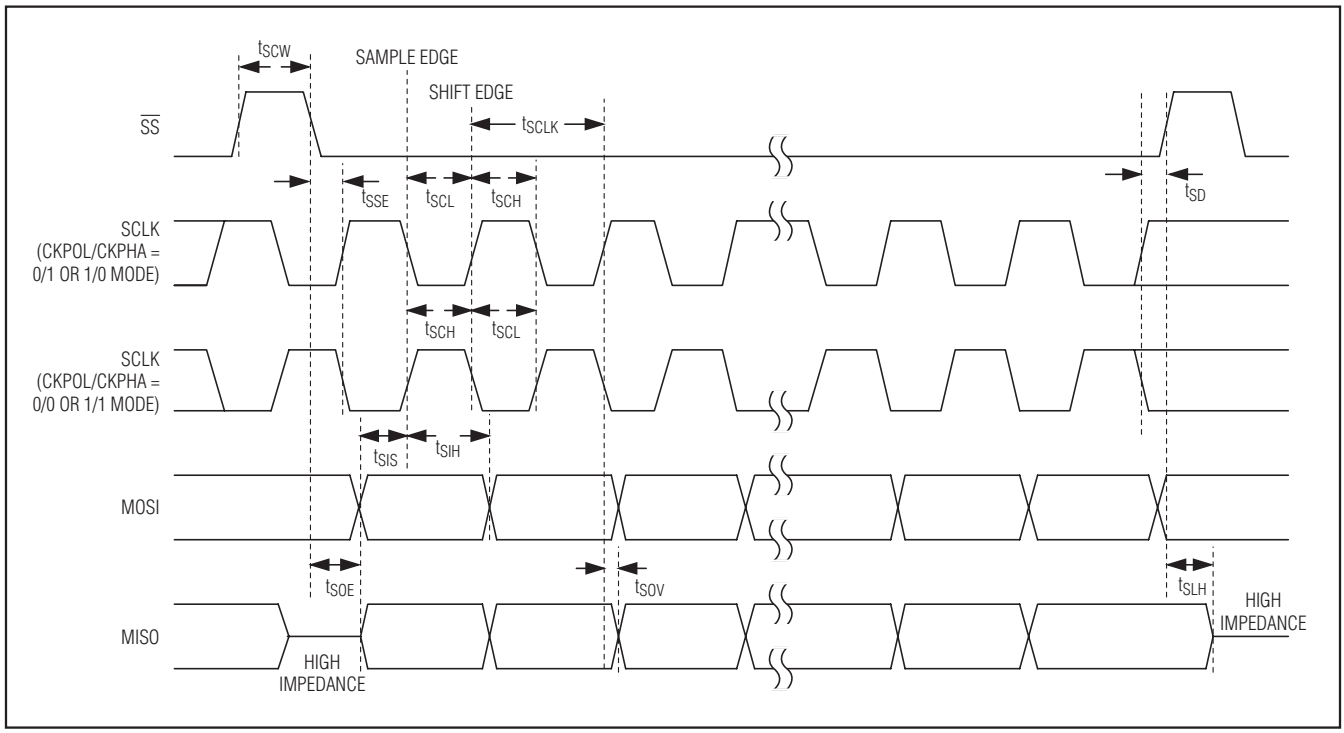


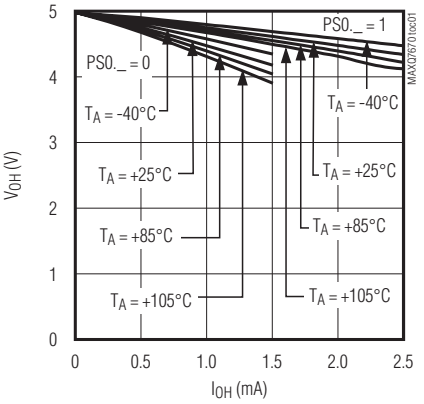
Figure 2. SPI Timing Diagram in Slave Mode

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

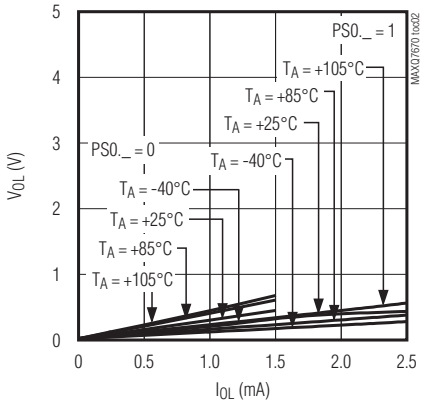
Typical Operating Characteristics

(V_{DVDDIO} = 5.0V, V_{AVDD} = 3.3V, V_{DVDD} = 2.5V, f_{SYSCLK} = 16MHz, ADC resolution = 10 bits, V_{REFDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

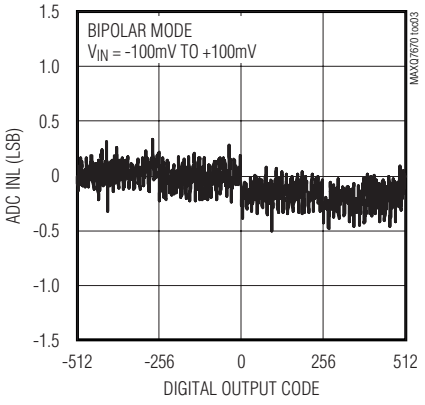
GPO._ OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



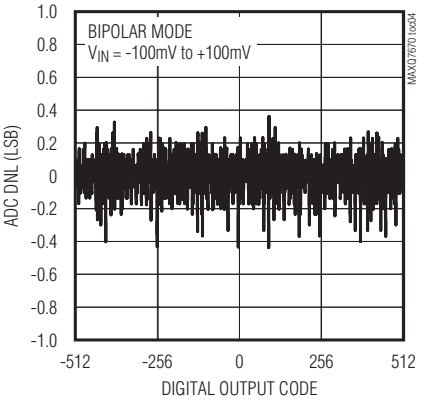
GPO._ OUTPUT LOW VOLTAGE vs. SINK CURRENT



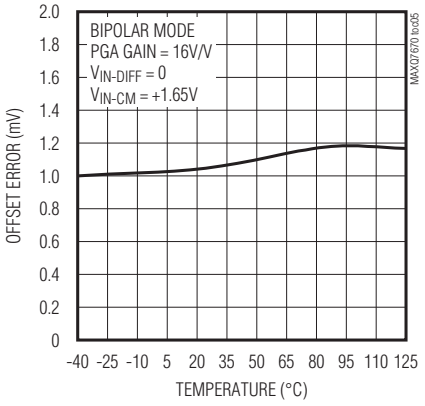
ADC INL vs. CODE (REF ADC = +3.3V, 150.9ksps, PGA GAIN = 16V/V)



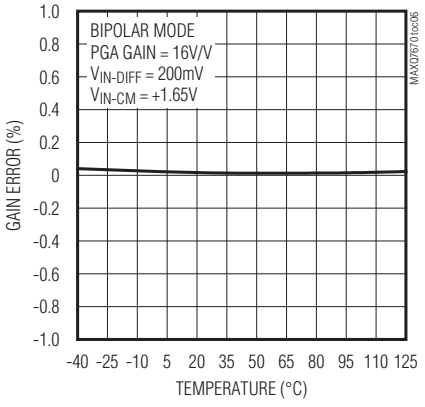
ADC DNL vs. CODE (REFADC = +3.3V, 150.9ksps, PGA GAIN = 16V/V)



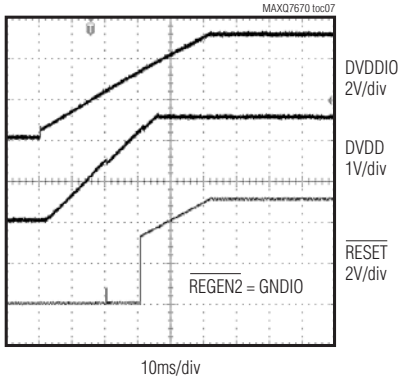
ADC OFFSET ERROR vs. TEMPERATURE



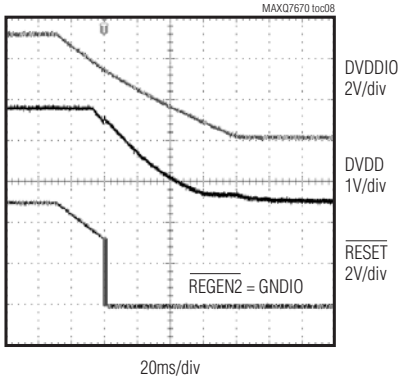
ADC GAIN ERROR vs. TEMPERATURE



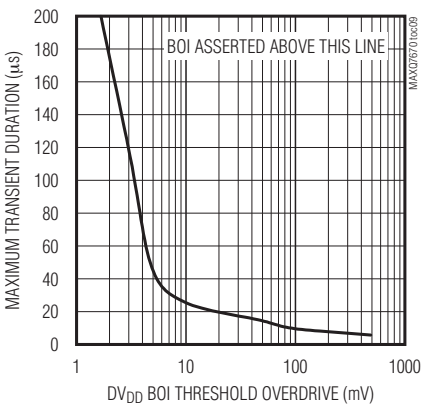
DVDD, $\overline{RESET}$ POWER-UP CHARACTERISTICS



DVDD, $\overline{RESET}$ POWER-DOWN CHARACTERISTICS



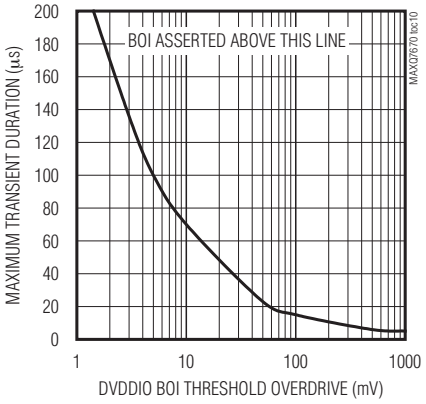
MAXIMUM DVDD TRANSIENT DURATION vs. BOI THRESHOLD OVERDRIVE



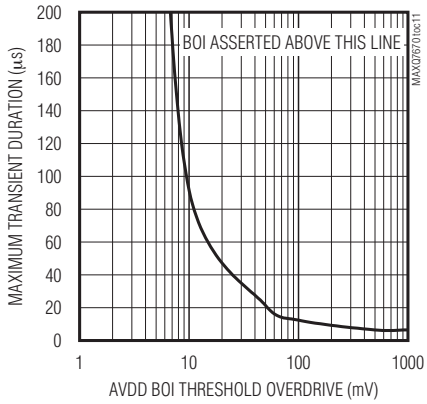
Typical Operating Characteristics (continued)

(V_{DVDDIO} = 5.0V, V_{AVDD} = 3.3V, V_{DVDD} = 2.5V, f_{SYSCLK} = 16MHz, ADC resolution = 10 bits, V_{REFDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

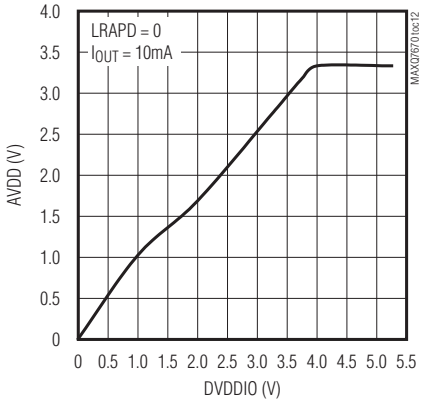
MAXIMUM DVDDIO TRANSIENT DURATION vs. BOI THRESHOLD OVERDRIVE



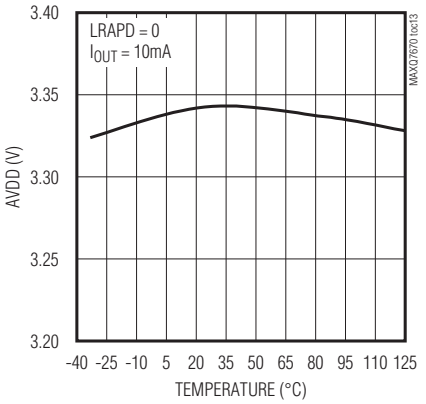
MAXIMUM AVDD TRANSIENT DURATION vs. BOI THRESHOLD OVERDRIVE



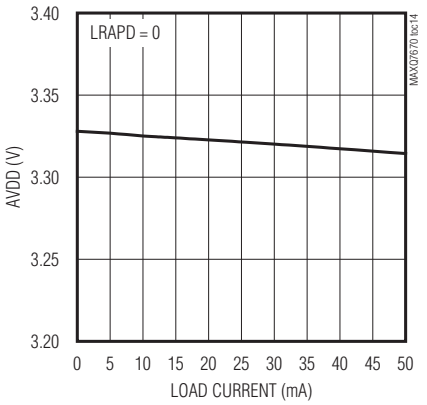
AVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. DVDDIO SUPPLY VOLTAGE



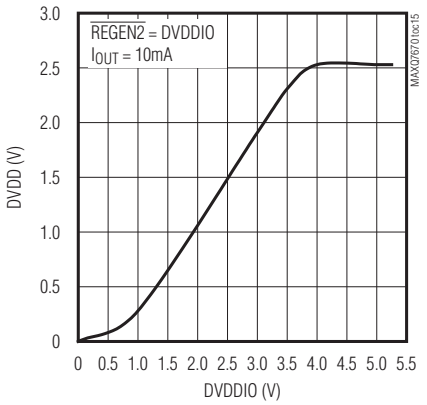
AVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. TEMPERATURE



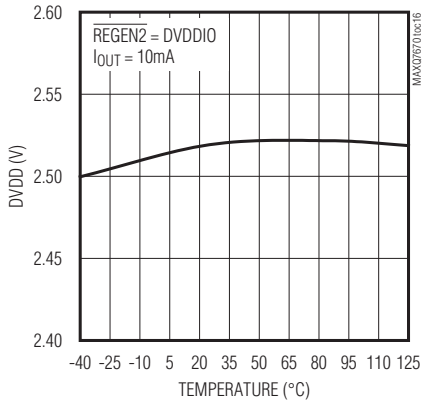
AVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



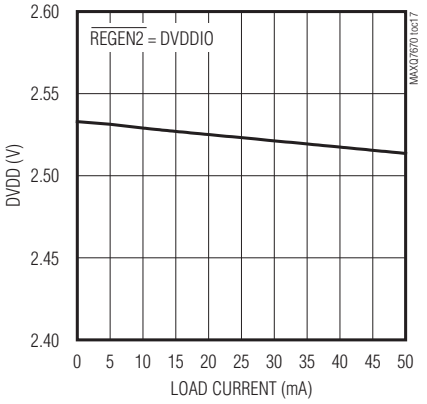
DVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. DVDDIO SUPPLY VOLTAGE



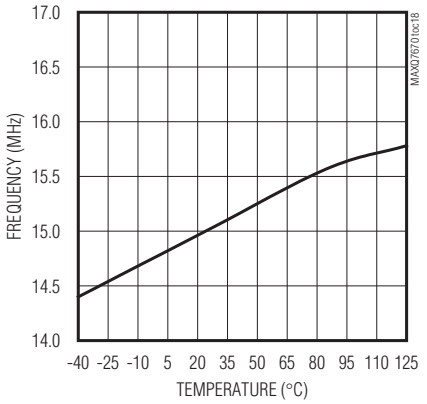
DVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. TEMPERATURE



DVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



RC OSCILLATOR OUTPUT FREQUENCY vs. TEMPERATURE



Pin Description (continued)

PIN	NAME	FUNCTION
23	SCLK	SPI Serial Clock. SCLK is the SPI interface serial clock I/O. In SPI master mode, SCLK is an output. While in SPI slave mode, SCLK is an input.
24	MOSI	SPI Serial Data I/O. MOSI is the SPI interface serial data output in master mode or serial data input in slave mode.
25	MISO	SPI Serial Data I/O. MISO is the SPI interface serial data input in master mode or serial data output in slave mode.
26	$\overline{\text{REGEN2}}$	Active-Low +2.5V Linear Regulator Enable Input. Connect $\overline{\text{REGEN2}}$ to GNDIO to enable the +2.5V linear regulator. Connect to DVDDIO to disable the +2.5V linear regulator.
27	TDO	JTAG Serial Test Data Output. TDO is the JTAG serial test, data output.
28	TMS	JTAG Test Mode Select. TMS is the JTAG test mode, select input.
29	TDI	JTAG Serial Test Data Input. TDI is the JTAG serial test, data input.
30	TCK	JTAG Serial Test Clock Input. TCK is the JTAG serial test, clock input.
31	P0.4/ ADCCNV	Port 0 Bit 4/ADC Start Conversion Control. P0.4 is a general-purpose digital I/O with interrupt/wake-up capability. ADCCNV is a firmware-configurable, rising or falling edge, start/convert signal used to trigger ADC conversions. The alternative function, ADCCNV, is selected using the register bits ACNT[2:0]. When using ADCCNV as a trigger for ADC conversion, set P0.4/ADCCNV as an input using the PD0 register. This action prevents any unintentional interference in the SARADC operation.
32	P0.5	Port 0 Bit 5. P0.5 is a general-purpose digital I/O with interrupt/wake-up capability.
33	$\overline{\text{RESET}}$	Reset Input/Output. Active-low input/output with internal 55kΩ pullup to DVDDIO. Drive low to reset the MAXQ7670. The MAXQ20 µC core holds $\overline{\text{RESET}}$ low during POR and during DVDD brownout conditions.
34	DGND	Digital Ground
35	XOUT	High-Frequency Crystal Output. Connect an external crystal to XIN and XOUT for normal operation, or leave unconnected if XIN is driven with an external clock source. Leave unconnected if an external clock source is not used.
36	XIN	High-Frequency Crystal Input. Connect an external crystal or resonator to XIN and XOUT for normal operation, or drive XIN with an external clock source. Leave unconnected if an external clock source is not used.
37	DVDD	Digital Supply Voltage. DVDD supplies internal digital core and flash memory. DVDD is directly connected to the output of the internal +2.5V linear regulator. Disable the internal regulator (through $\overline{\text{REGEN2}}$) to connect an external supply. Bypass DVDD to DGND with a 0.1µF capacitor as close as possible to the device.
40	AVDD	Analog Supply Voltage. AVDD supplies PGA and ADC. AVDD is directly connected to the output of the internal +3.3V linear regulator. Disable the internal regulator (via software) to connect an external supply. Bypass AVDD to AGND with a 0.1µF capacitor as close as possible to the device.
—	EP	Exposed Pad. Connect EP to the ground plane.

Detailed Description

The MAXQ7670 incorporates a 16-bit RISC arithmetic logic unit (ALU) with a Harvard memory architecture that addresses 64KB (32K x 16) of flash and 2048 bytes (1024 x 16) of RAM memory. This core combined with digital and analog peripherals provide versatile data-acquisition functions. The peripherals include up to seven digital I/Os, a 4-wire SPI interface, a CAN 2.0B bus, a JTAG interface, a timer, an integrated RC oscillator, two linear regulators, a watchdog timer, three power-supply supervisors, a 10-bit 250ksps SAR ADC with programmable-gain amplifier (PGA) and eight single-ended or four differential multiplexed inputs. The power-efficient MAXQ20 µC core consumes less than 1mA/MIPS. Refer to the *MAXQ7670 User's Guide* for more detailed information on configuring and programming the MAXQ7670.

Analog Input Peripheral

The integrated 10-bit ADC employs an ultra-low-power SAR-based conversion method and operates up to 250ksps with PGA = 1V/V (150.9ksps with PGA = 16V/V). The integrated 8-channel multiplexer (mux) and PGA allow the ADC to measure eight single-ended (relative to AGND) or four fully differential analog inputs with software-selectable input ranges through the PGA. See Figures 3 and 4.

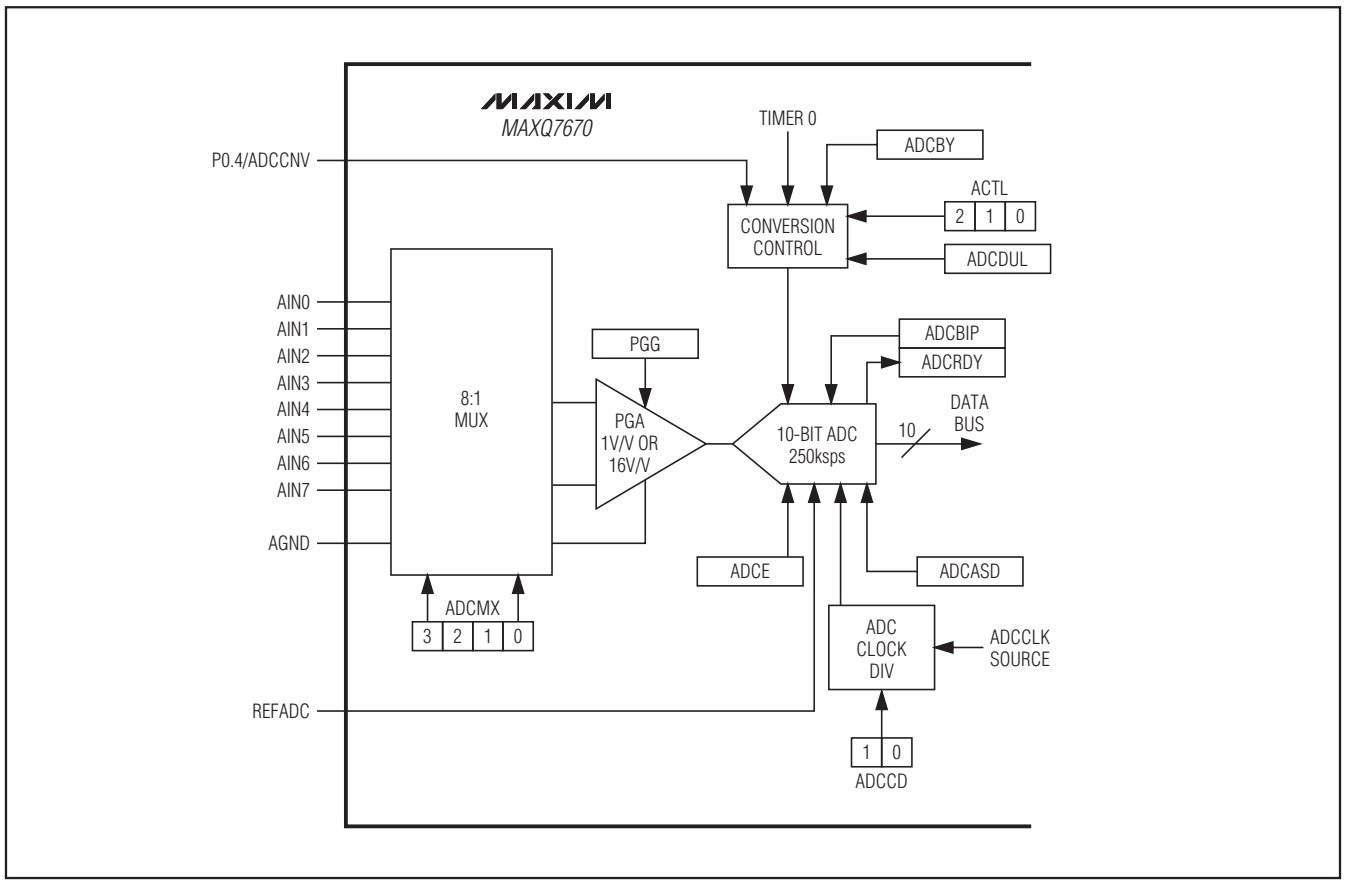


Figure 3. Simplified Analog Input Diagram (Eight Single-Ended Inputs)

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

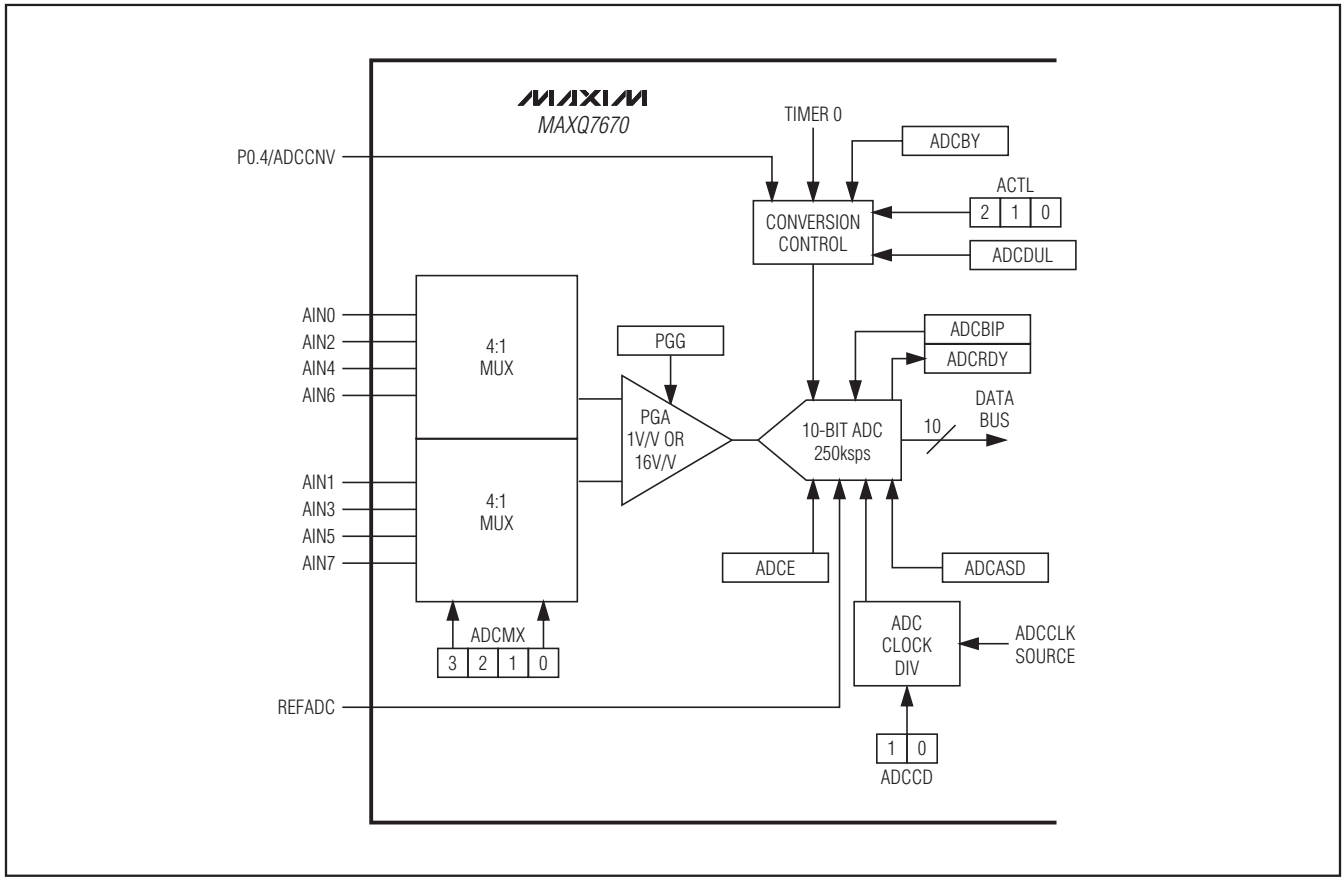


Figure 4. Simplified Analog Input Diagram (Four Fully Differential Inputs)

The MAXQ7670 ADC uses a fully differential SAR conversion technique and an integrated T/H (track and hold) block to convert voltage signals into a 10-bit digital result. Both single-ended and differential configurations are implemented using an analog input channel multiplexer that supports 8 single-ended or 4 differential channels.

In single-ended mode, the mux selects from either of the ground-referenced analog inputs AIN0–AIN7. In differential input configuration, analog inputs are selected from the following pairs: AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, and AIN6/AIN7. Table 1 shows the single-ended and differential input configurations possible for the ADC mux.

Analog Input Track and Hold

A SAR conversion in the MAXQ7670 has different T/H cycles depending on whether a gain of 1 (bypass) or a gain of 16 (PGA enabled) is selected.

Gain = 1V/V

In gain = 1V/V, the conversion has a two-stage T/H cycle. In track mode, a positive input capacitor connects to the signal channel. A negative input capacitor connects to the reference channel. After the T/H enters hold mode, the difference between the signal and the reference channel is converted to a 10-bit value. This two-stage cycle takes 16 SARCLKs to complete.

Gain = 16V/V

In gain = 16V/V, the conversion has a three-stage T/H cycle: amplification, ADC track, and ADC hold. First, the PGA tracks the selected input and reference signals. The PGA amplifies the difference between the two signals and holds the result for the next stage, ADC track. The ADC tracks and converts the PGA result into a 10-bit value. The SAR operation itself does not change irrespective of the chosen gain. This three-stage cycle takes 26.5 SARCLKs to complete. Figure 5 shows the conversion timing differences between gain = 1V/V and gain = 16V/V.

Table 1. ADC Mux Input Configurations

SAR CHANNEL SELECT (REGISTER ACNT[14:11])	SIGNAL CHANNEL INTO ADC	REFERENCE CHANNEL INTO ADC	MEASUREMENT TYPE
0000	AIN0	AGND	Single-ended measurement on AIN0
0001	AIN1	AGND	Single-ended measurement on AIN1
0010	AIN2	AGND	Single-ended measurement on AIN2
0011	AIN3	AGND	Single-ended measurement on AIN3
0100	AIN4	AGND	Single-ended measurement on AIN4
0101	AIN5	AGND	Single-ended measurement on AIN5
0110	AIN6	AGND	Single-ended measurement on AIN6
0111	AIN7	AGND	Single-ended measurement on AIN7
1000	—	—	Reserved
1001	—	—	Reserved
1010	AIN0	AIN1	AIN0/AIN1
1011	AIN2	AIN3	AIN2/AIN3
1100	AIN4	AIN5	AIN4/AIN5
1101	AIN6	AIN7	AIN6/AIN7
1110	—	—	Reserved
1111	—	—	VCIM differential zero offset trim

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

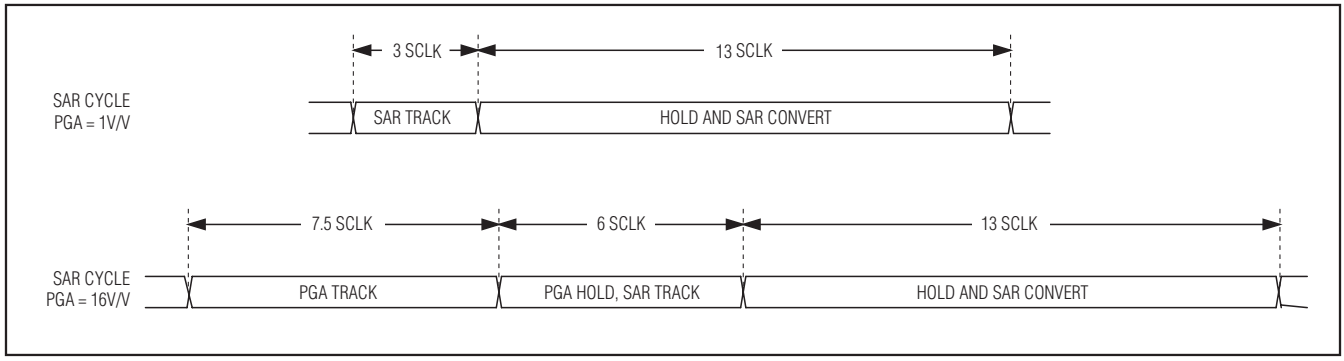


Figure 5. Conversion Timing Differences Between Gain = 1V/V and Gain = 16V/V

Input Impedance

The input-capacitance charging rate determines the time required for the T/H to acquire an input signal. The required acquisition time lengthens with the increase of the input signals source resistance. Any source below 5kΩ does not significantly affect the ADC's performance. A high-impedance source can be accommodated by placing a 1µF capacitor between the input channel and AGND. The combination of analog-input source impedance and the capacitance at the analog input creates an RC filter that limits the analog-input bandwidth.

Controlling ADC Conversions

Use the following methods to control the ADC conversion timing:

1) Software register bit control

2) Continuous conversion

3) Internal timer (T0)

4) External input through ADCCNV

Refer to the *MAXQ7670 User's Guide* for more detailed information on the ADC and mux.

POR and Brownout

The MAXQ7670 operates from a single, external +5V supply connected to the DVDDIO. DVDDIO is the supply rail for the digital I/O and the supply input for both integrated linear regulators. The +3.3V linear regulator powers AVDD, while the +2.5V linear regulator powers DVDD. Alternatively, connect $\overline{\text{REGEN2}}$ to DVDDIO and apply external power supplies to AVDD and DVDD.

Power supplies DVDDIO, DVDD, and AVDD each include a brownout monitor that alerts the µC through an interrupt when the corresponding supply voltages drop below a defined threshold. This condition is generally referred to as brownout interrupt (BOI). Enable BOI by setting the VABE, VDBE, and VIBE bits in the APE register. By continually checking for low supply voltages, appropriate action can be taken for brownout conditions.

Startup Using Internal Regulators

Once the +5V DVDDIO supply reaches approximately 1.25V, the +2.5V linear regulator turns on and DVDD begins ramping. Between the DVDD levels of 1V and the reset threshold, the DVDD monitor holds $\overline{\text{RESET}}$ low. DVDD releases $\overline{\text{RESET}}$ after reaching the reset threshold. The MAXQ7670 jumps to the reset vector location (8000h in the utility ROM). During this time, DVDD finishes ramping to its nominal voltage of +2.5V.

During this POR time, the software-enabled +3.3V linear regulator remains off. Turn on the +3.3V linear regulator after the MAXQ7670 has completed its bootup routines and is running application code. To turn on the +3.3V regulator, set the LRAPD bit in the APE register to 0. The AVDD supply begins ramping to its nominal voltage of +3.3V.

Brownout Detectors

The MAXQ7670 features brownout monitors for the +5V DVDDIO, +3.3V AVDD, and +2.5V DVDD power supplies. When enabled, these monitors generate interrupts when DVDDIO, AVDD, or DVDD fall below their respective brownout thresholds. Monitoring the supply rails alerts the µC to brownout conditions so appropriate action can be taken. Under normal conditions the DVDDIO brownout monitor signals a falling +5V supply before the DVDD or AVDD brownout monitors indicate that the +2.5V or +3.3V are falling. The exceptions to this condition are:

- If either DVDD or AVDD are externally powered and the source of power is removed
- If there is some type of device failure that pulls the regulator outputs low without affecting the +5V DVDDIO supply

The DVDD reset supervisor resets the MAXQ7670 when the +2.5V DVDD falls below the reset threshold. The processor remains in reset until DVDD returns above the reset threshold. The µC does not execute commands in reset mode. See Figure 6 for the µC response to DVDD brownout and reset.

Refer to the *MAXQ7670 User's Guide* for detailed programming information, and a more thorough description of POR and brownout behavior.

Internal 3.3V Linear Regulator

The integrated 3.3V 50mA linear regulator or an external 3.3V supply powers AVDD. The integrated 3.3V regulator is inactive upon power-up. Enable the integrated regulator with software programming after power-up. When using an external supply, connect a regulated 3.3V supply to AVDD after applying DVDDIO.

Internal 2.5V Linear Regulator

The integrated 2.5V 50mA linear regulator or an external 2.5V supply applied at DVDD powers DVDD. Connect $\overline{\text{REGEN2}}$ to GNDIO to enable the integrated regulator. Connect $\overline{\text{REGEN2}}$ to DVDDIO to use an external supply. When using an external supply, connect a regulated 2.5V supply to DVDD after applying DVDDIO.

DVDDIO Current Requirements

Both internal linear regulators are capable of supplying up to 50mA each. When using the regulators to power AVDD and DVDD and to provide power to external devices, make sure DVDDIO's power input can source a current greater than the sum of the MAXQ7670 supply current and the load currents of the two regulators.

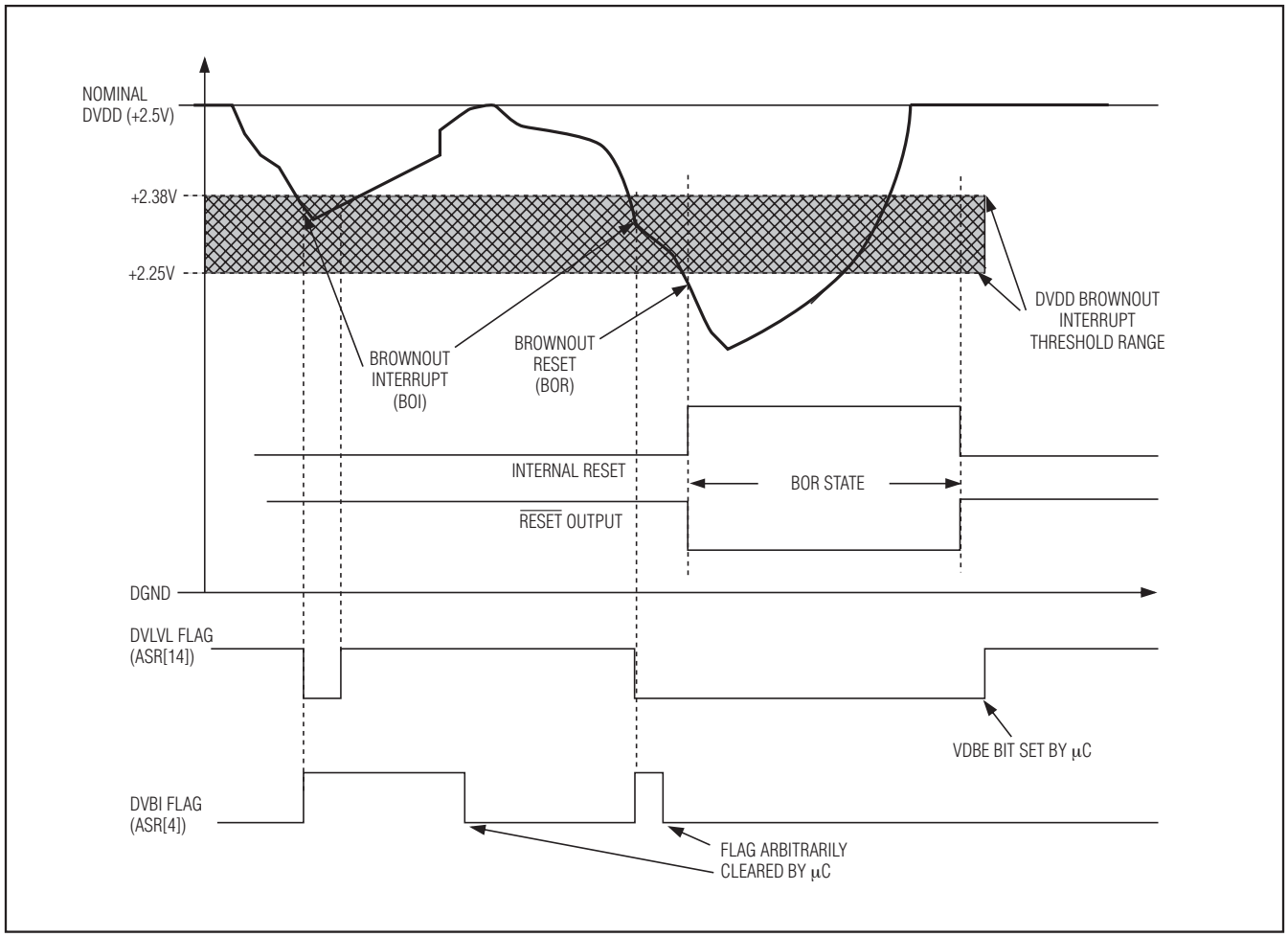


Figure 6. DVDD Brownout and Reset Behavior

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

System Clock Generator

The MAXQ7670 oscillator module provides the master clock generator that supplies the system clock for the µC core and all of the peripheral modules. The high-frequency oscillator operates with an 8MHz or 16MHz crystal. Alternatively, use the integrated RC oscillator in applications that do not require precise timing. The MAXQ7670 executes most instructions in a single SYSCLK period. The oscillator module contains all of the primary clock generation circuitry. Figure 7 shows a block diagram of the system clock module.

The MAXQ7670 contains the following features for generating its master clock signal timing source:

- Internal, fast-starting, 15MHz RC oscillator eliminates external crystal
- Internal high-frequency oscillator that can drive an external 8MHz or 16MHz crystal
- External high-frequency 0.166MHz to 16MHz clock input
- Power-up timer
- Power-saving management modes
- Fail-safe modes

Watchdog Timer

The primary function of the watchdog timer is to supervise software execution, watching for stalled or stuck software. The watchdog timer performs a controlled system restart when the µC fails to write to the watchdog timer register before a selectable timeout interval expires. A watchdog timer typically has four objectives:

1) To detect if a system is operating normally
2) To detect an infinite loop in any of the tasks
3) To detect an arbitration deadlock involving two or more tasks
4) To detect if some lower priority tasks are not getting to run because of higher priority tasks

As illustrated in Figure 8, the internal RC oscillator (CLK_RC) drives the watchdog timer through a series of dividers. The programmable divider output determines the timeout interval. When enabled, the interrupt flag WDIF sets. A system reset occurs after a time delay (based on the divider ratio) unless an interrupt service routine clears the watchdog interrupt.

The watchdog timer functions as the source of both the watchdog interrupt and the watchdog reset. The interrupt timeout has a default divide ratio of 2^{12} of the CLK_RC, with the watchdog reset set to timeout 2^9 clock cycles later. With the nominal RC oscillator value of 15MHz, an interrupt timeout occurs every 0.273ms, followed by a watchdog reset 34µs later. The watchdog timer resets to the default divide ratio following any reset event. Use the WD0 and WD1 bits in the WDCN register to increase the watchdog interrupt period. Changing the WD[1:0] bits before a watchdog interrupt timeout occurs (i.e. before the watchdog reset counter begins) resets the watchdog timer count. The watchdog reset timeout occurs 512 RC oscillator cycles after the watchdog interrupt timeout. For more information on the MAXQ7670 watchdog timer, refer to the *MAXQ7670 User's Guide.*

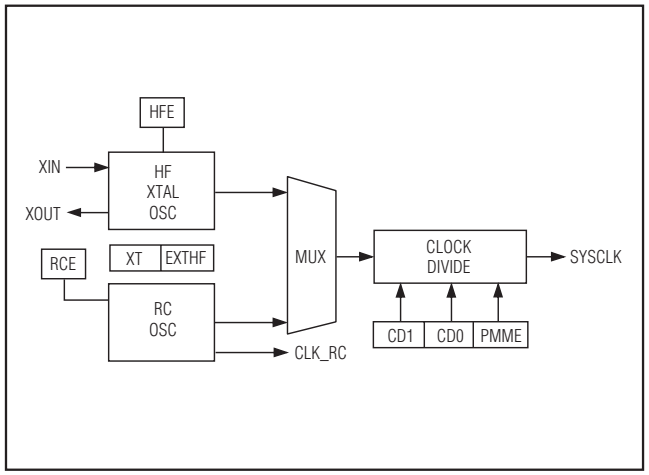


Figure 7. High-Frequency and RC Oscillator Functional Diagram

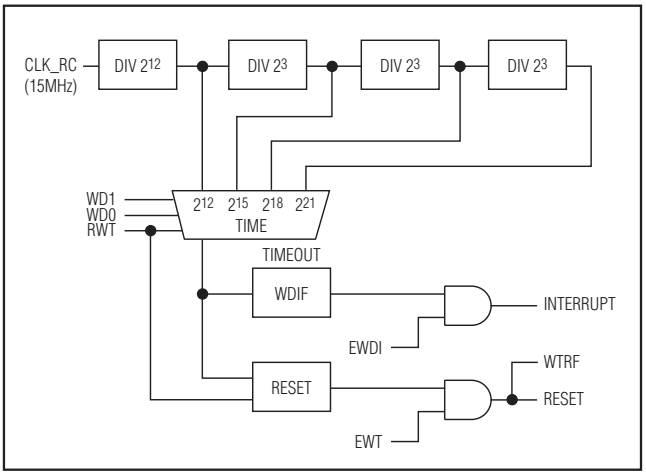


Figure 8. Watchdog Functional Diagram

frequency is limited to SYSCLK/2 in master mode and SYSCLK/8 in slave mode. Figure 10 shows the functional diagram of the SPI port. Figures 1 and 2 illustrate the timing parameters listed in the *Electrical Characteristics* table.

General-Purpose Digital I/Os

The MAXQ7670 provides seven general-purpose digital I/Os (GPIOs). Some of the GPIOs include an additional special function (SF), such as a timer input/output. For example, the state of P0.6/T0 is programmable to depend on timer channel 0 logic. When used as a port, each I/O is configurable for high-impedance, weak pullup to DVDDIO or pulldown to GNDIO. At power-up, each GPIO is configured as an input with a pullup to DVDDIO. In addition, each GPIO can be programmed to cause an interrupt (on falling or rising edges). In stop mode, use any interrupt to wake-up the device.

The port direction (PD) register determines the input/output direction of each I/O. The port output (PO) register contains the current state of the logic output buffers. When an I/O is configured as an output, writing to the PO register controls the output logic state. Reading the PO register shows the current state of the output buffers, independent of the data direction. The port input (PI) register is a read-only register that always reflects the logic state of the I/Os.

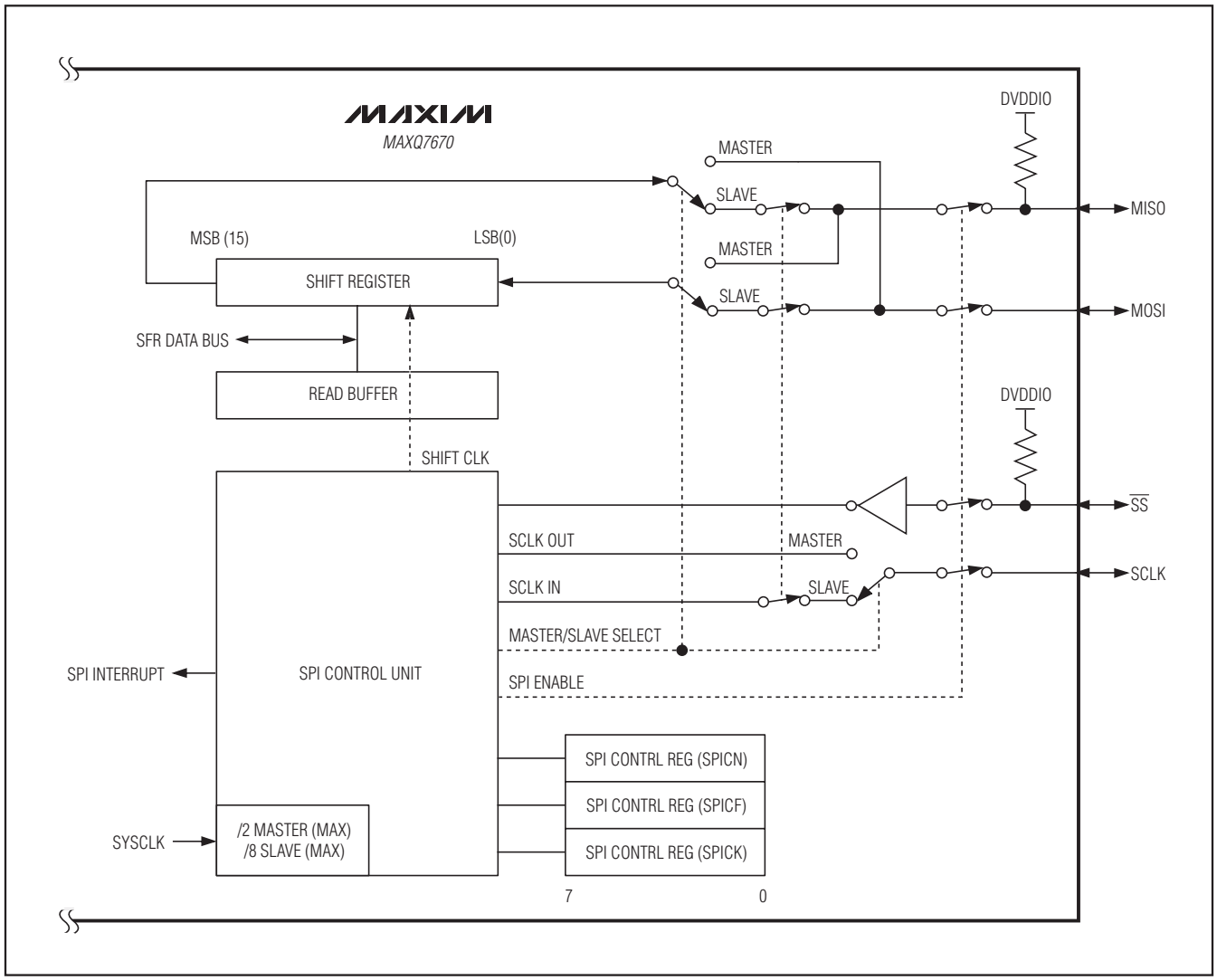


Figure 10. SPI Functional Diagram

Power Management

Advanced power-management features minimize power consumption by dynamically matching the processing speed of the device to the required performance level. During periods of reduced activity, lower the system clock speed to reduce power consumption. Use the source-clock-divide feature to reduce the system clock speed to 1/2, 1/4, and 1/8 of the source clock's speed. A lower power state is thus achievable without additional hardware. For extremely power-sensitive applications, two additional low-power modes are available:

- PMM: divide-by-256 power-management mode (PMME = 1)
- Stop mode (STOP = 1)

Enabling PMM reduces the system clock speed to 1/256 of the source clock speed, and significantly reduces power consumption. The optional switchback feature allows enabled interrupt sources including external, CAN, and SPI interrupts to bring the µC out of the power-management mode and to run at a faster system clock speed.

Power consumption is minimal in stop mode. In this mode, the external oscillator, internal RC oscillator, system clock, and all processing activity stop. Triggering an enabled external interrupt or applying an external reset signal to $\overline{\text{RESET}}$ brings the µC out of stop mode. Upon exiting stop mode, the µC can either wait for the external crystal to warm up, or execute immediately by using the internal RC oscillator as the crystal warms up.

Interrupts

Multiple interrupt sources are available for quick response to internal and external events. Examples of events that can trigger an interrupt are:

- Watchdog interrupt
- GPIO0–GPIO7 interrupts
- SPI mode fault, write collision, receive overrun, and transfer complete interrupts
- Timer 0 low compare, low overflow, capture/compare, and overflow interrupts
- CAN0 receive and transmit interrupts and a change in CAN0 status register interrupt
- ADC data ready interrupt
- Voltage brownout interrupts
- Crystal oscillator failure interrupt

Each interrupt has flag and enable bits. The flag indicates whether an interrupt event has occurred. Enable the µC to generate an interrupt by setting the enable bit. Interrupts are organized into modules. Enable the interrupt individually, by module, and globally.

The µC jumps to an ISR after an enabled interrupt event occurs. Use the interrupt identification register (IIR) to determine whether the interrupt is a system or peripheral interrupt. In the ISR, clear the interrupt flag to eliminate repeated interrupts from the same event. After clearing the interrupt, allow a delay before issuing the return from interrupt (RETI) instruction. Asynchronous interrupt flags require a one-instruction delay and synchronous interrupt flags require a two-instruction delay.

The MAXQ architecture uses a single interrupt vector (IV) and single ISR design. The IV register holds the address of the ISR. In the application code, assign a unique address to each ISR. Otherwise, the IV automatically jumps to 0000h, the beginning of application code, after an enabled interrupt occurs.

Reset Sources

Reset sources are provided for µC control. Although code execution stops in the reset state, the internal RC oscillator continues to oscillate. Internal resets, such as the power-on and watchdog resets, pull $\overline{\text{RESET}}$ low.

Power-On Reset (POR)

An internal POR circuit enhances system reliability. The POR circuit forces the device to perform a POR whenever a rising voltage on DVDD climbs above the POR threshold. At this point the following events occur:

- All registers and circuits enter the default state
- The POR flag (WDCN.7) sets to indicate if the source of the reset was a loss of power
- The internal 15MHz RC oscillator becomes the clock source
- Code execution begins at location 8000h

Refer to the *MAXQ7670 User's Guide* for more information.

Watchdog Timer Reset

The watchdog timer functions are described in the *MAXQ7670 User's Guide*. Execution resumes at location 8000h following a watchdog timer reset.

External System Reset

Pulling $\overline{\text{RESET}}$ low externally causes the device to enter the reset state. The external reset functions as described in the *MAXQ7670 User's Guide*. Execution resumes at location 8000h after $\overline{\text{RESET}}$ is released.

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

Crystal Selection

The MAXQ7670 uses an 8MHz or 16MHz Jauch JXG53P2 (or similar specification):

Frequency: 8MHz or 16MHz ±0.25%.

C_{LOAD}: 12pF.

C_O: < 7pF max.

Series resonance resistance: max 50Ω/300Ω for 16MHz/8MHz, respectively.

Note: Series resonance resistance is the resistance observed when the resonator is in the series resonant condition. This is a parameter often stated by quartz crystal vendors and is called R1. When a resonator is used in the parallel resonant mode with an external load capacitance, as is the case with the MAXQ7670 oscillator circuit, the effective resistance is sometimes stated. This effective resistance at the loaded frequency of oscillation is:

$$R1 \times (1 + (C_O/C_{LOAD}))2$$

For typical C_O and C_{LOAD} values, the effective resistance can be greater than R1 by a factor of two.

Development and Technical Support

Highly versatile, affordably priced development tools for this µC are available from Maxim and third-party suppliers. Tools for the MAXQ7670 include:

- Compilers
- Evaluation kits
- JTAG-to-serial converters for programming and debugging

A list of development tool vendors can be found at **www.maxim-ic.com/microcontrollers**. For technical support, go to **www.maxim-ic.com/support**.

Table 2. System Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)						
	AP (8h)	**A (9h)**	**PFX (Bh)**	**IP (Ch)**	**SP (Dh)**	**DPC (Eh)**	**DP (Fh)**
0h	AP	**A[0]**	**PFX[0]**	**IP**	—	—	—
1h	APC	**A[1]**	**PFX[1]**	—	**SP**	—	—
2h	—	**A[2]**	**PFX[2]**	—	**IV**	—	—
3h	—	**A[3]**	**PFX[3]**	—	—	OFFS	**DP0**
4h	PSF	**A[4]**	**PFX[4]**	—	—	**DPC**	—
5h	IC	**A[5]**	**PFX[5]**	—	—	**GR**	—
6h	IMR	**A[6]**	**PFX[6]**	—	**LC0**	GRL	—
7h	—	**A[7]**	**PFX[7]**	—	**LC1**	**BP**	**DP1**
8h	SC	**A[8]**		—	—	***GRS***	—
9h	—	**A[9]**	—	—	—	GRH	—
Ah	—	**A[10]**	—	—	—	***GRXL***	—
Bh	*IIR*	**A[11]**	—	—	—	***FP***	—
Ch	—	**A[12]**	—	—	—	—	—
Dh	—	**A[13]**	—	—	—	—	—
Eh	CKCN	**A[14]**	—	—	—	—	—
Fh	WDCN	**A[15]**	—	—	—	—	—

Table 5. Peripheral Register Bit Functions and Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO0	—	—	—	—	—	—	—	—	PO0.7	PO0.6	PO0.5	PO0.4	—	PO0.2	PO0.1	PO0.0
	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1
EIF0	—	—	—	—	—	—	—	—	IE7	IE6	IE5	IE4	—	IE2	IE1	IE0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PI0	—	—	—	—	—	—	—	—	PI0.7	PI0.6	PI0.5	PI0.4	—	PI0.2	PI0.1	PI0.0
	0	0	0	0	0	0	0	0	ST	ST	ST	ST	0	ST	ST	ST
EIE0	—	—	—	—	—	—	—	—	EX7	EX6	EX5	EX4	—	EX2	EX1	EX0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PD0	—	—	—	—	—	—	—	—	PD0.7	PD0.6	PD0.5	PD0.4	—	PD0.2	PDO.1	PD0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
EIES0	—	—	—	—	—	—	—	—	IT7	IT6	IT5	IT4	—	IT2	IT1	IT0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PS0	—	—	—	—	—	—	—	—	PS7	PS6	PS5	PS4	—	PS2	PS1	PS0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PR0	—	—	—	—	—	—	—	—	PR7	PR6	PR5	PR4	—	PR2	PR1	PR0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPIB	SPIB.15	SPIB.14	SPIB.13	SPIB.12	SPIB.11	SPIB.10	SPIB.9	SPIB.8	SPIB.7	SPIB.6	SPIB.5	SPIB.4	SPIB.3	SPIB.2	SPIB.1	SPIB.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPICN	—	—	—	—	—	—	—	—	STBY	SPIC	ROVR	WCOL	MODF	MODFE	MSTM	SPIEN
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPICF	—	—	—	—	—	—	—	—	ESPII	—	—	—	—	CHR	CKPHA	CKPOL
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPICK	—	—	—	—	—	—	—	—	SPICK7	SPICK6	SPICK5	SPICK4	SPICK3	SPICK2	SPICK1	SPICK0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FCNTL	—	—	—	—	—	—	—	—	FBUSY	—	—	—	—	FC2	FC1	FC0
	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
FPCTL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DPMG
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID0	—	—	—	—	—	—	—	—	ID0.7	ID0.6	ID0.5	ID0.4	ID0.3	ID0.2	ID0.1	ID0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNA0	—	—	—	—	—	—	—	—	ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2H0	—	—	—	—	—	—	—	—	T2H0.7	T2H0.6	T2H0.5	T2H0.4	T2H0.3	T2H0.2	T2H0.1	T2H0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2RH0	—	—	—	—	—	—	—	—	T2RH0.7	T2RH0.6	T2RH0.5	T2RH0.4	T2RH0.3	T2RH0.2	T2RH0.1	T2RH0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CH0	—	—	—	—	—	—	—	—	T2CH0.7	T2CH0.6	T2CH0.5	T2CH0.4	T2CH0.3	T2CH0.2	T2CH0.1	T2CH0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNB0	—	—	—	—	—	—	—	—	ET2L	T2OE1	T2POL1	—	TF2	TF2L	TCC2	TC2L
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2V0	T2V0.15	T2V0.14	T2V0.13	T2V0.12	T2V0.11	T2V0.10	T2V0.9	T2V0.8	T2V0.7	T2V0.6	T2V0.5	T2V0.4	T2V0.3	T2V0.2	T2V0.1	T2V0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R0	T2R0.15	T2R0.14	T2R0.13	T2R0.12	T2R0.11	T2R0.10	T2R0.9	T2R0.8	T2R0.7	T2R0.6	T2R0.5	T2R0.4	T2R0.3	T2R0.2	T2R0.1	T2R0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C0	T2C0.15	T2C0.14	T2C0.13	T2C0.12	T2C0.11	T2C0.10	T2C0.9	T2C0.8	T2C0.7	T2C0.6	T2C0.5	T2C0.4	T2C0.3	T2C0.2	T2C0.1	T2C0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG0	—	—	—	—	—	—	—	—	T2C1	T2DIV2	T2DIV1	T2DIV0	T2MD	CCF1	CCF0	C/T2
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDT0	ICDT0.15	ICDT0.14	ICDT0.13	ICDT0.12	ICDT0.11	ICDT0.10	ICDT0.9	ICDT0.8	ICDT0.7	ICDT0.6	ICDT0.5	ICDT0.4	ICDT0.3	ICDT0.2	ICDT0.1	ICDT0.0
	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB
ICDT1	ICDT1.15	ICDT1.14	ICDT1.13	ICDT1.12	ICDT1.11	ICDT1.10	ICDT1.9	ICDT1.8	ICDT1.7	ICDT1.6	ICDT1.5	ICDT1.4	ICDT1.3	ICDT1.2	ICDT1.1	ICDT1.0
	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB
ICDC	—	—	—	—	—	—	—	—	DME	—	REGE	—	CMD3	CMD2	CMD1	CMD0
	0	0	0	0	0	0	0	0	DW	0	DW	0	DW	DW	DW	DW
ICDF	—	—	—	—	—	—	—	—	—	—	—	—	PSS1	PSS0	SPE	TXC
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDB	—	—	—	—	—	—	—	—	ICDB.7	ICDB.6	ICDB.5	ICDB.4	ICDB.3	ICDB.2	ICDB.1	ICDB.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDA	ICDA.15	ICDA.14	ICDA.13	ICDA.12	ICDA.11	ICDA.10	ICDA.9	ICDA.8	ICDA.7	ICDA.6	ICDA.5	ICDA.4	ICDA.3	ICDA.2	ICDA.1	ICDA.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDD	ICDD.15	ICDD.14	ICDD.13	ICDD.12	ICDD.11	ICDD.10	ICDD.9	ICDD.8	ICDD.7	ICDD.6	ICDD.5	ICDD.4	ICDD.3	ICDD.2	ICDD.1	ICDD.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM	—	—	—	—	CRTMS	CRTM	TESTCAN	—	DCW	FTEST	DOFF	—	SRT	—	SCANMODE	TME
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0C	—	—	—	—	—	—	—	—	ERIE	STIE	PDE	SIESTA	CRST	AUTOB	ERCS	SWINT
	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
C0S	—	—	—	—	—	—	—	—	BSS	EC96/128	WKS	RXS	TXS	ER2	ER1	ER0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0IR	—	—	—	—	—	—	—	—	INTIN7	INTIN6	INTIN5	INTIN4	INTIN3	INTIN2	INTIN1	INTIN0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0TE	—	—	—	—	—	—	—	—	C0TE.7	C0TE.6	C0TE.5	C0TE.4	C0TE.3	C0TE.2	C0TE.1	C0TE.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0RE	—	—	—	—	—	—	—	—	C0RE.7	C0RE.6	C0RE.5	C0RE.4	C0RE.3	C0RE.2	C0RE.1	C0RE.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0R	—	—	—	—	—	—	—	—	CAN0BA	INCDEC	AID	C0BPR7	C0BPR6	—	C0BIE	C0IE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0DP	C0DP.15	C0DP.14	C0DP.13	C0DP.12	C0DP.11	C0DP.10	C0DP.9	C0DP.8	C0DP.7	C0DP.6	C0DP.5	C0DP.4	C0DP.3	C0DP.2	C0DP.1	C0DP.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0DB	C0DB.15	C0DB.14	C0DB.13	C0DB.12	C0DB.11	C0DB.10	C0DB.9	C0DB.8	C0DB.7	C0DB.6	C0DB.5	C0DB.4	C0DB.3	C0DB.2	C0DB.1	C0DB.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0RMS	—	C0RMS.15	C0RMS.14	C0RMS.13	C0RMS.12	C0RMS.11	C0RMS.10	C0RMS.9	C0RMS.8	C0RMS.7	C0RMS.6	C0RMS.5	C0RMS.4	C0RMS.3	C0RMS.2	C0RMS.1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0TMA	—	C0TMA.15	C0TMA.14	C0TMA.13	C0TMA.12	C0TMA.11	C0TMA.10	C0TMA.9	C0TMA.8	C0TMA.7	C0TMA.6	C0TMA.5	C0TMA.4	C0TMA.3	C0TMA.2	C0TMA.1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M1C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M2C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M3C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M4C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M5C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M6C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M7C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M8C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M9C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M10C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M11C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M12C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C0M13C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M14C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M15C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
APE	—	—	LRAPD	VIBE	VDBE	VDPE	VABE	—	—	—	PGG0	—	—	BIASE	—	ADCE
	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
ACNT	—	ADCMX3	ADCMX2	ADCMX1	ADCMX0	—	ADCBIP	—	—	ADCDUL	ADCRSEF	ADCASD	ADCBY	ADCS2	ADCS1	ADCS0
	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADCD	—	—	—	—	—	—	ADCD.9	ADCD.8	ADCD.7	ADCD.6	ADCD.5	ADCD.4	ADCD.3	ADCD.2	ADCD.1	ADCD.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AIE	—	—	—	—	—	—	—	—	—	HFFIE	VIOBIE	DVBIE	AVBIE	—	ADCIE	—
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ASR	VIOLVL	DVLVL	AVLVL	—	XHFRY	—	—	—	—	HFFINT	VIOBI	DVBI	AVBI	—	ADCRY	—
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OSCC	—	—	—	—	—	—	—	—	—	ADCCD1	ADCCD0	—	—	XTE	RCE	—
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits indicated by "—" are unused.

Bits indicated by "DB" have read/write access only in background or debug mode. These bits are cleared after a POR.

Bits indicated by "DW" are only written to in debug mode. These bits are cleared after a POR.

The OSCC register is cleared to 0002h after a POR and is not affected by other forms of reset.