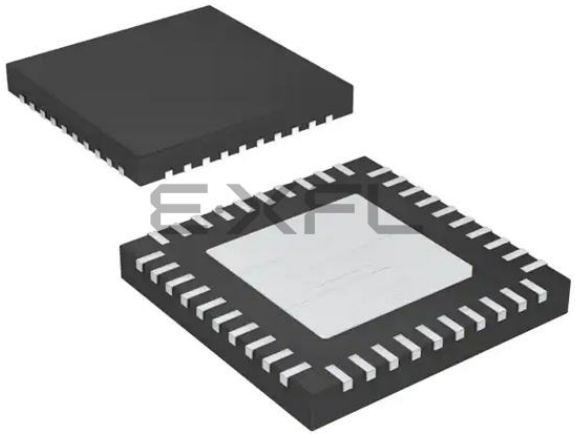
Analog Devices Inc./Maxim Integrated - MAXQ7670ATL/V+ Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	7
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-TQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq7670atl-v

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MEMORY SECTION						
Flash Memory Size		Program or data storage		64		KB
Flash Page Size		16-bit word size		256		Words
Flash Erase/Write Endurance		Program or data (Note 7)	10,000			Cycles
Flash Data Retention (Note 7)		All flash, T_A = +25°C	100			Years
		All flash, T_A = +85°C	15			
Flash Erase Time		Flash page erase	20		50	ms
		Entire flash mass erase	200		500	
Flash Programming Time		Flash single word programming	20		40	µs
		Entire flash programming	0.66		1.31	s
RAM Memory Size				2		KB
Utility ROM Size		16-bit word size		4		KWords
ANALOG SENSE PATH (Includes PGA and ADC)						
Resolution	N_{ADC}	No missing codes	10			Bits
Integral Nonlinearity	INL_{ADC}	PGA gain = 16V/V, bipolar mode, V_{IN} = ±100mV, 150.9ksps		±0.5	±1	LSB_{10}
		PGA gain = 1V/V, unipolar mode, V_{IN} = +1.0V, 250ksps		±0.4	±1	
Differential Nonlinearity	DNL_{ADC}	PGA gain = 1V/V or 16V/V		±0.4	±1	LSB_{10}
Input-Referred Offset Error		Test at T_A = +25°C, PGA gain = 1V/V or 16V/V		±1	±10	mV
Offset-Error Temperature Coefficient		PGA gain = 16V/V, bipolar mode		±2		µV/°C
Gain Error		PGA gain = 16V/V, bipolar mode, excludes offset and reference error, test at T_A = +25°C	-2		+2	%
Gain-Error Temperature Coefficient		PGA gain = 16V/V, bipolar mode		±5		ppm/°C
Conversion Clock Frequency	f_{ADCCLK}	f_{SYSCLK} = 8MHz or 16MHz	0.5		4.0	MHz
Sample Rate	f_{SAMPLE}	PGA gain = 16V/V, f_{ADCCLK} = 4MHz			150.9	ksps
		PGA gain = 1V/V, f_{ADCCLK} = 4MHz			250	
Channel Select, Track-and-Hold Acquisition Time	t_{ACQ}	PGA gain = 16V/V, 13.5 ADCCLK cycles at 4MHz		3.375		µs
		PGA gain = 1V/V, three ADCCLK cycles at 4MHz		0.75		
Conversion Time	t_{CONV}	13 ADCCLK cycles at 4MHz		3.25		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Capability		LRAPD = 0	50			mA
Output Short-Circuit Current		LRAPD = 0, AVDD shorted to AGND		100		mA
Maximum AVDD Bypass Capacitor to AGND		LRAPD = 0		0.47		µF
+2.5V (DVDD) LINEAR REGULATOR						
DVDD Output Voltage		$\overline{REGEN2}$ = GNDIO	2.38	2.5	2.62	V
No-Load Quiescent Current		$\overline{REGEN2}$ = GNDIO, all internal digital peripherals disabled		15		µA
Output Current Capability		$\overline{REGEN2}$ = GNDIO	50			mA
Output Short-Circuit Current		$\overline{REGEN2}$ = GNDIO, DV_{DD} shorted to DGND		100		mA
Maximum DVDD Bypass Capacitor to DGND		$\overline{REGEN2}$ = GNDIO		0.47		µF
SUPPLY-VOLTAGE SUPERVISORS AND BROWNOUT DETECTION						
DVDD Reset Threshold		Asserts $\overline{RESET}$ if V_{DVDD} is below this threshold	2.1		2.25	V
DVDD Interrupt Threshold		Generates an interrupt if V_{DVDD} falls below this threshold	2.25		2.38	V
Minimum DVDD Interrupt and Reset Threshold Difference				0.14		V
AVDD Interrupt Threshold		Generates an interrupt if V_{AVDD} falls below this threshold	3.0		3.15	V
DVDDIO Interrupt Threshold		Generates an interrupt if V_{DVDDIO} falls below this threshold	4.5		4.75	V
Operational Range		DV_{DD}	1		2.75	V
		AV_{DD}	1		3.6	
		DV_{DDIO}	1		5.25	
Supervisor Hysteresis				±0.7		%
CAN INTERFACE						
CAN Baud Rate		f_{CANCLK} = 8MHz			1	Mbps
CANCLK Mean Frequency Error		8MHz or 16MHz, 50ppm external crystal		60		ppm
CANCLK Total Frequency Error		8MHz or 16MHz, 50ppm external crystal; measured over a 12ms interval; mean plus peak cycle jitter		< 0.5		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Capacitance		I/O pins three-state		15		pF
Maximum Output Impedance		PD0._ = 0		880		Ω
		PD0._ = 1		450		
SYSTEM CLOCK						
System Clock Frequency	f_{SYSCLK}	From any clock source	0		16.67	MHz
SPI INTERFACE TIMING						
SPI Master Operating Frequency	f_{MCLK}	0.5 x f_{SYSCLK}			8	MHz
SPI Slave Mode Operating Frequency	f_{SCLK}				$f_{SYSCLK}/8$	MHz
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		t_{SYSCLK} - 25			ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}		t_{SYSCLK}			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		t_{SYSCLK} - 25			ns
MOSI Output Setup Time to SCLK Sample Edge	t_{MOS}		t_{SYSCLK} - 25			ns
MISO Input Setup Time to SCLK Sample Edge	t_{MIS}		30			ns
MISO Input Hold Time After SCLK Sample Edge	t_{MIH}		0			ns
SCLK Inactive to MOSI Inactive	t_{MLH}		t_{SYSCLK} - 25			ns
MOSI Input Setup Time to SCLK Sample Edge	t_{SIS}		30			ns
MOSI Input Hold Time After SCLK Sample Edge	t_{SIH}		t_{SYSCLK} + 25			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				3 t_{SYSCLK} + 25	ns
MISO Output Disabled After $\overline{SS}$ Edge Rise	t_{SLH}				2 t_{SYSCLK} + 50	ns
$\overline{SS}$ Falling Edge to MISO Active	t_{SOE}		2 t_{SYSCLK} + 2.5			ns

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SS}$ Falling Edge to First SCLK Sample Edge	t_{SSE}		2 t_{SYSCLK} + 5			ns
SCLK Inactive to $\overline{SS}$ Rising Edge	t_{SD}		t_{SYSCLK} + 10			ns
Minimum $\overline{CS}$ Pulse Width	t_{SCW}		t_{SYSCLK} + 10			ns

Note 1: All devices are 100% production tested at T_A = +25°C and +125°C. Temperature limits to T_A = -40°C are guaranteed by design.

Note 2: All analog functions disabled and all digital inputs connected to supply or ground.

Note 3: High-speed/8 mode without CAN; V_{DVDD} = +2.5V, CPU and 16-bit timer running at 2MHz from an external, 16MHz crystal oscillator; all other peripherals disabled; all digital I/Os static at V_{DVDDIO} or GNDIO; T_A = T_{MIN} to T_{MAX}.

Note 4: High-speed/1 mode with CAN; V_{DVDD} = +2.5V, CPU and 16-bit timer running at 16MHz from an external, 16MHz crystal oscillator; CAN enabled and communicating at 500kbps; all other peripherals disabled, all digital I/Os (except CANTXD and CANRXD) static at V_{DVDDIO} or GNDIO, T_A = T_{MIN} to T_{MAX}.

Note 5: Low speed, PMM1 mode without CAN; V_{DVDD} = +2.5V, CPU and one timer running from an external, 16MHz crystal oscillator in PMM1 mode; all other peripherals disabled; all digital I/Os static at V_{DVDDIO} or GNDIO, T_A = T_{MIN} to T_{MAX}.

Note 6: CAN transmitting at 500kbps; 16-bit timer output switching at 500kHz; all active I/Os are loaded with a 20pF capacitor; all remaining digital I/Os are static at V_{DVDDIO} or GNDIO, T_A = T_{MIN} to T_{MAX}.

Note 7: Guaranteed by design and characterization.

Note 8: This is not a static capacitance. It is the capacitance presented to the analog input when the T/H amplifier is in sample mode.

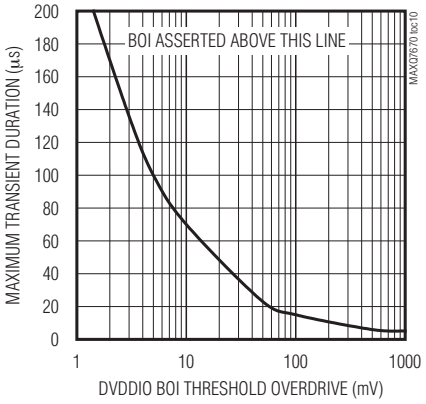
Note 9: The switched capacitor on the REFADC input can disturb the reference voltage. To reduce this disturbance, place a 0.1µF capacitor from REFADC to AGND as close as possible to REFADC.

Note 10: The digital design is fully static. However, the lower clock limit is set by a clock detect circuit. The MAXQ7670 switches to the internal RC clock if the external input goes below 166kHz. This clock detect circuit also acts to detect a crystal failure when a crystal is used.

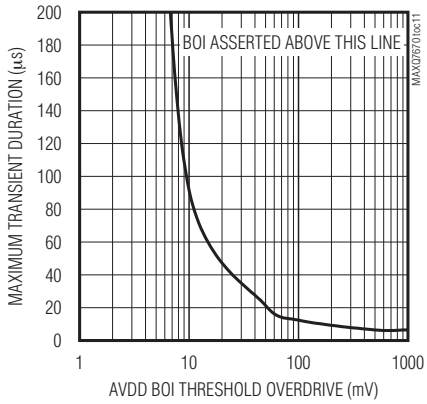
Typical Operating Characteristics (continued)

(V_{DVDDIO} = 5.0V, V_{AVDD} = 3.3V, V_{DVDD} = 2.5V, f_{SYSCLK} = 16MHz, ADC resolution = 10 bits, V_{REFDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

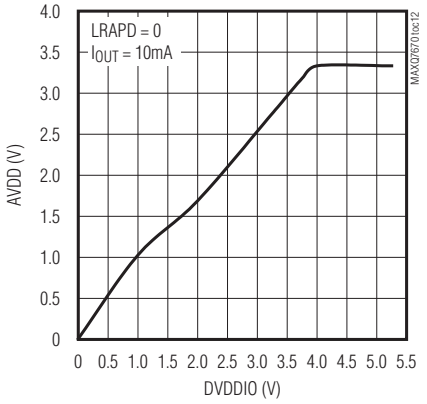
MAXIMUM DVDDIO TRANSIENT DURATION vs. BOI THRESHOLD OVERDRIVE



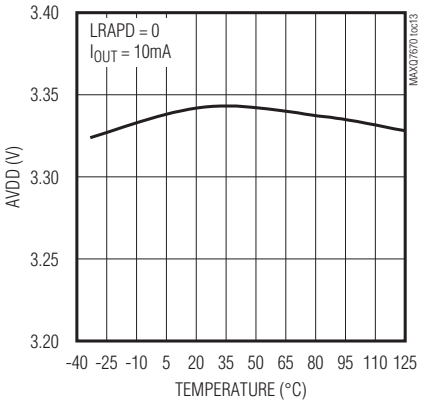
MAXIMUM AVDD TRANSIENT DURATION vs. BOI THRESHOLD OVERDRIVE



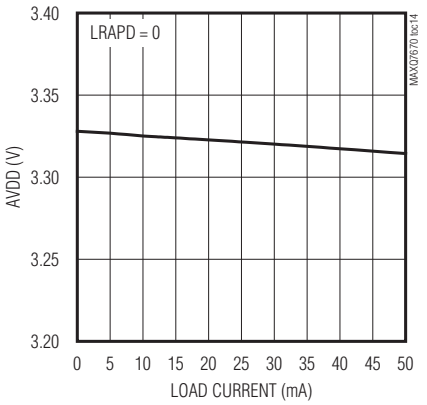
AVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. DVDDIO SUPPLY VOLTAGE



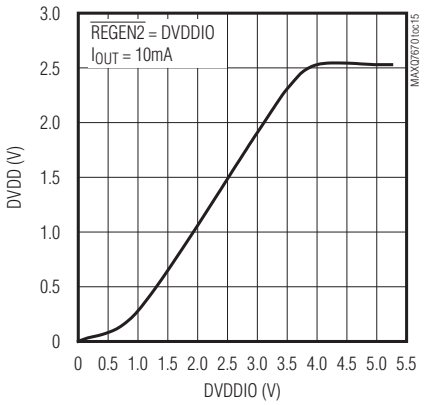
AVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. TEMPERATURE



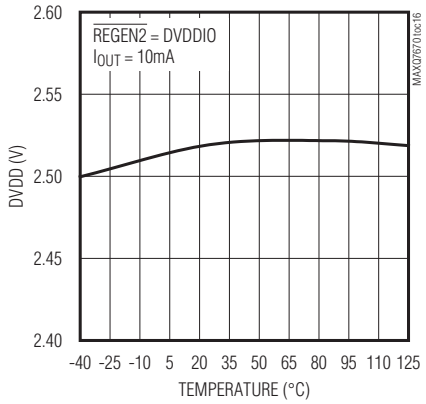
AVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



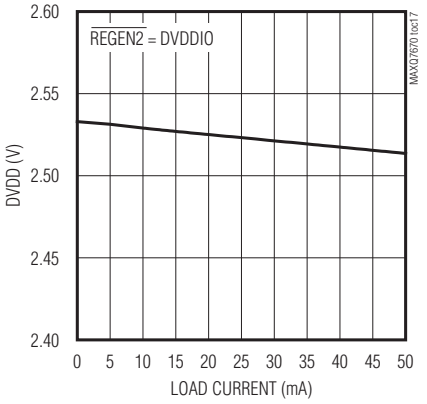
DVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. DVDDIO SUPPLY VOLTAGE



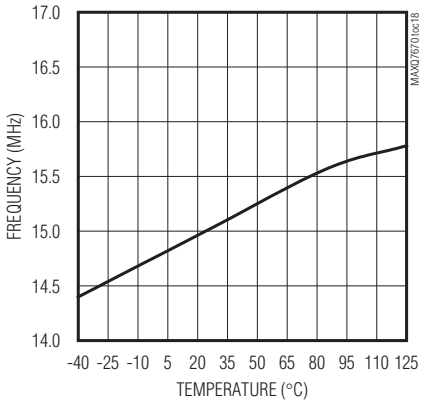
DVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. TEMPERATURE



DVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



RC OSCILLATOR OUTPUT FREQUENCY vs. TEMPERATURE



Pin Description (continued)

PIN	NAME	FUNCTION
23	SCLK	SPI Serial Clock. SCLK is the SPI interface serial clock I/O. In SPI master mode, SCLK is an output. While in SPI slave mode, SCLK is an input.
24	MOSI	SPI Serial Data I/O. MOSI is the SPI interface serial data output in master mode or serial data input in slave mode.
25	MISO	SPI Serial Data I/O. MISO is the SPI interface serial data input in master mode or serial data output in slave mode.
26	$\overline{\text{REGEN2}}$	Active-Low +2.5V Linear Regulator Enable Input. Connect $\overline{\text{REGEN2}}$ to GNDIO to enable the +2.5V linear regulator. Connect to DVDDIO to disable the +2.5V linear regulator.
27	TDO	JTAG Serial Test Data Output. TDO is the JTAG serial test, data output.
28	TMS	JTAG Test Mode Select. TMS is the JTAG test mode, select input.
29	TDI	JTAG Serial Test Data Input. TDI is the JTAG serial test, data input.
30	TCK	JTAG Serial Test Clock Input. TCK is the JTAG serial test, clock input.
31	P0.4/ ADCCNV	Port 0 Bit 4/ADC Start Conversion Control. P0.4 is a general-purpose digital I/O with interrupt/wake-up capability. ADCCNV is a firmware-configurable, rising or falling edge, start/convert signal used to trigger ADC conversions. The alternative function, ADCCNV, is selected using the register bits ACNT[2:0]. When using ADCCNV as a trigger for ADC conversion, set P0.4/ADCCNV as an input using the PD0 register. This action prevents any unintentional interference in the SARADC operation.
32	P0.5	Port 0 Bit 5. P0.5 is a general-purpose digital I/O with interrupt/wake-up capability.
33	$\overline{\text{RESET}}$	Reset Input/Output. Active-low input/output with internal 55kΩ pullup to DVDDIO. Drive low to reset the MAXQ7670. The MAXQ20 µC core holds $\overline{\text{RESET}}$ low during POR and during DVDD brownout conditions.
34	DGND	Digital Ground
35	XOUT	High-Frequency Crystal Output. Connect an external crystal to XIN and XOUT for normal operation, or leave unconnected if XIN is driven with an external clock source. Leave unconnected if an external clock source is not used.
36	XIN	High-Frequency Crystal Input. Connect an external crystal or resonator to XIN and XOUT for normal operation, or drive XIN with an external clock source. Leave unconnected if an external clock source is not used.
37	DVDD	Digital Supply Voltage. DVDD supplies internal digital core and flash memory. DVDD is directly connected to the output of the internal +2.5V linear regulator. Disable the internal regulator (through $\overline{\text{REGEN2}}$) to connect an external supply. Bypass DVDD to DGND with a 0.1µF capacitor as close as possible to the device.
40	AVDD	Analog Supply Voltage. AVDD supplies PGA and ADC. AVDD is directly connected to the output of the internal +3.3V linear regulator. Disable the internal regulator (via software) to connect an external supply. Bypass AVDD to AGND with a 0.1µF capacitor as close as possible to the device.
—	EP	Exposed Pad. Connect EP to the ground plane.

Detailed Description

The MAXQ7670 incorporates a 16-bit RISC arithmetic logic unit (ALU) with a Harvard memory architecture that addresses 64KB (32K x 16) of flash and 2048 bytes (1024 x 16) of RAM memory. This core combined with digital and analog peripherals provide versatile data-acquisition functions. The peripherals include up to seven digital I/Os, a 4-wire SPI interface, a CAN 2.0B bus, a JTAG interface, a timer, an integrated RC oscillator, two linear regulators, a watchdog timer, three power-supply supervisors, a 10-bit 250ksps SAR ADC with programmable-gain amplifier (PGA) and eight single-ended or four differential multiplexed inputs. The power-efficient MAXQ20 µC core consumes less than 1mA/MIPS. Refer to the *MAXQ7670 User's Guide* for more detailed information on configuring and programming the MAXQ7670.

Analog Input Peripheral

The integrated 10-bit ADC employs an ultra-low-power SAR-based conversion method and operates up to 250ksps with PGA = 1V/V (150.9ksps with PGA = 16V/V). The integrated 8-channel multiplexer (mux) and PGA allow the ADC to measure eight single-ended (relative to AGND) or four fully differential analog inputs with software-selectable input ranges through the PGA. See Figures 3 and 4.

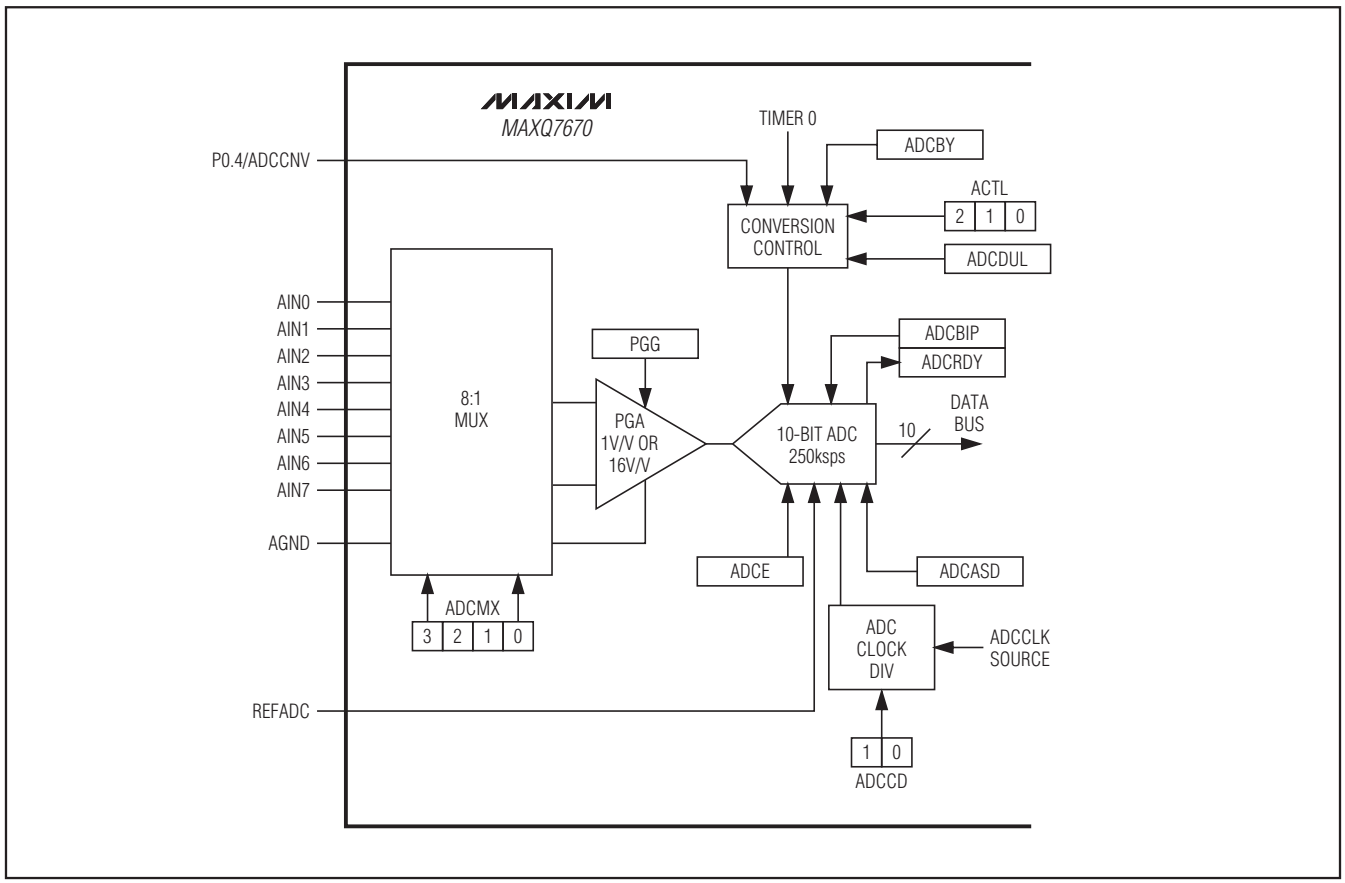


Figure 3. Simplified Analog Input Diagram (Eight Single-Ended Inputs)

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

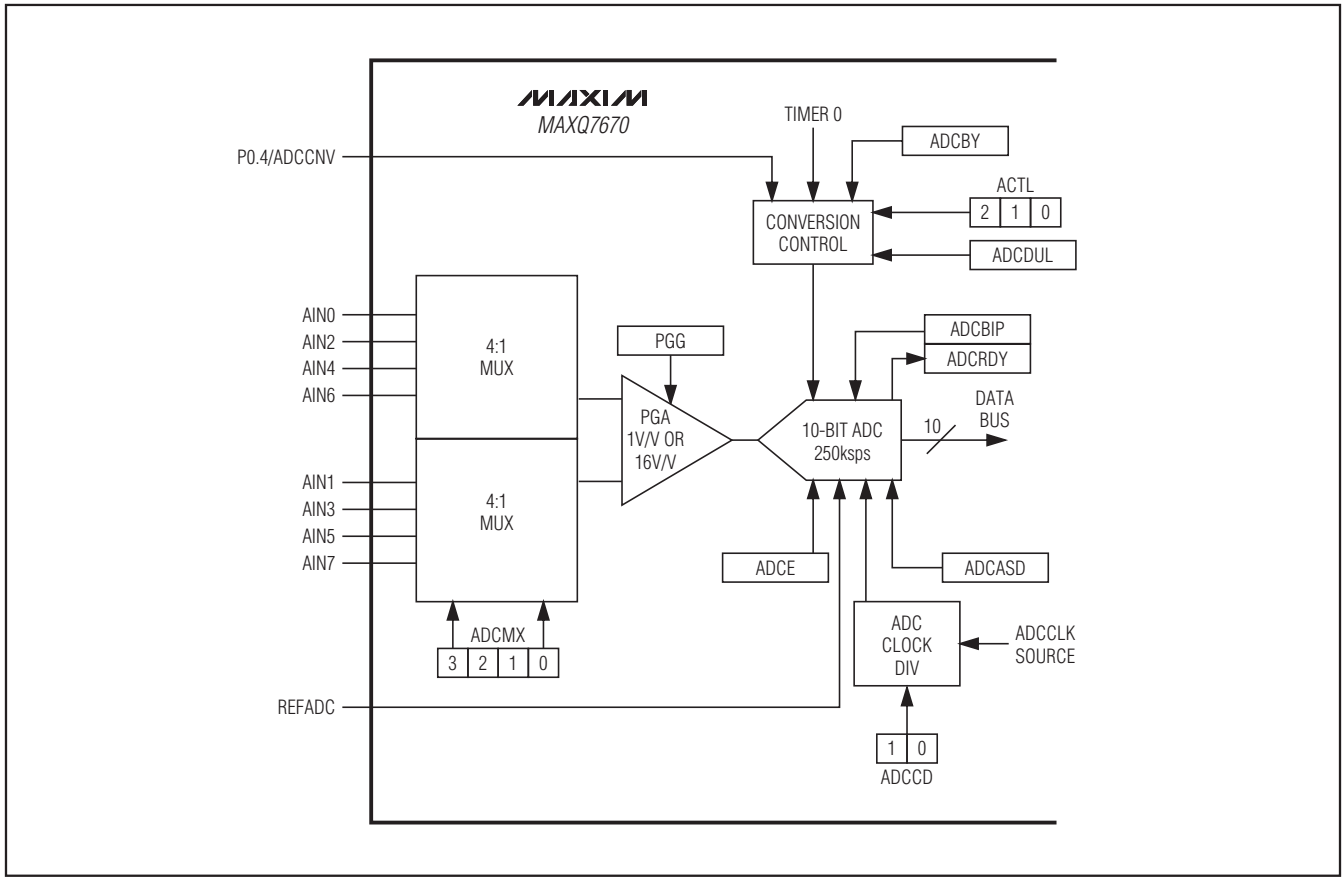


Figure 4. Simplified Analog Input Diagram (Four Fully Differential Inputs)

The MAXQ7670 ADC uses a fully differential SAR conversion technique and an integrated T/H (track and hold) block to convert voltage signals into a 10-bit digital result. Both single-ended and differential configurations are implemented using an analog input channel multiplexer that supports 8 single-ended or 4 differential channels.

In single-ended mode, the mux selects from either of the ground-referenced analog inputs AIN0–AIN7. In differential input configuration, analog inputs are selected from the following pairs: AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, and AIN6/AIN7. Table 1 shows the single-ended and differential input configurations possible for the ADC mux.

Analog Input Track and Hold

A SAR conversion in the MAXQ7670 has different T/H cycles depending on whether a gain of 1 (bypass) or a gain of 16 (PGA enabled) is selected.

Gain = 1V/V

In gain = 1V/V, the conversion has a two-stage T/H cycle. In track mode, a positive input capacitor connects to the signal channel. A negative input capacitor connects to the reference channel. After the T/H enters hold mode, the difference between the signal and the reference channel is converted to a 10-bit value. This two-stage cycle takes 16 SARCLKs to complete.

Gain = 16V/V

In gain = 16V/V, the conversion has a three-stage T/H cycle: amplification, ADC track, and ADC hold. First, the PGA tracks the selected input and reference signals. The PGA amplifies the difference between the two signals and holds the result for the next stage, ADC track. The ADC tracks and converts the PGA result into a 10-bit value. The SAR operation itself does not change irrespective of the chosen gain. This three-stage cycle takes 26.5 SARCLKs to complete. Figure 5 shows the conversion timing differences between gain = 1V/V and gain = 16V/V.

Table 1. ADC Mux Input Configurations

SAR CHANNEL SELECT (REGISTER ACNT[14:11])	SIGNAL CHANNEL INTO ADC	REFERENCE CHANNEL INTO ADC	MEASUREMENT TYPE
0000	AIN0	AGND	Single-ended measurement on AIN0
0001	AIN1	AGND	Single-ended measurement on AIN1
0010	AIN2	AGND	Single-ended measurement on AIN2
0011	AIN3	AGND	Single-ended measurement on AIN3
0100	AIN4	AGND	Single-ended measurement on AIN4
0101	AIN5	AGND	Single-ended measurement on AIN5
0110	AIN6	AGND	Single-ended measurement on AIN6
0111	AIN7	AGND	Single-ended measurement on AIN7
1000	—	—	Reserved
1001	—	—	Reserved
1010	AIN0	AIN1	AIN0/AIN1
1011	AIN2	AIN3	AIN2/AIN3
1100	AIN4	AIN5	AIN4/AIN5
1101	AIN6	AIN7	AIN6/AIN7
1110	—	—	Reserved
1111	—	—	VCIM differential zero offset trim

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

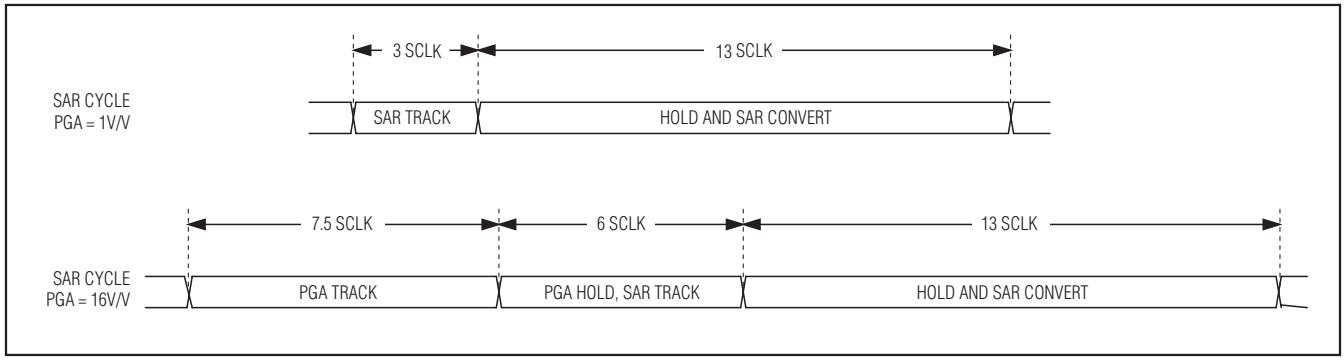


Figure 5. Conversion Timing Differences Between Gain = 1V/V and Gain = 16V/V

Input Impedance

The input-capacitance charging rate determines the time required for the T/H to acquire an input signal. The required acquisition time lengthens with the increase of the input signals source resistance. Any source below 5kΩ does not significantly affect the ADC's performance. A high-impedance source can be accommodated by placing a 1µF capacitor between the input channel and AGND. The combination of analog-input source impedance and the capacitance at the analog input creates an RC filter that limits the analog-input bandwidth.

Controlling ADC Conversions

Use the following methods to control the ADC conversion timing:

1) Software register bit control

2) Continuous conversion

3) Internal timer (T0)

4) External input through ADCCNV

Refer to the *MAXQ7670 User's Guide* for more detailed information on the ADC and mux.

POR and Brownout

The MAXQ7670 operates from a single, external +5V supply connected to the DVDDIO. DVDDIO is the supply rail for the digital I/O and the supply input for both integrated linear regulators. The +3.3V linear regulator powers AVDD, while the +2.5V linear regulator powers DVDD. Alternatively, connect $\overline{\text{REGEN2}}$ to DVDDIO and apply external power supplies to AVDD and DVDD.

Power supplies DVDDIO, DVDD, and AVDD each include a brownout monitor that alerts the µC through an interrupt when the corresponding supply voltages drop below a defined threshold. This condition is generally referred to as brownout interrupt (BOI). Enable BOI by setting the VABE, VDBE, and VIBE bits in the APE register. By continually checking for low supply voltages, appropriate action can be taken for brownout conditions.

Startup Using Internal Regulators

Once the +5V DVDDIO supply reaches approximately 1.25V, the +2.5V linear regulator turns on and DVDD begins ramping. Between the DVDD levels of 1V and the reset threshold, the DVDD monitor holds $\overline{\text{RESET}}$ low. DVDD releases $\overline{\text{RESET}}$ after reaching the reset threshold. The MAXQ7670 jumps to the reset vector location (8000h in the utility ROM). During this time, DVDD finishes ramping to its nominal voltage of +2.5V.

During this POR time, the software-enabled +3.3V linear regulator remains off. Turn on the +3.3V linear regulator after the MAXQ7670 has completed its bootup routines and is running application code. To turn on the +3.3V regulator, set the LRAPD bit in the APE register to 0. The AVDD supply begins ramping to its nominal voltage of +3.3V.

Brownout Detectors

The MAXQ7670 features brownout monitors for the +5V DVDDIO, +3.3V AVDD, and +2.5V DVDD power supplies. When enabled, these monitors generate interrupts when DVDDIO, AVDD, or DVDD fall below their respective brownout thresholds. Monitoring the supply rails alerts the µC to brownout conditions so appropriate action can be taken. Under normal conditions the DVDDIO brownout monitor signals a falling +5V supply before the DVDD or AVDD brownout monitors indicate that the +2.5V or +3.3V are falling. The exceptions to this condition are:

- If either DVDD or AVDD are externally powered and the source of power is removed
- If there is some type of device failure that pulls the regulator outputs low without affecting the +5V DVDDIO supply

Timer and PWM

The MAXQ7670 includes a 16-bit timer channel. The timer offers two ports, T0 and T0B, to facilitate PWM outputs, and capture timing events. The autoreload 16-bit timer/counter offers the following functions:

- 8-/16-bit timer/counter
- Up/down autoreload
- Counter function of external pulse
- Capture
- Compare
- PWM output
- Event timer
- System supervisor

Refer to the *MAXQ7670 User's Guide* and Application Note 3205: *Using Timers in the MAXQ Family of Microcontrollers* for more information about the timer module.

CAN Interface Bus

The MAXQ7670 incorporates a fully compliant CAN 2.0B controller.

Two groups of registers provide the µC interface to the CAN controller. To simplify the software associated with the operation of the CAN controllers, most of the global CAN status and controls as well as the individual message center control/status registers are located in the peripheral register map. The remaining registers associated with the data identification, identification masks, format, and data are located in a dual port memory to allow the CAN controller and the processor access to the required functions. The CAN controller can directly access the dual port memory. The processor accesses the dual port memory through a dedicated interface that consists of the CAN 0 data pointer (C0DP) and the CAN 0 data buffer (C0DB) special function registers. See Figure 9 for CAN controller details.

CAN Functional Description

The CAN module stores up to 15 messages. Each message consists of an acceptance identifier and 8 bytes of data. The MAXQ7670 supports both the standard 11-bit and extended 29-bit identification modes.

Configure each of the first 14 message centers either to transmit or receive. Message center 15 is a receive-only center, storing any message that centers 1–14 do not accept.

A message center only accepts an incoming message if the following conditions are satisfied:

- The incoming message's arbitration value matches the message center's acceptance identifier
- The first 2 data bytes of the incoming message match the bytes in the media arbitration registers (C0MA0 and C0MA1)

Use the global mask registers to mask out bits in the incoming message that do not require a comparison.

A message center, configured to transmit, meets these conditions: T/R = 1, TIH = 0, DTUP = 1, MSRDY = 1, and MTRQ = 1. The message center transmits its contents when it receives an incoming request message containing the same identifier (i.e., a remote frame).

Global control and status registers in the CAN unit enable the µC to evaluate error messages, validate and locate new data, establish the bus timing for the CAN bus, establish the identification mask bits, and verify the source of individual messages. In addition, each message center is individually equipped with the necessary status and controls to establish directions, interrupt generation, identification mode (standard or extended), data field size, data status, automatic remote frame request and acknowledgment, and masked or nonmasked identification acceptance testing.

JTAG Interface Bus

The joint test action group (JTAG) IEEE® 1149.1 standard defines a unique method for in-circuit testing and programming. The MAXQ7670 conforms to this standard, implementing an external test access port (TAP) and internal TAP controller for communication with a JTAG bus master, such as an automatic test equipment (ATE). For detailed information on the TAP and TAP controller, refer to IEEE Standard 1149.1 on the IEEE website at www.standards.ieee.org. The JTAG on the MAXQ7670 does not support boundary scan test capability.

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frequency is limited to SYSCLK/2 in master mode and SYSCLK/8 in slave mode. Figure 10 shows the functional diagram of the SPI port. Figures 1 and 2 illustrate the timing parameters listed in the *Electrical Characteristics* table.

General-Purpose Digital I/Os

The MAXQ7670 provides seven general-purpose digital I/Os (GPIOs). Some of the GPIOs include an additional special function (SF), such as a timer input/output. For example, the state of P0.6/T0 is programmable to depend on timer channel 0 logic. When used as a port, each I/O is configurable for high-impedance, weak pullup to DVDDIO or pulldown to GNDIO. At power-up, each GPIO is configured as an input with a pullup to DVDDIO. In addition, each GPIO can be programmed to cause an interrupt (on falling or rising edges). In stop mode, use any interrupt to wake-up the device.

The port direction (PD) register determines the input/output direction of each I/O. The port output (PO) register contains the current state of the logic output buffers. When an I/O is configured as an output, writing to the PO register controls the output logic state. Reading the PO register shows the current state of the output buffers, independent of the data direction. The port input (PI) register is a read-only register that always reflects the logic state of the I/Os.

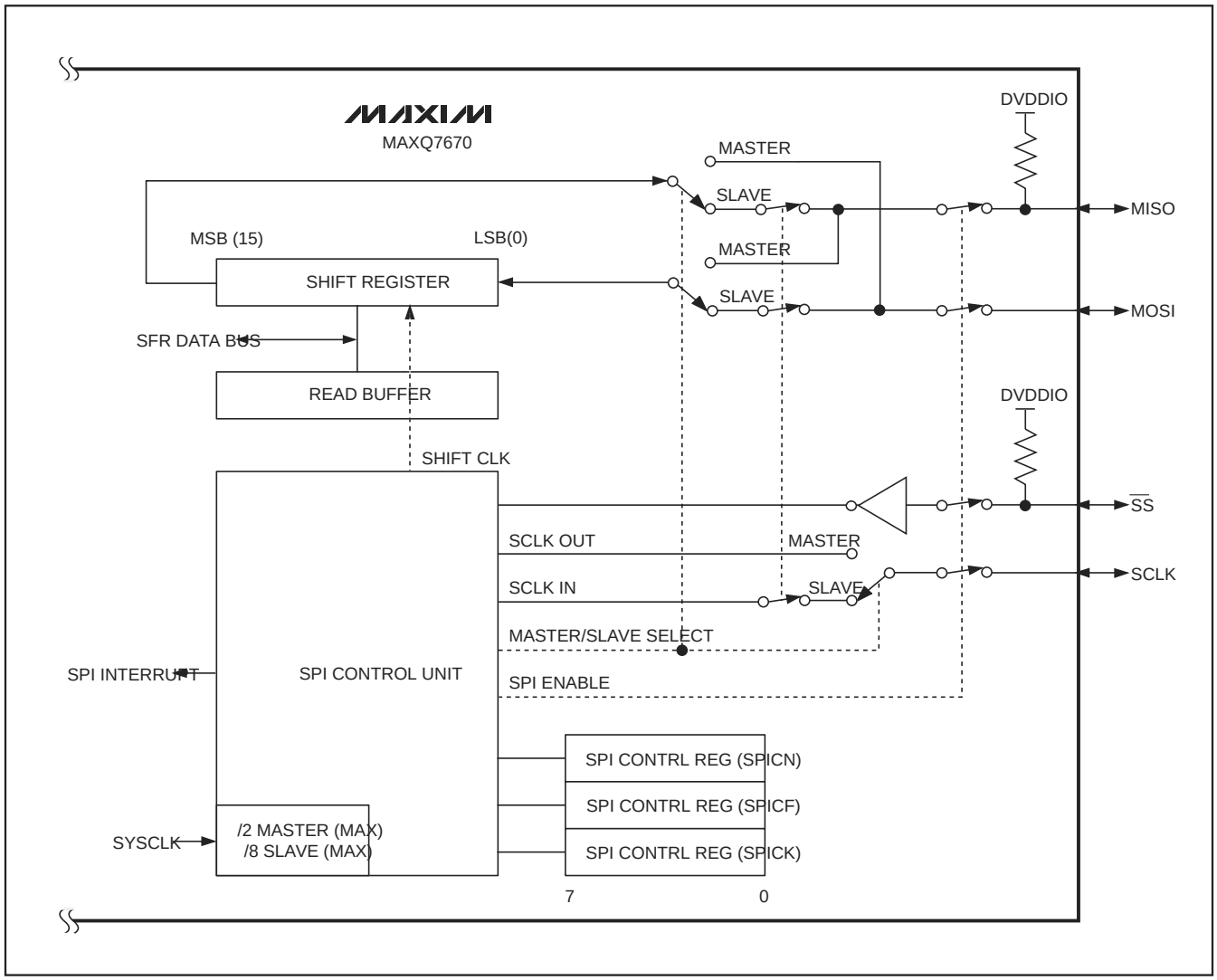

Figure 10. SPI Functional Diagram

The DVDD reset supervisor resets the MAXQ7670 when the +2.5V DVDD falls below the reset threshold. The processor remains in reset until DVDD returns above the reset threshold. The µC does not execute commands in reset mode. See Figure 6 for the µC response to DVDD brownout and reset.

Refer to the *MAXQ7670 User's Guide* for detailed programming information, and a more thorough description of POR and brownout behavior.

Internal 3.3V Linear Regulator

The integrated 3.3V 50mA linear regulator or an external 3.3V supply powers AVDD. The integrated 3.3V regulator is inactive upon power-up. Enable the integrated regulator with software programming after power-up. When using an external supply, connect a regulated 3.3V supply to AVDD after applying DVDDIO.

Internal 2.5V Linear Regulator

The integrated 2.5V 50mA linear regulator or an external 2.5V supply applied at DVDD powers DVDD. Connect REGEN2 to GNDIO to enable the integrated regulator. Connect REGEN2 to DVDDIO to use an external supply. When using an external supply, connect a regulated 2.5V supply to DVDD after applying DVDDIO.

DVDDIO Current Requirements

Both internal linear regulators are capable of supplying up to 50mA each. When using the regulators to power AVDD and DVDD and to provide power to external devices, make sure DVDDIO's power input can source a current greater than the sum of the MAXQ7670 supply current and the load currents of the two regulators.

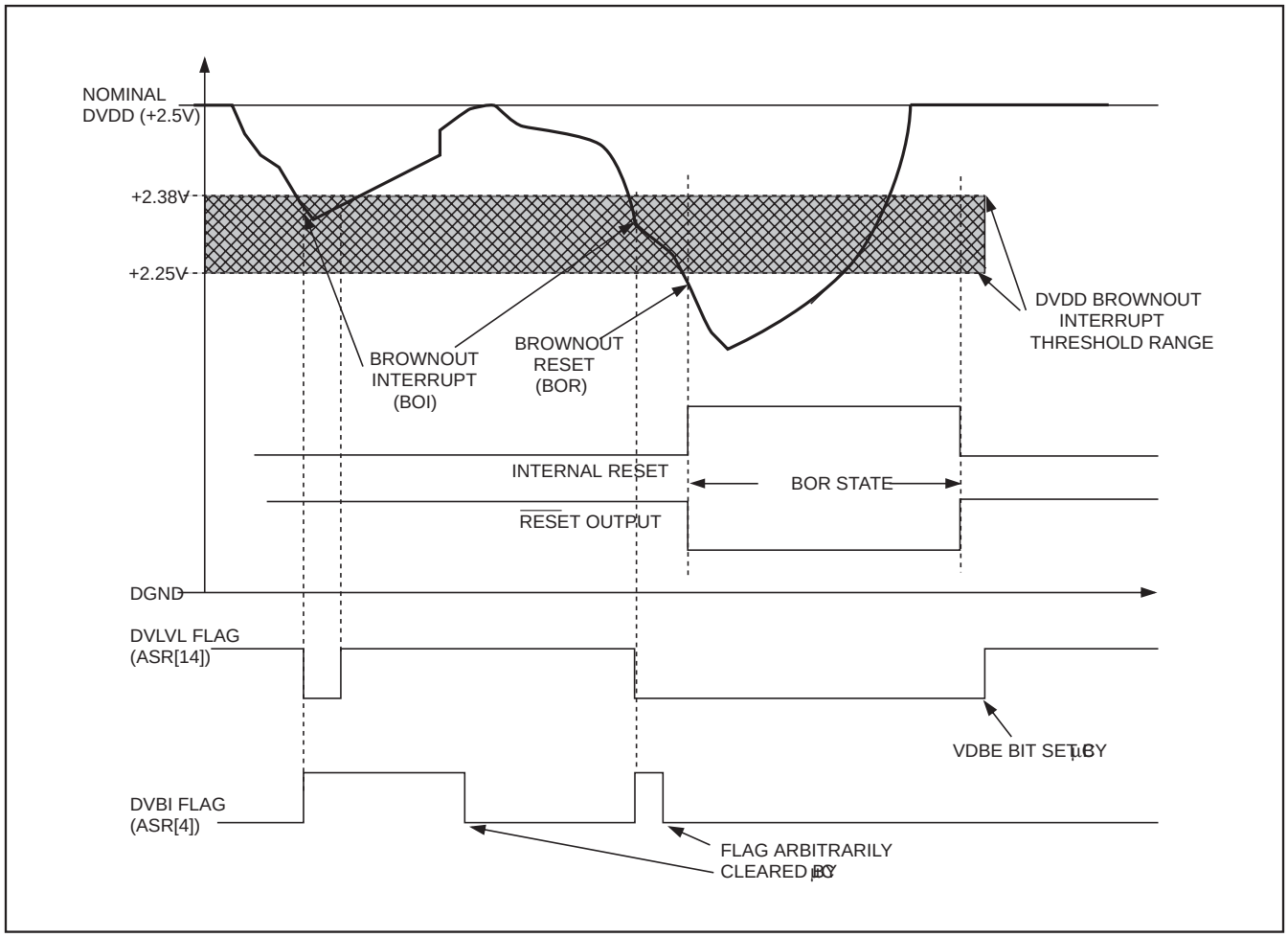

Figure 6. DVDD Brownout and Reset Behavior

Table 3. System Register Bit and Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AP									—	—	—	—	AP (4 Bits)			
									0	0	0	0	0	0	0	0
APC									CLR	IDS	—	—	—	MOD2	MOD1	MOD0
									0	0	0	0	0	0	0	0
PSF									Z	S	—	GPF1	GPF0	OV	C	E
									1	0	0	0	0	0	0	0
IC									—	—	CGDS	—	—	—	INS	IGE
									0	0	0	0	0	0	0	0
IMR									IMS	—	IM5	IM4	IM3	IM2	IM1	IM0
									0	0	0	0	0	0	0	0
SC									TAP	—	CDA1	CDA0	UPA	ROD	PWL	—
									1	0	0	0	0	0	s*	0
IIR									IIS	—	II5	II4	II3	II2	II1	II0
									0	0	0	0	0	0	0	0
CKCN									XT	—	RGMD	STOP	SWB	PMME	CD1	CD0
									s*	0	s*	0	0	0	0	1
WDCN									POR	EWDI	WD1	WD0	WDIF	WTRF	EWT	RWT
									s*	s*	0	0	0	s*	s*	0
A[n] (0..15)	A[n] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PFX[n] (0..15)	PFX[n] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IP	IP (16 Bits)															
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SP	—	—	—	—	—	—	—	—	—	—	—	—	SP (4 Bits)			
	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
IV	IV (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[0]	LC[0] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[1]	LC[1] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OFFS									OFFS (8 Bits)							
									0	0	0	0	0	0	0	0
DPC	—	—	—	—	—	—	—	—	—	—	—	WBS2	WBS1	WBS0	SDPS1	SDPS0
	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
GR	GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRL									GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
									0	0	0	0	0	0	0	0
BP	BP (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRS	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0	GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRH									GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
									0	0	0	0	0	0	0	0
GRXL	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FP	FP (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP[0]	DP[0] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP[1]	DP[1] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

*Bits indicated by an "s" are only affected by a POR and not by other forms of reset. These bits are set to 0 after a POR. Refer to the *MAXQ7670 User's Guide* for more information.