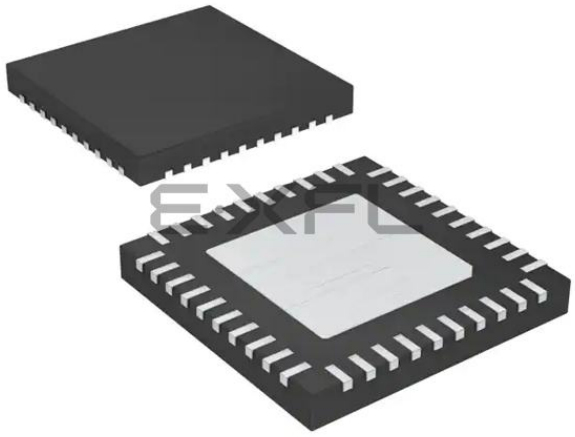
Analog Devices Inc./Maxim Integrated - MAXQ7670ATL+ Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	7
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-TQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq7670atl

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

ABSOLUTE MAXIMUM RATINGS

DVDD to DGND .....-0.3V to +3V
DVDDIO to GNDIO .....-0.3V to +5.5V
AVDD to AGND .....-0.3V to +4V
DGND to GNDIO. .....-0.3V to +0.3V
GNDIO to AGND. .....-0.3V to +0.3V
AGND to DGND.....-0.3V to +0.3V
Analog Inputs to AGND.....-0.3V to (V_{AVDD} + 0.3V)
$\overline{RESET}$, Digital Inputs/Outputs to GNDIO .....-0.3V to (V_{DVDDIO} + 0.3V)
XIN, XOUT to DGND .....-0.3V to (V_{DVDD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 36mW/°C above +70°C) 2857mW
Continuous Current into Any Pin.....±50mA
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage Ranges	DVDD	$\overline{REGEN2}$ = DVDDIO, $DV_{DD} \le AV_{DD}$, $DV_{DD} \le DV_{DDIO}$	2.25	2.5	2.75	V
	AVDD	LRAPD = 1, $AV_{DD} \le DV_{DDIO}$	3.0	3.3	3.6	
	DVDDIO		4.5	5.0	5.25	
AVDD Supply Current	I_{AVDD}	Shutdown (Note 2)		3	10	µA
		All analog functions enabled		6	7	mA
Analog Module Incremental Subfunction Supply Current	ΔI_{AVDD}	ADC, 50ksps, 4MHz ADCCLK		5200		µA
		ADC, 250ksps, 4MHz ADCCLK		5600		
		AVDD brownout interrupt monitor		3		
		PGA enabled		5500		
DVDD Supply Current	I_{DVDD}	CPU in stop mode, all peripherals disabled		25	200	µA
		High speed/2MHz mode (Note 3)		2.0	2.5	mA
		High speed/16MHz mode (Note 4)		11.3		
		Low speed/625kHz mode (Note 5)		0.95		
		Program flash erase or write		14	23	
Digital Peripheral Incremental Subfunction Supply Current	ΔI_{DVDD}	DVDDIO brownout reset monitor		1		µA
		HF crystal oscillator		60		
		Internal fixed-frequency oscillator		50		
DVDDIO Supply Current	I_{DVDDIO}	All digital I/Os static at GNDIO or DV_{DDIO}		2	20	µA
		CAN transmitting, timer output switching (Note 6)		0.2	0.3	mA

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Channel Select Plus Conversion Time	t_{ACQ} + t_{CONV}	PGA gain = 16V/V, 26.5 ADCCLK cycles at 4MHz		6.625		µs
		PGA gain = 1V/V, 16 ADCCLK cycles at 4MHz		4		
Turn-On Time	t_{RECOV}			10		µs
Aperture Delay				60		ns
Aperture Jitter				100		ps_{P-P}
Differential Input Voltage Range		At AIN0–AIN7, unipolar mode, PGA gain = 1V/V	0		V_{REFADC}	V
		At AIN0–AIN7, unipolar mode, PGA gain = 16V/V	0		0.125	
		At AIN0–AIN7, bipolar mode, PGA gain = 1V/V	$-V_{REFADC}$ /2		$+V_{REFADC}$ /2	
		At AIN0–AIN7, bipolar mode, PGA gain = 16V/V	$-V_{REFADC}$ /32		$+V_{REFADC}$ /32	
Absolute Input Voltage Range		At AIN0–AIN7	0		V_{AVDD}	V
Input Leakage Current		At AIN0–AIN7		±0.1		µA
Input-Referred Noise		At AIN0–AIN7, PGA gain = 16V/V		50		$µV_{RMS}$
		At AIN0–AIN7, PGA gain = 1V/V		400		
Small-Signal Bandwidth (-3dB)		V_{IN} = 12mV_{P-P}, PGA gain = 16V/V		33		MHz
		V_{IN} = 200mV_{P-P}, PGA gain = 1V/V		23		
Large-Signal Bandwidth (-3dB)		V_{IN} = 150mV_{P-P}, PGA gain =16V/V		33		MHz
		V_{IN} = 2.5V_{P-P}, PGA gain = 1V/V		19		
Input Capacitance (Note 8)		Single-ended, any AIN0–AIN7, PGA gain = 16V/V		16		pF
		Single-ended, any AIN0–AIN7, PGA gain = 1V/V		13		
Input Common-Mode Rejection Ratio	CMRR	AIN0–AIN7, V_{CM} = differential input range		75		dB
Power-Supply Rejection Ratio	PSRR	AV_{DD} = 3.0V to 3.6V		90		dB
EXTERNAL REFERENCE INPUTS						
REFADC Input Voltage Range			1.0	3.3	V_{AVDD}	V
REFADC Leakage Current		ADC disabled		1		µA
Input Capacitance		(Note 9)		20		pF
+3.3V (AVDD) LINEAR REGULATOR						
AVDD Output Voltage		LRAPD = 0	3.15	3.3	3.45	V
No-Load Quiescent Current		LRAPD = 0, all internal analog peripherals disabled		10		µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-FREQUENCY CRYSTAL OSCILLATOR						
Clock Frequency		Using external crystal		8 or 16	16	MHz
		External input (Note 10)	0.166		16.67	
Stability		Excluding crystal drift		25		ppm
Startup Time		f_{SYSCLK} cycles		65,535		Cycles
XIN Input Low Voltage		Driven with external clock source			0.3 x V_{DVDD}	V
XIN Input High Voltage		Driven with external clock source	0.7 x V_{DVDD}			V
INTERNAL FIXED-FREQUENCY OSCILLATOR						
Frequency	f_{IFFCLK}	T_A = T_{MIN} to T_{MAX}	13.8	15	16.35	MHz
Tolerance		T_A = +25°C		±0.4		%
Temperature Drift		T_A = T_{MIN} to T_{MAX}		5		%
Power-Supply Rejection		T_A = +25°C, DV_{DD} = 2.25V to 2.75V		±1.5		%
RESET ($\overline{RESET}$)						
$\overline{RESET}$ Internal Pullup Resistance		Pulled up to DVDDIO		55		kΩ
$\overline{RESET}$ Output Low Voltage		$\overline{RESET}$ asserted, no external load			0.4	V
$\overline{RESET}$ Output High Voltage		$\overline{RESET}$ deasserted, no external load	0.9 x V_{DVDDIO}			V
$\overline{RESET}$ Input Low Voltage		Driven with external clock source			0.3 x V_{DVDD}	V
$\overline{RESET}$ Input High Voltage		Driven with external clock source	0.7 x V_{DVDDIO}			V
DIGITAL INPUTS (P0._, CANRXD, MISO, MOSI, $\overline{SS}$, SCLK, TCK, TDI, TMS)						
Input Low Voltage					0.8	V
Input High Voltage			2.1			V
Input Hysteresis				500		mV
Input Leakage Current		V_{IN} = GNDIO or V_{DVDDIO}, pullup disabled	-10	±0.01	+10	µA
Input Pullup Resistance				55		kΩ
Input Pulldown Resistance				55		kΩ
Input Capacitance				15		pF
DIGITAL OUTPUTS (P0._, CANTXD, MOSI, SCLK, $\overline{SS}$, TDO)						
Output Low Voltage		I_{SINK} = 0.5mA			0.4	V
Output High Voltage		I_{SOURCE} = 0.5mA	V_{DVDDIO} - 0.5			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Capacitance		I/O pins three-state		15		pF
Maximum Output Impedance		PD0._ = 0		880		Ω
		PD0._ = 1		450		
SYSTEM CLOCK						
System Clock Frequency	f_{SYSCLK}	From any clock source	0		16.67	MHz
SPI INTERFACE TIMING						
SPI Master Operating Frequency	f_{MCLK}	0.5 x f_{SYSCLK}			8	MHz
SPI Slave Mode Operating Frequency	f_{SCLK}				$f_{SYSCLK}/8$	MHz
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		t_{SYSCLK} - 25			ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}		t_{SYSCLK}			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		t_{SYSCLK} - 25			ns
MOSI Output Setup Time to SCLK Sample Edge	t_{MOS}		t_{SYSCLK} - 25			ns
MISO Input Setup Time to SCLK Sample Edge	t_{MIS}		30			ns
MISO Input Hold Time After SCLK Sample Edge	t_{MIH}		0			ns
SCLK Inactive to MOSI Inactive	t_{MLH}		t_{SYSCLK} - 25			ns
MOSI Input Setup Time to SCLK Sample Edge	t_{SIS}		30			ns
MOSI Input Hold Time After SCLK Sample Edge	t_{SIH}		t_{SYSCLK} + 25			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				3 t_{SYSCLK} + 25	ns
MISO Output Disabled After $\overline{SS}$ Edge Rise	t_{SLH}				2 t_{SYSCLK} + 50	ns
$\overline{SS}$ Falling Edge to MISO Active	t_{SOE}		2 t_{SYSCLK} + 2.5			ns

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5.0V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, V_{REFADC} = +3.3V, system clock = 16MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SS}$ Falling Edge to First SCLK Sample Edge	t_{SSE}		2 t_{SYSCLK} + 5			ns
SCLK Inactive to $\overline{SS}$ Rising Edge	t_{SD}		t_{SYSCLK} + 10			ns
Minimum $\overline{CS}$ Pulse Width	t_{SCW}		t_{SYSCLK} + 10			ns

Note 1: All devices are 100% production tested at T_A = +25°C and +125°C. Temperature limits to T_A = -40°C are guaranteed by design.

Note 2: All analog functions disabled and all digital inputs connected to supply or ground.

Note 3: High-speed/8 mode without CAN; V_{DVDD} = +2.5V, CPU and 16-bit timer running at 2MHz from an external, 16MHz crystal oscillator; all other peripherals disabled; all digital I/Os static at V_{DVDDIO} or GNDIO; T_A = T_{MIN} to T_{MAX}.

Note 4: High-speed/1 mode with CAN; V_{DVDD} = +2.5V, CPU and 16-bit timer running at 16MHz from an external, 16MHz crystal oscillator; CAN enabled and communicating at 500kbps; all other peripherals disabled, all digital I/Os (except CANTXD and CANRXD) static at V_{DVDDIO} or GNDIO, T_A = T_{MIN} to T_{MAX}.

Note 5: Low speed, PMM1 mode without CAN; V_{DVDD} = +2.5V, CPU and one timer running from an external, 16MHz crystal oscillator in PMM1 mode; all other peripherals disabled; all digital I/Os static at V_{DVDDIO} or GNDIO, T_A = T_{MIN} to T_{MAX}.

Note 6: CAN transmitting at 500kbps; 16-bit timer output switching at 500kHz; all active I/Os are loaded with a 20pF capacitor; all remaining digital I/Os are static at V_{DVDDIO} or GNDIO, T_A = T_{MIN} to T_{MAX}.

Note 7: Guaranteed by design and characterization.

Note 8: This is not a static capacitance. It is the capacitance presented to the analog input when the T/H amplifier is in sample mode.

Note 9: The switched capacitor on the REFADC input can disturb the reference voltage. To reduce this disturbance, place a 0.1µF capacitor from REFADC to AGND as close as possible to REFADC.

Note 10: The digital design is fully static. However, the lower clock limit is set by a clock detect circuit. The MAXQ7670 switches to the internal RC clock if the external input goes below 166kHz. This clock detect circuit also acts to detect a crystal failure when a crystal is used.

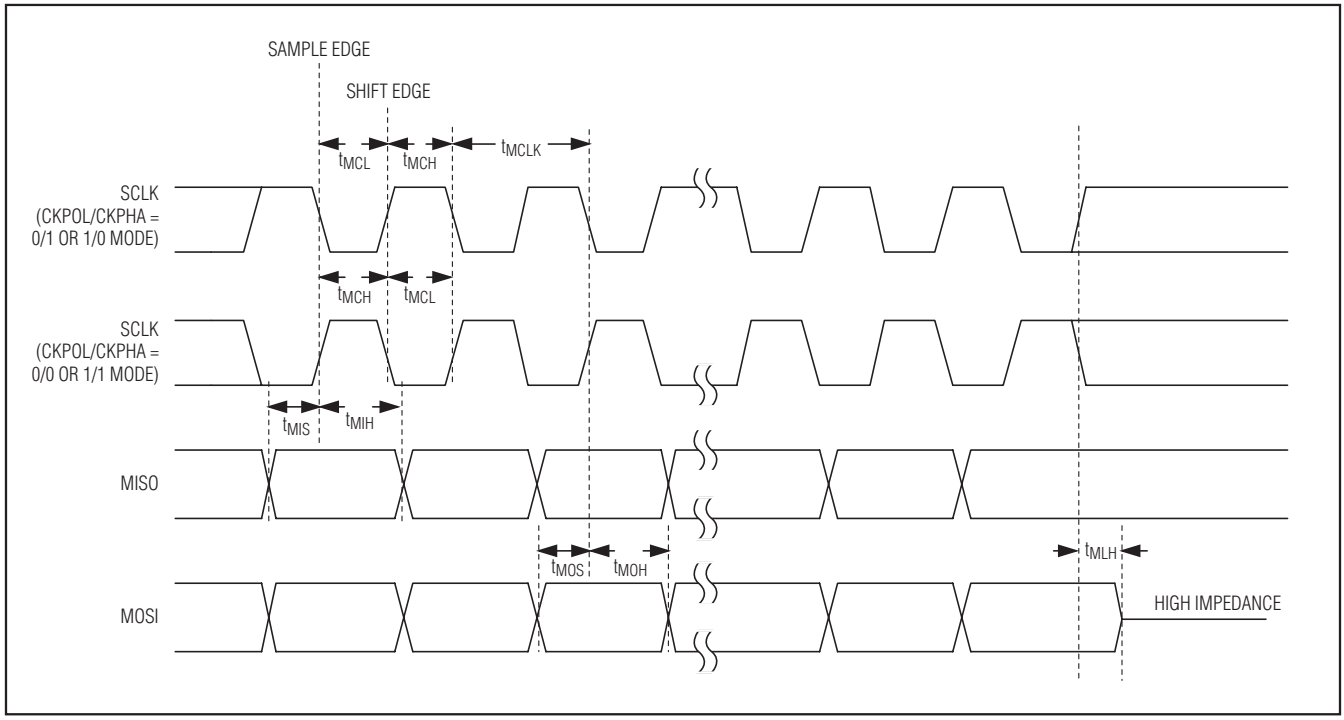


Figure 1. SPI Timing Diagram in Master Mode

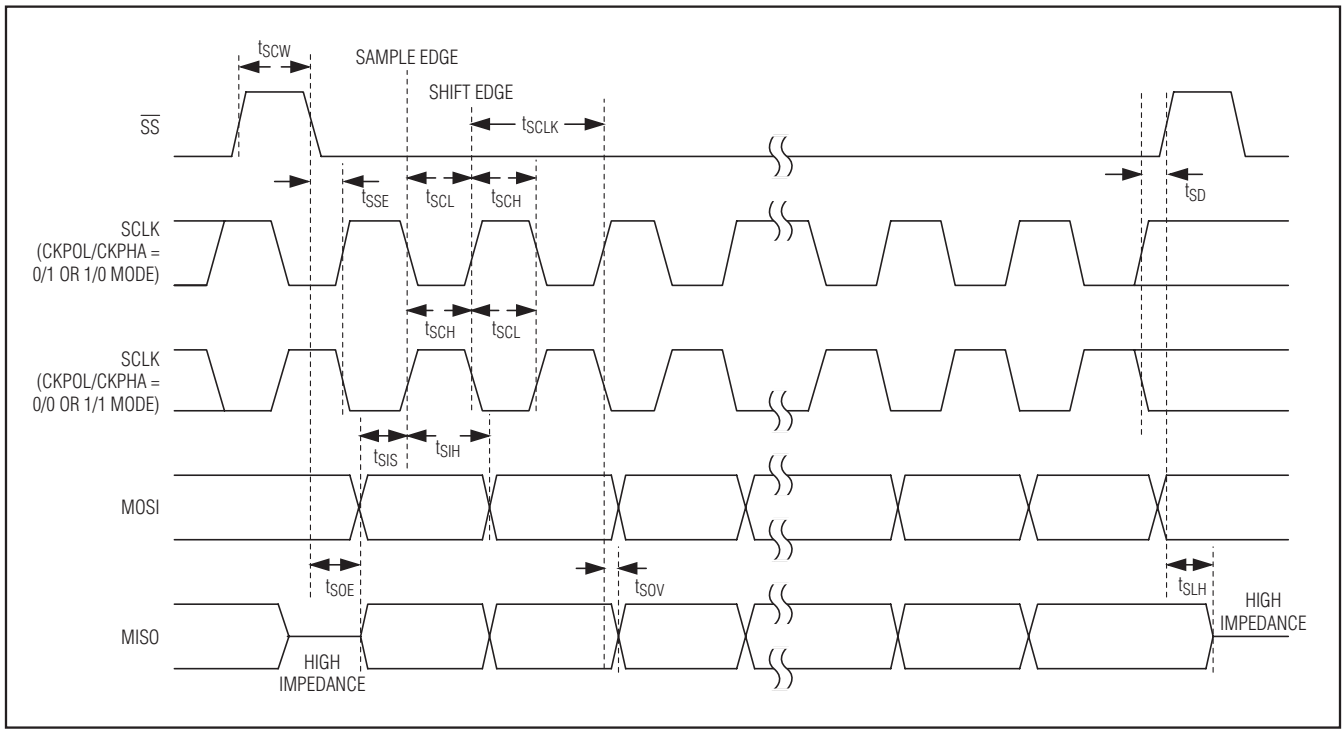


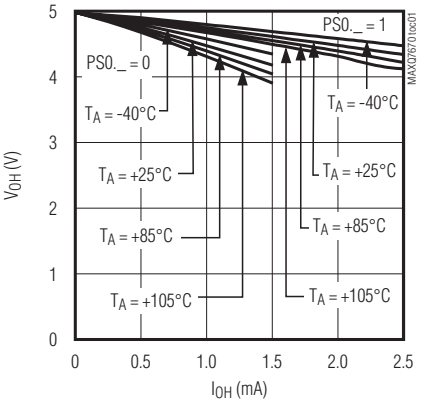
Figure 2. SPI Timing Diagram in Slave Mode

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

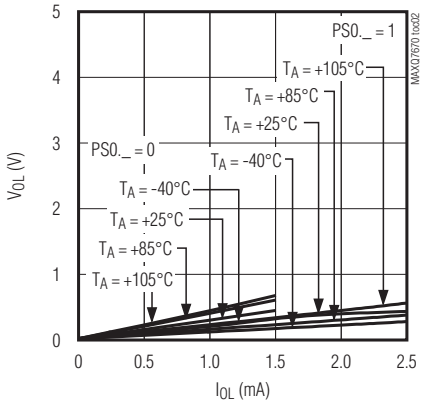
Typical Operating Characteristics

(V_{DVDDIO} = 5.0V, V_{AVDD} = 3.3V, V_{DVDD} = 2.5V, f_{SYSCLK} = 16MHz, ADC resolution = 10 bits, V_{REFDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

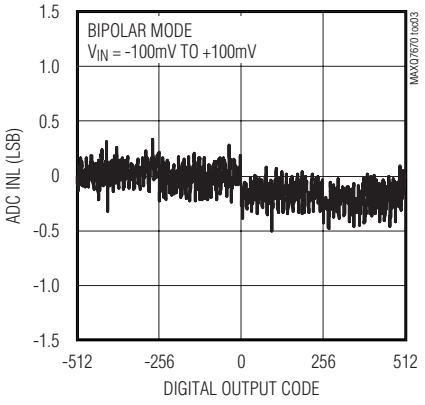
GPO._ OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



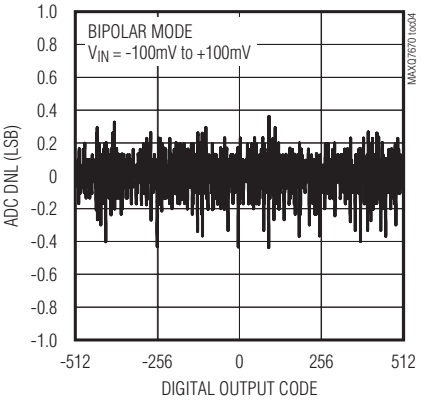
GPO._ OUTPUT LOW VOLTAGE vs. SINK CURRENT



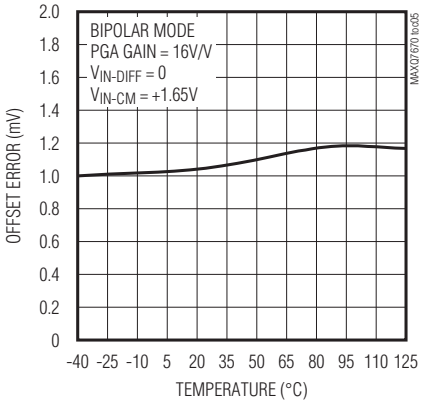
ADC INL vs. CODE (REF ADC = +3.3V, 150.9ksps, PGA GAIN = 16V/V)



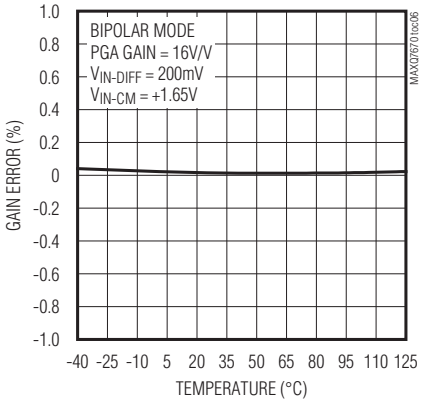
ADC DNL vs. CODE (REFADC = +3.3V, 150.9ksps, PGA GAIN = 16V/V)



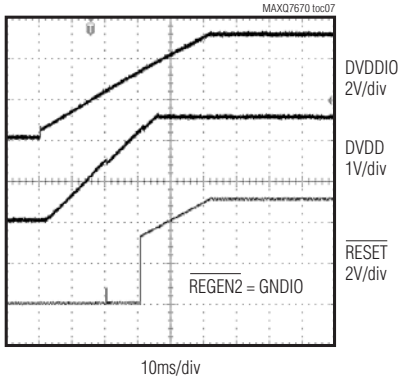
ADC OFFSET ERROR vs. TEMPERATURE



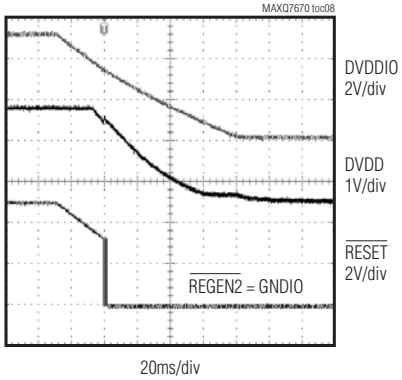
ADC GAIN ERROR vs. TEMPERATURE



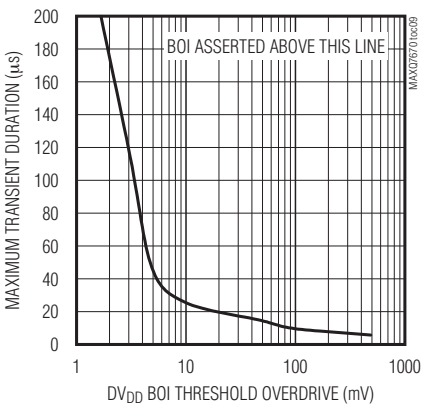
DVDD, $\overline{RESET}$ POWER-UP CHARACTERISTICS



DVDD, $\overline{RESET}$ POWER-DOWN CHARACTERISTICS



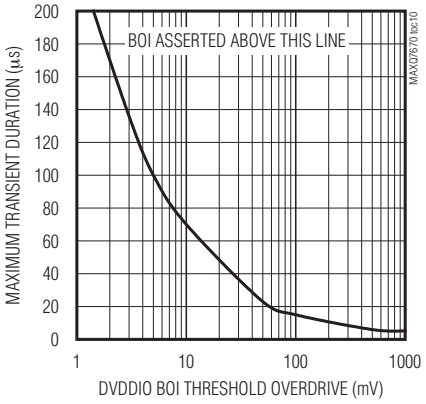
MAXIMUM DVDD TRANSIENT DURATION vs. BOI THRESHOLD OVERDRIVE



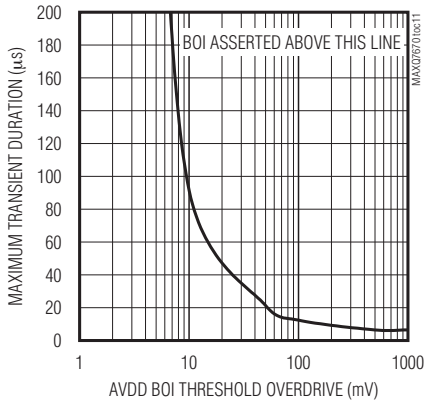
Typical Operating Characteristics (continued)

(V_{DVDDIO} = 5.0V, V_{AVDD} = 3.3V, V_{DVDD} = 2.5V, f_{SYSCLK} = 16MHz, ADC resolution = 10 bits, V_{REFDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

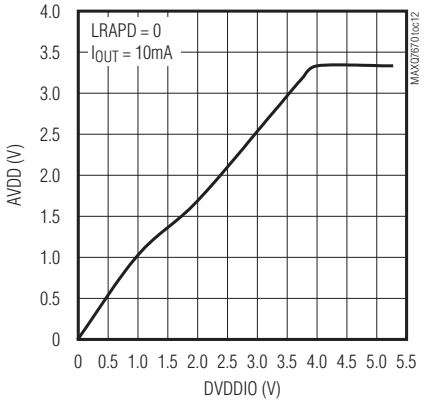
MAXIMUM DVDDIO TRANSIENT DURATION vs. BOI THRESHOLD OVERDRIVE



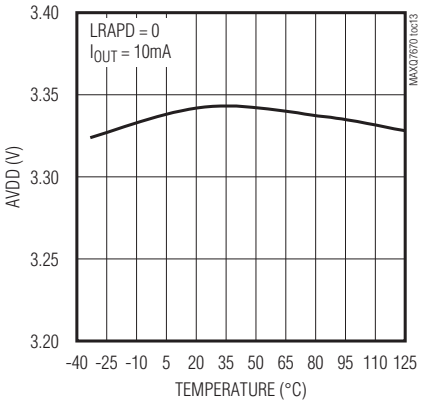
MAXIMUM AVDD TRANSIENT DURATION vs. BOI THRESHOLD OVERDRIVE



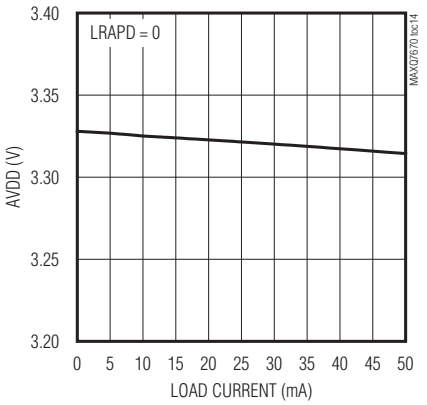
AVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. DVDDIO SUPPLY VOLTAGE



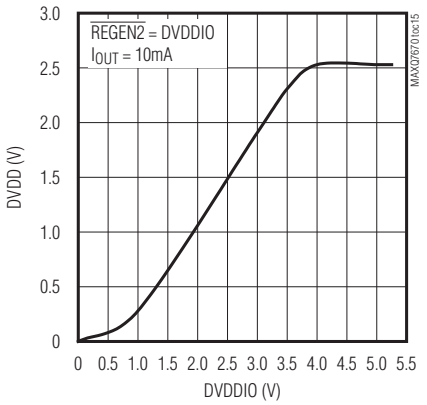
AVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. TEMPERATURE



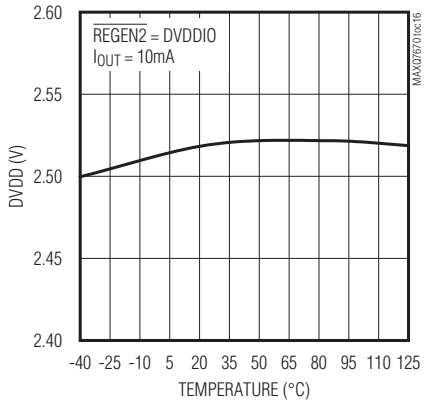
AVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



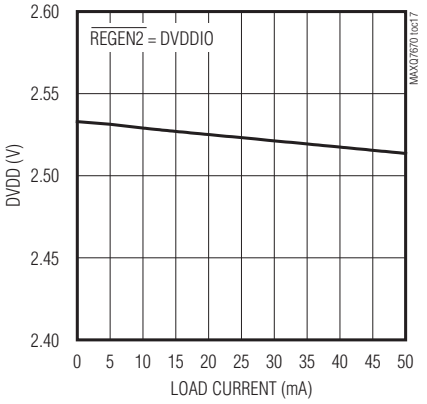
DVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. DVDDIO SUPPLY VOLTAGE



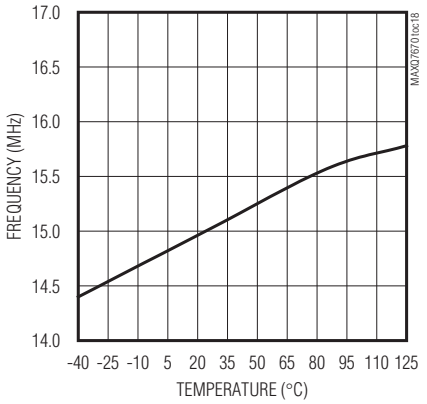
DVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. TEMPERATURE



DVDD LINEAR REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



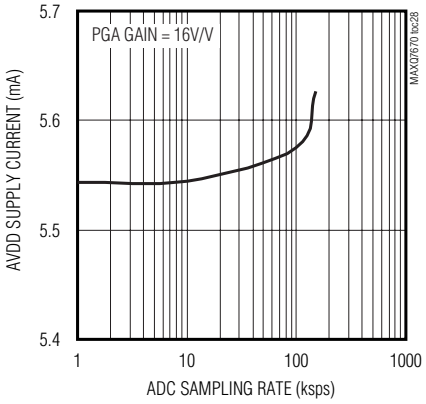
RC OSCILLATOR OUTPUT FREQUENCY vs. TEMPERATURE



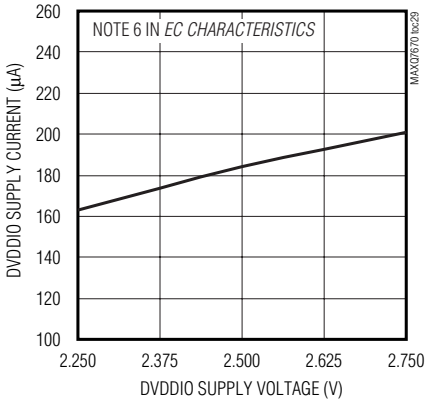
Typical Operating Characteristics (continued)

(V_{DVDDIO} = 5.0V, V_{AVDD} = 3.3V, V_{DVDD} = 2.5V, f_{SYSCLK} = 16MHz, ADC resolution = 10 bits, V_{REFDAC} = 3.3V, T_A = +25°C, unless otherwise noted.)

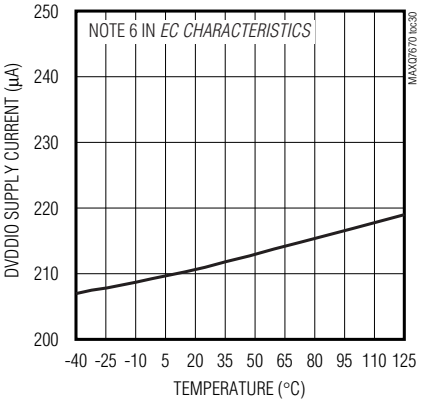
AVDD SUPPLY CURRENT vs. ADC SAMPLING RATE



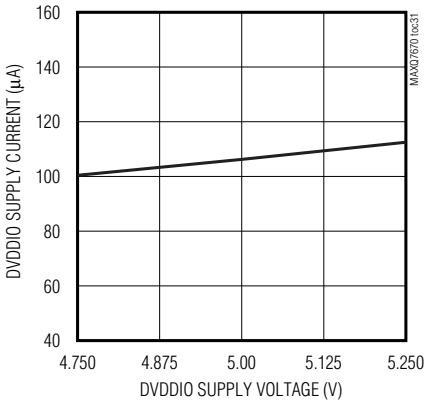
DVDDIO DYNAMIC SUPPLY CURRENT vs. DVDDIO SUPPLY VOLTAGE



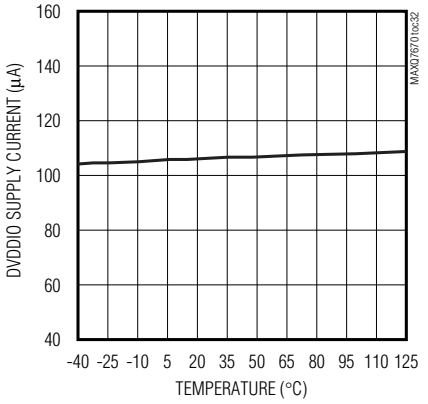
DVDDIO DYNAMIC SUPPLY CURRENT vs. TEMPERATURE



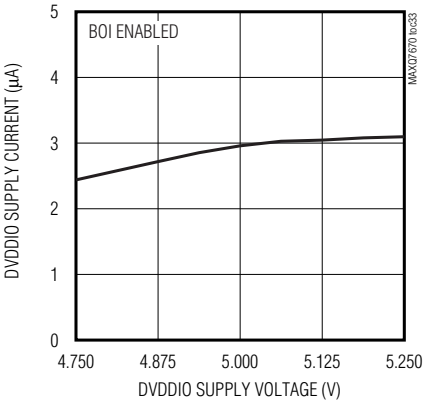
DVDDIO STATIC SUPPLY CURRENT vs. DVDDIO SUPPLY VOLTAGE



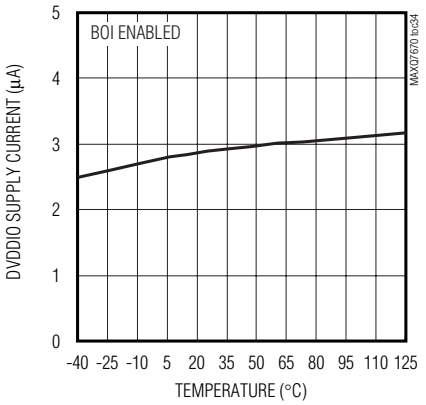
DVDDIO STATIC SUPPLY CURRENT vs. TEMPERATURE



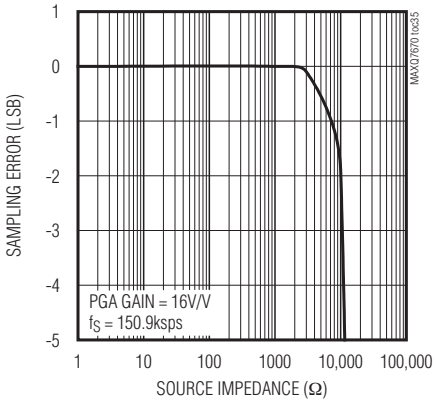
DVDDIO INCREMENTAL SUPPLY CURRENT vs. DVDDIO SUPPLY VOLTAGE



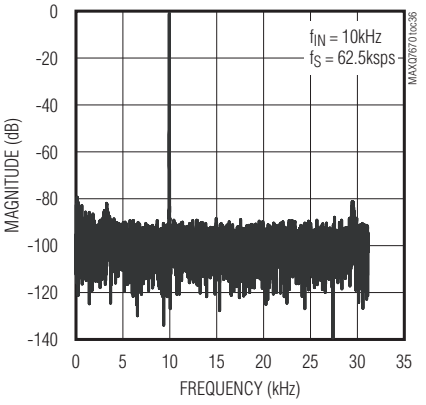
DVDDIO INCREMENTAL SUPPLY CURRENT vs. TEMPERATURE



ADC SAMPLING ERROR vs. INPUT SOURCE IMPEDANCE

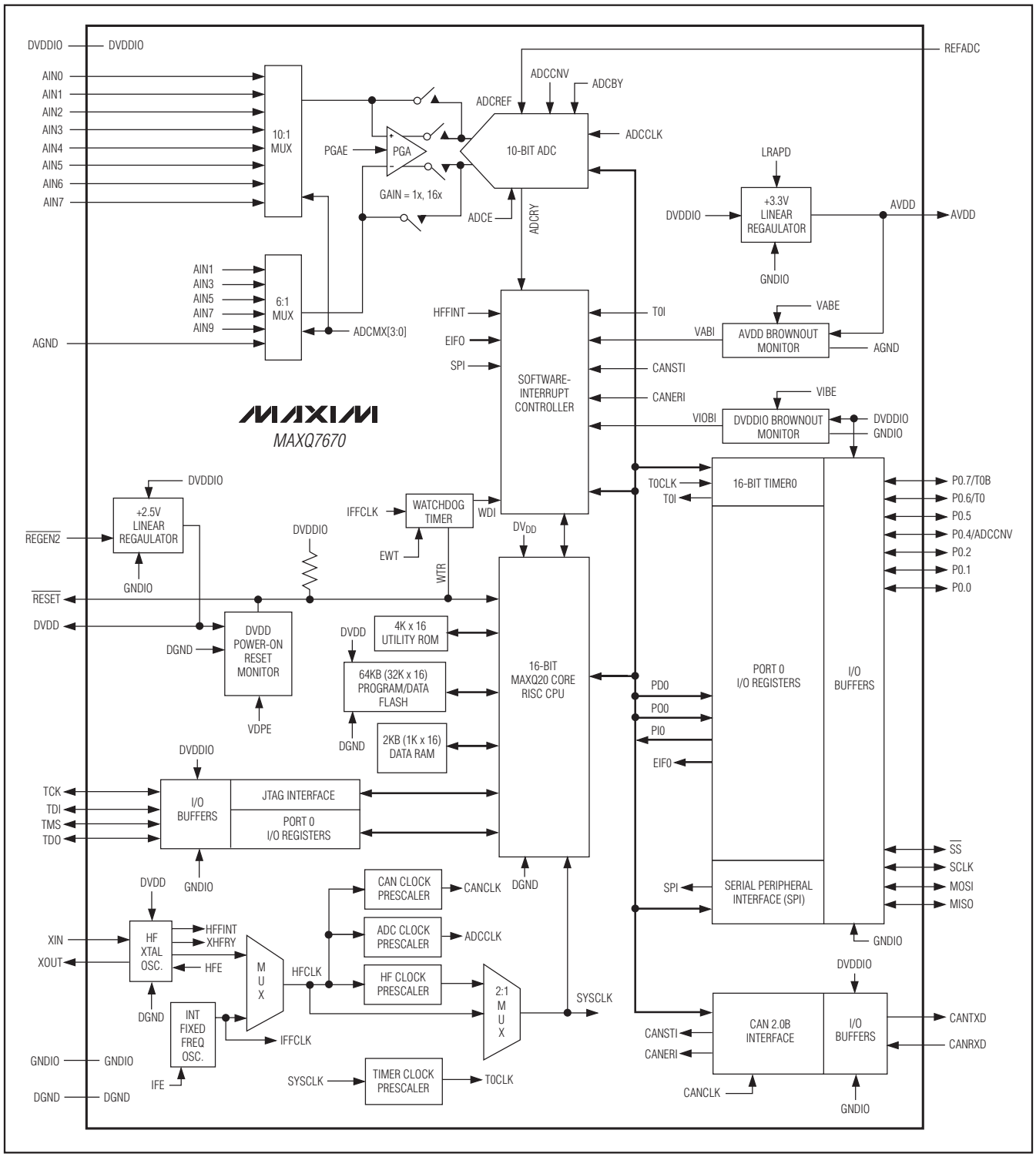


SNR



Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

Block Diagram



Detailed Description

The MAXQ7670 incorporates a 16-bit RISC arithmetic logic unit (ALU) with a Harvard memory architecture that addresses 64KB (32K x 16) of flash and 2048 bytes (1024 x 16) of RAM memory. This core combined with digital and analog peripherals provide versatile data-acquisition functions. The peripherals include up to seven digital I/Os, a 4-wire SPI interface, a CAN 2.0B bus, a JTAG interface, a timer, an integrated RC oscillator, two linear regulators, a watchdog timer, three power-supply supervisors, a 10-bit 250ksps SAR ADC with programmable-gain amplifier (PGA) and eight single-ended or four differential multiplexed inputs. The power-efficient MAXQ20 µC core consumes less than 1mA/MIPS. Refer to the *MAXQ7670 User's Guide* for more detailed information on configuring and programming the MAXQ7670.

Analog Input Peripheral

The integrated 10-bit ADC employs an ultra-low-power SAR-based conversion method and operates up to 250ksps with PGA = 1V/V (150.9ksps with PGA = 16V/V). The integrated 8-channel multiplexer (mux) and PGA allow the ADC to measure eight single-ended (relative to AGND) or four fully differential analog inputs with software-selectable input ranges through the PGA. See Figures 3 and 4.

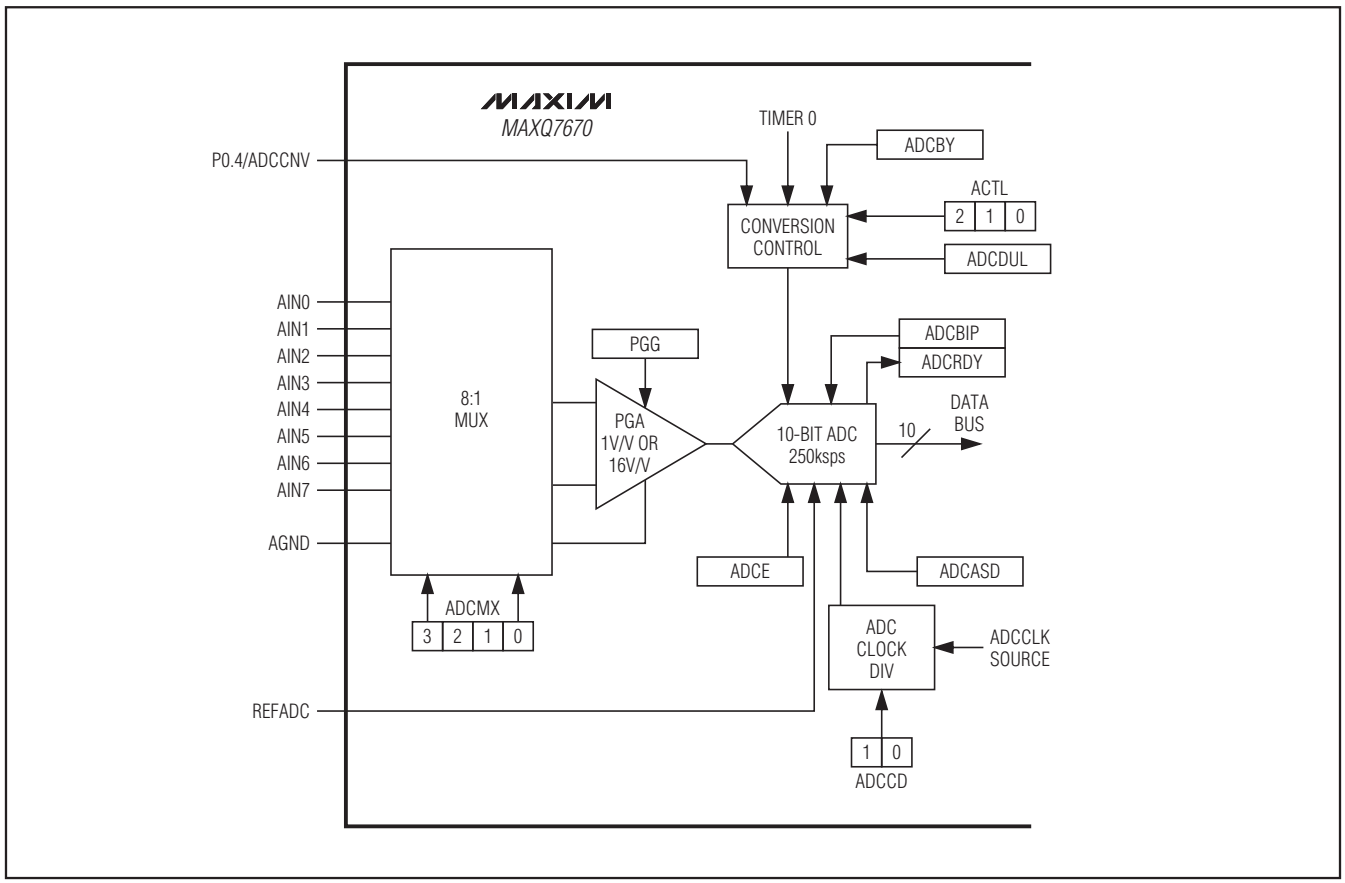


Figure 3. Simplified Analog Input Diagram (Eight Single-Ended Inputs)

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

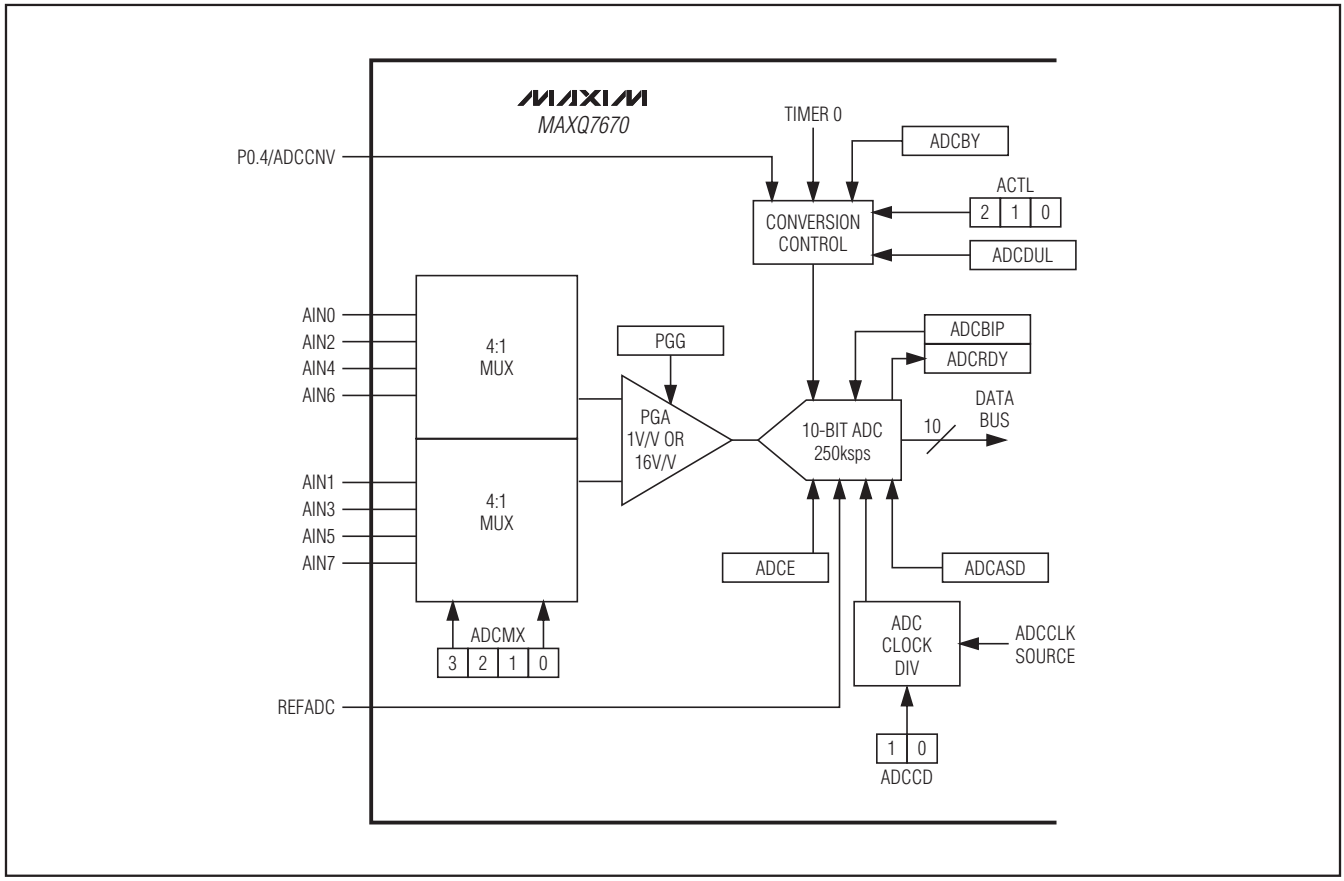


Figure 4. Simplified Analog Input Diagram (Four Fully Differential Inputs)

The MAXQ7670 ADC uses a fully differential SAR conversion technique and an integrated T/H (track and hold) block to convert voltage signals into a 10-bit digital result. Both single-ended and differential configurations are implemented using an analog input channel multiplexer that supports 8 single-ended or 4 differential channels.

In single-ended mode, the mux selects from either of the ground-referenced analog inputs AIN0–AIN7. In differential input configuration, analog inputs are selected from the following pairs: AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, and AIN6/AIN7. Table 1 shows the single-ended and differential input configurations possible for the ADC mux.

Analog Input Track and Hold

A SAR conversion in the MAXQ7670 has different T/H cycles depending on whether a gain of 1 (bypass) or a gain of 16 (PGA enabled) is selected.

Gain = 1V/V

In gain = 1V/V, the conversion has a two-stage T/H cycle. In track mode, a positive input capacitor connects to the signal channel. A negative input capacitor connects to the reference channel. After the T/H enters hold mode, the difference between the signal and the reference channel is converted to a 10-bit value. This two-stage cycle takes 16 SARCLKs to complete.

Gain = 16V/V

In gain = 16V/V, the conversion has a three-stage T/H cycle: amplification, ADC track, and ADC hold. First, the PGA tracks the selected input and reference signals. The PGA amplifies the difference between the two signals and holds the result for the next stage, ADC track. The ADC tracks and converts the PGA result into a 10-bit value. The SAR operation itself does not change irrespective of the chosen gain. This three-stage cycle takes 26.5 SARCLKs to complete. Figure 5 shows the conversion timing differences between gain = 1V/V and gain = 16V/V.

Table 1. ADC Mux Input Configurations

SAR CHANNEL SELECT (REGISTER ACNT[14:11])	SIGNAL CHANNEL INTO ADC	REFERENCE CHANNEL INTO ADC	MEASUREMENT TYPE
0000	AIN0	AGND	Single-ended measurement on AIN0
0001	AIN1	AGND	Single-ended measurement on AIN1
0010	AIN2	AGND	Single-ended measurement on AIN2
0011	AIN3	AGND	Single-ended measurement on AIN3
0100	AIN4	AGND	Single-ended measurement on AIN4
0101	AIN5	AGND	Single-ended measurement on AIN5
0110	AIN6	AGND	Single-ended measurement on AIN6
0111	AIN7	AGND	Single-ended measurement on AIN7
1000	—	—	Reserved
1001	—	—	Reserved
1010	AIN0	AIN1	AIN0/AIN1
1011	AIN2	AIN3	AIN2/AIN3
1100	AIN4	AIN5	AIN4/AIN5
1101	AIN6	AIN7	AIN6/AIN7
1110	—	—	Reserved
1111	—	—	VCIM differential zero offset trim

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

System Clock Generator

The MAXQ7670 oscillator module provides the master clock generator that supplies the system clock for the µC core and all of the peripheral modules. The high-frequency oscillator operates with an 8MHz or 16MHz crystal. Alternatively, use the integrated RC oscillator in applications that do not require precise timing. The MAXQ7670 executes most instructions in a single SYSCLK period. The oscillator module contains all of the primary clock generation circuitry. Figure 7 shows a block diagram of the system clock module.

The MAXQ7670 contains the following features for generating its master clock signal timing source:

- Internal, fast-starting, 15MHz RC oscillator eliminates external crystal
- Internal high-frequency oscillator that can drive an external 8MHz or 16MHz crystal
- External high-frequency 0.166MHz to 16MHz clock input
- Power-up timer
- Power-saving management modes
- Fail-safe modes

Watchdog Timer

The primary function of the watchdog timer is to supervise software execution, watching for stalled or stuck software. The watchdog timer performs a controlled system restart when the µC fails to write to the watchdog timer register before a selectable timeout interval expires. A watchdog timer typically has four objectives:

1) To detect if a system is operating normally
2) To detect an infinite loop in any of the tasks
3) To detect an arbitration deadlock involving two or more tasks
4) To detect if some lower priority tasks are not getting to run because of higher priority tasks

As illustrated in Figure 8, the internal RC oscillator (CLK_RC) drives the watchdog timer through a series of dividers. The programmable divider output determines the timeout interval. When enabled, the interrupt flag WDIF sets. A system reset occurs after a time delay (based on the divider ratio) unless an interrupt service routine clears the watchdog interrupt.

The watchdog timer functions as the source of both the watchdog interrupt and the watchdog reset. The interrupt timeout has a default divide ratio of 2^{12} of the CLK_RC, with the watchdog reset set to timeout 2^9 clock cycles later. With the nominal RC oscillator value of 15MHz, an interrupt timeout occurs every 0.273ms, followed by a watchdog reset 34µs later. The watchdog timer resets to the default divide ratio following any reset event. Use the WD0 and WD1 bits in the WDCN register to increase the watchdog interrupt period. Changing the WD[1:0] bits before a watchdog interrupt timeout occurs (i.e. before the watchdog reset counter begins) resets the watchdog timer count. The watchdog reset timeout occurs 512 RC oscillator cycles after the watchdog interrupt timeout. For more information on the MAXQ7670 watchdog timer, refer to the *MAXQ7670 User's Guide.*

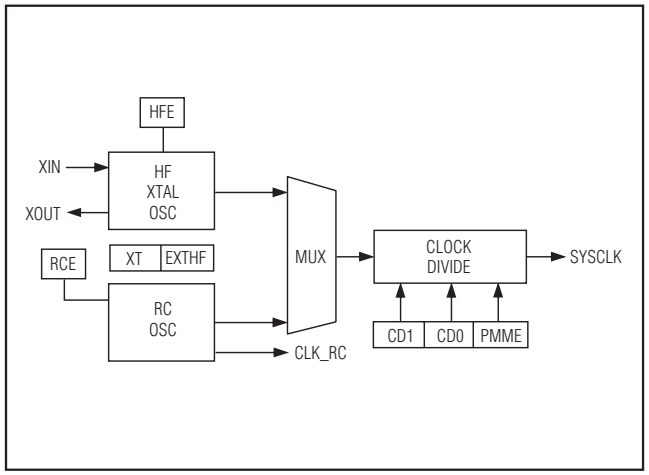


Figure 7. High-Frequency and RC Oscillator Functional Diagram

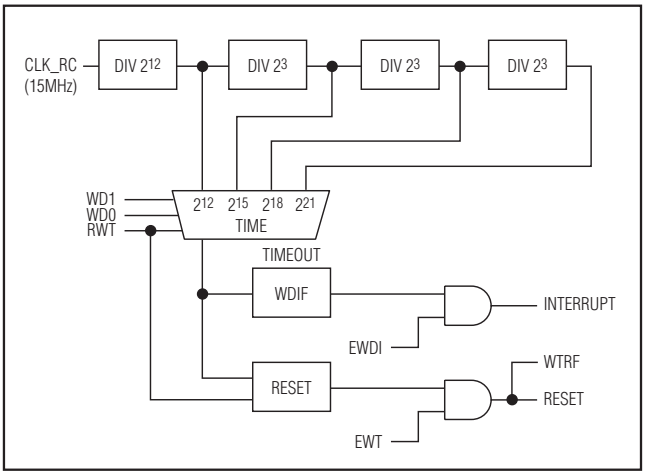


Figure 8. Watchdog Functional Diagram

Timer and PWM

The MAXQ7670 includes a 16-bit timer channel. The timer offers two ports, T0 and T0B, to facilitate PWM outputs, and capture timing events. The autoreload 16-bit timer/counter offers the following functions:

- 8-/16-bit timer/counter
- Up/down autoreload
- Counter function of external pulse
- Capture
- Compare
- PWM output
- Event timer
- System supervisor

Refer to the *MAXQ7670 User's Guide* and Application Note 3205: *Using Timers in the MAXQ Family of Microcontrollers* for more information about the timer module.

CAN Interface Bus

The MAXQ7670 incorporates a fully compliant CAN 2.0B controller.

Two groups of registers provide the µC interface to the CAN controller. To simplify the software associated with the operation of the CAN controllers, most of the global CAN status and controls as well as the individual message center control/status registers are located in the peripheral register map. The remaining registers associated with the data identification, identification masks, format, and data are located in a dual port memory to allow the CAN controller and the processor access to the required functions. The CAN controller can directly access the dual port memory. The processor accesses the dual port memory through a dedicated interface that consists of the CAN 0 data pointer (C0DP) and the CAN 0 data buffer (C0DB) special function registers. See Figure 9 for CAN controller details.

CAN Functional Description

The CAN module stores up to 15 messages. Each message consists of an acceptance identifier and 8 bytes of data. The MAXQ7670 supports both the standard 11-bit and extended 29-bit identification modes.

Configure each of the first 14 message centers either to transmit or receive. Message center 15 is a receive-only center, storing any message that centers 1–14 do not accept.

A message center only accepts an incoming message if the following conditions are satisfied:

- The incoming message's arbitration value matches the message center's acceptance identifier
- The first 2 data bytes of the incoming message match the bytes in the media arbitration registers (C0MA0 and C0MA1)

Use the global mask registers to mask out bits in the incoming message that do not require a comparison.

A message center, configured to transmit, meets these conditions: T/R = 1, TIH = 0, DTUP = 1, MSRDY = 1, and MTRQ = 1. The message center transmits its contents when it receives an incoming request message containing the same identifier (i.e., a remote frame).

Global control and status registers in the CAN unit enable the µC to evaluate error messages, validate and locate new data, establish the bus timing for the CAN bus, establish the identification mask bits, and verify the source of individual messages. In addition, each message center is individually equipped with the necessary status and controls to establish directions, interrupt generation, identification mode (standard or extended), data field size, data status, automatic remote frame request and acknowledgment, and masked or nonmasked identification acceptance testing.

JTAG Interface Bus

The joint test action group (JTAG) IEEE® 1149.1 standard defines a unique method for in-circuit testing and programming. The MAXQ7670 conforms to this standard, implementing an external test access port (TAP) and internal TAP controller for communication with a JTAG bus master, such as an automatic test equipment (ATE). For detailed information on the TAP and TAP controller, refer to IEEE Standard 1149.1 on the IEEE website at www.standards.ieee.org. The JTAG on the MAXQ7670 does not support boundary scan test capability.

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frequency is limited to SYSCLK/2 in master mode and SYSCLK/8 in slave mode. Figure 10 shows the functional diagram of the SPI port. Figures 1 and 2 illustrate the timing parameters listed in the *Electrical Characteristics* table.

General-Purpose Digital I/Os

The MAXQ7670 provides seven general-purpose digital I/Os (GPIOs). Some of the GPIOs include an additional special function (SF), such as a timer input/output. For example, the state of P0.6/T0 is programmable to depend on timer channel 0 logic. When used as a port, each I/O is configurable for high-impedance, weak pullup to DVDDIO or pulldown to GNDIO. At power-up, each GPIO is configured as an input with a pullup to DVDDIO. In addition, each GPIO can be programmed to cause an interrupt (on falling or rising edges). In stop mode, use any interrupt to wake-up the device.

The port direction (PD) register determines the input/output direction of each I/O. The port output (PO) register contains the current state of the logic output buffers. When an I/O is configured as an output, writing to the PO register controls the output logic state. Reading the PO register shows the current state of the output buffers, independent of the data direction. The port input (PI) register is a read-only register that always reflects the logic state of the I/Os.

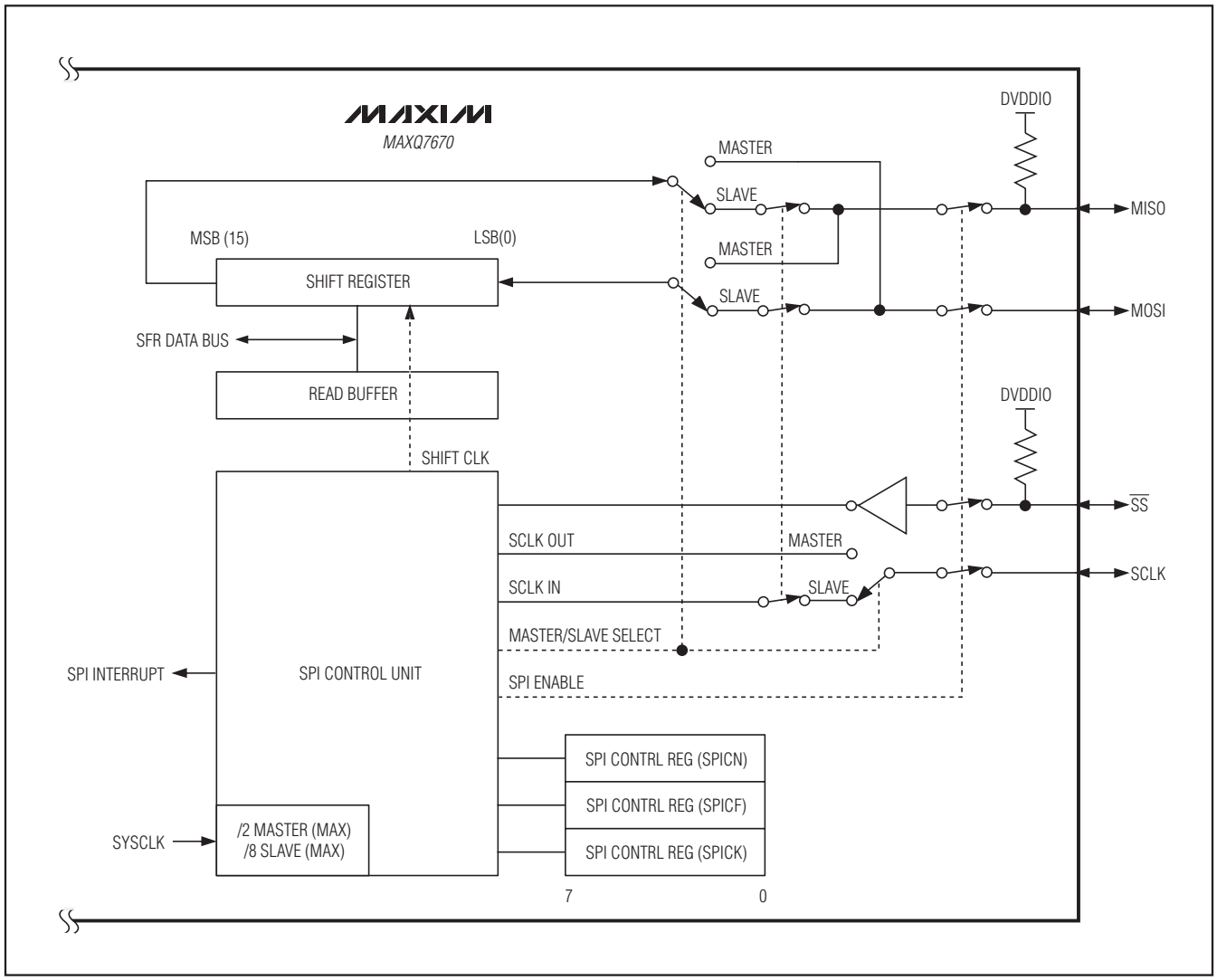

Figure 10. SPI Functional Diagram

Power Management

Advanced power-management features minimize power consumption by dynamically matching the processing speed of the device to the required performance level. During periods of reduced activity, lower the system clock speed to reduce power consumption. Use the source-clock-divide feature to reduce the system clock speed to 1/2, 1/4, and 1/8 of the source clock's speed. A lower power state is thus achievable without additional hardware. For extremely power-sensitive applications, two additional low-power modes are available:

- PMM: divide-by-256 power-management mode (PMME = 1)
- Stop mode (STOP = 1)

Enabling PMM reduces the system clock speed to 1/256 of the source clock speed, and significantly reduces power consumption. The optional switchback feature allows enabled interrupt sources including external, CAN, and SPI interrupts to bring the µC out of the power-management mode and to run at a faster system clock speed.

Power consumption is minimal in stop mode. In this mode, the external oscillator, internal RC oscillator, system clock, and all processing activity stop. Triggering an enabled external interrupt or applying an external reset signal to $\overline{\text{RESET}}$ brings the µC out of stop mode. Upon exiting stop mode, the µC can either wait for the external crystal to warm up, or execute immediately by using the internal RC oscillator as the crystal warms up.

Interrupts

Multiple interrupt sources are available for quick response to internal and external events. Examples of events that can trigger an interrupt are:

- Watchdog interrupt
- GPIO0–GPIO7 interrupts
- SPI mode fault, write collision, receive overrun, and transfer complete interrupts
- Timer 0 low compare, low overflow, capture/compare, and overflow interrupts
- CAN0 receive and transmit interrupts and a change in CAN0 status register interrupt
- ADC data ready interrupt
- Voltage brownout interrupts
- Crystal oscillator failure interrupt

Each interrupt has flag and enable bits. The flag indicates whether an interrupt event has occurred. Enable the µC to generate an interrupt by setting the enable bit. Interrupts are organized into modules. Enable the interrupt individually, by module, and globally.

The µC jumps to an ISR after an enabled interrupt event occurs. Use the interrupt identification register (IIR) to determine whether the interrupt is a system or peripheral interrupt. In the ISR, clear the interrupt flag to eliminate repeated interrupts from the same event. After clearing the interrupt, allow a delay before issuing the return from interrupt (RETI) instruction. Asynchronous interrupt flags require a one-instruction delay and synchronous interrupt flags require a two-instruction delay.

The MAXQ architecture uses a single interrupt vector (IV) and single ISR design. The IV register holds the address of the ISR. In the application code, assign a unique address to each ISR. Otherwise, the IV automatically jumps to 0000h, the beginning of application code, after an enabled interrupt occurs.

Reset Sources

Reset sources are provided for µC control. Although code execution stops in the reset state, the internal RC oscillator continues to oscillate. Internal resets, such as the power-on and watchdog resets, pull $\overline{\text{RESET}}$ low.

Power-On Reset (POR)

An internal POR circuit enhances system reliability. The POR circuit forces the device to perform a POR whenever a rising voltage on DVDD climbs above the POR threshold. At this point the following events occur:

- All registers and circuits enter the default state
- The POR flag (WDCN.7) sets to indicate if the source of the reset was a loss of power
- The internal 15MHz RC oscillator becomes the clock source
- Code execution begins at location 8000h

Refer to the *MAXQ7670 User's Guide* for more information.

Watchdog Timer Reset

The watchdog timer functions are described in the *MAXQ7670 User's Guide*. Execution resumes at location 8000h following a watchdog timer reset.

External System Reset

Pulling $\overline{\text{RESET}}$ low externally causes the device to enter the reset state. The external reset functions as described in the *MAXQ7670 User's Guide*. Execution resumes at location 8000h after $\overline{\text{RESET}}$ is released.

Table 3. System Register Bit and Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AP									—	—	—	—	AP (4 Bits)			
									0	0	0	0	0	0	0	0
APC									CLR	IDS	—	—	—	MOD2	MOD1	MOD0
									0	0	0	0	0	0	0	0
PSF									Z	S	—	GPF1	GPF0	OV	C	E
									1	0	0	0	0	0	0	0
IC									—	—	CGDS	—	—	—	INS	IGE
									0	0	0	0	0	0	0	0
IMR									IMS	—	IM5	IM4	IM3	IM2	IM1	IM0
									0	0	0	0	0	0	0	0
SC									TAP	—	CDA1	CDA0	UPA	ROD	PWL	—
									1	0	0	0	0	0	s*	0
IIR									IIS	—	II5	II4	II3	II2	II1	II0
									0	0	0	0	0	0	0	0
CKCN									XT	—	RGMD	STOP	SWB	PMME	CD1	CD0
									s*	0	s*	0	0	0	0	1
WDCN									POR	EWDI	WD1	WD0	WDIF	WTRF	EWT	RWT
									s*	s*	0	0	0	s*	s*	0
A[n] (0..15)	A[n] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PFX[n] (0..15)	PFX[n] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IP	IP (16 Bits)															
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SP	—	—	—	—	—	—	—	—	—	—	—	—	SP (4 Bits)			
	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
IV	IV (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[0]	LC[0] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[1]	LC[1] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OFFS									OFFS (8 Bits)							
									0	0	0	0	0	0	0	0
DPC	—	—	—	—	—	—	—	—	—	—	—	WBS2	WBS1	WBS0	SDPS1	SDPS0
	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
GR	GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRL									GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
									0	0	0	0	0	0	0	0
BP	BP (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRS	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0	GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRH									GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
									0	0	0	0	0	0	0	0
GRXL	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FP	FP (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP[0]	DP[0] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP[1]	DP[1] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

*Bits indicated by an "s" are only affected by a POR and not by other forms of reset. These bits are set to 0 after a POR. Refer to the *MAXQ7670 User's Guide* for more information.

Table 5. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM	—	—	—	—	CRTMS	CRTM	TESTCAN	—	DCW	FTEST	DOFF	—	SRT	—	SCANMODE	TME
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0C	—	—	—	—	—	—	—	—	ERIE	STIE	PDE	SIESTA	CRST	AUTOB	ERCS	SWINT
	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
C0S	—	—	—	—	—	—	—	—	BSS	EC96/128	WKS	RXS	TXS	ER2	ER1	ER0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0IR	—	—	—	—	—	—	—	—	INTIN7	INTIN6	INTIN5	INTIN4	INTIN3	INTIN2	INTIN1	INTIN0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0TE	—	—	—	—	—	—	—	—	C0TE.7	C0TE.6	C0TE.5	C0TE.4	C0TE.3	C0TE.2	C0TE.1	C0TE.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0RE	—	—	—	—	—	—	—	—	C0RE.7	C0RE.6	C0RE.5	C0RE.4	C0RE.3	C0RE.2	C0RE.1	C0RE.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0R	—	—	—	—	—	—	—	—	CAN0BA	INCDEC	AID	C0BPR7	C0BPR6	—	C0BIE	C0IE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0DP	C0DP.15	C0DP.14	C0DP.13	C0DP.12	C0DP.11	C0DP.10	C0DP.9	C0DP.8	C0DP.7	C0DP.6	C0DP.5	C0DP.4	C0DP.3	C0DP.2	C0DP.1	C0DP.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0DB	C0DB.15	C0DB.14	C0DB.13	C0DB.12	C0DB.11	C0DB.10	C0DB.9	C0DB.8	C0DB.7	C0DB.6	C0DB.5	C0DB.4	C0DB.3	C0DB.2	C0DB.1	C0DB.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0RMS	—	C0RMS.15	C0RMS.14	C0RMS.13	C0RMS.12	C0RMS.11	C0RMS.10	C0RMS.9	C0RMS.8	C0RMS.7	C0RMS.6	C0RMS.5	C0RMS.4	C0RMS.3	C0RMS.2	C0RMS.1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0TMA	—	C0TMA.15	C0TMA.14	C0TMA.13	C0TMA.12	C0TMA.11	C0TMA.10	C0TMA.9	C0TMA.8	C0TMA.7	C0TMA.6	C0TMA.5	C0TMA.4	C0TMA.3	C0TMA.2	C0TMA.1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M1C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M2C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M3C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M4C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M5C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M6C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M7C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M8C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M9C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M10C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M11C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M12C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Microcontroller with 10-Bit ADC, PGA, 64KB Flash, and CAN Interface

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/08	Initial release	—
1	7/09	Updated *Ordering Information* to indicate automotive qualified part	1