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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, I²C, QSPI, SDHC, SPI, UART/USART, USB
Peripherals	DMA, I²S, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16b SAR; D/A 2x6b, 1x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	210-UFBGA, WLCSP
Supplier Device Package	210-WLCSP (6.94x6.94)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk28fn2m0acau15r

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Symbol	Description	Min.	Max.	Unit
V_{DD_CORE}[1]	Internal digital logic supply voltage	– 0.3	1.47	V
V_{DD}	Digital supply voltage for Ports A, B,C,D	–0.3	3.8	V
V_{DDA}	Analog supply voltage	– 0.3	3.8	V
V_{DDIO_E}	V_{DDIO_E} is an independent voltage supply for PORTE [2]	–0.3	3.8	V
V_{BAT}	RTC supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
I_D	Maximum current single pin limit (digital output pins)	–25	25	mA
V_{REGIN}	USB regulator input	–0.3	6.0	V
V_{USB0_Dx}	USB0_DP and USB_DM input voltage	–0.3	3.63	V
V_{USB1_DPx}	USB1_DP and USB1_DM input voltage	–0.3	3.63	V

1. V_{DD_CORE} must not exceed V_{DD} on power up or power down
2. V_{DDIO_E} is independent of the V_{DD} domain and can operate at a voltage independent of V_{DD}.

1.4.1 Recommended Power-On-Reset (POR) Sequencing

- V_{DD}/V_{DDIO_E} and V_{DD_CORE}

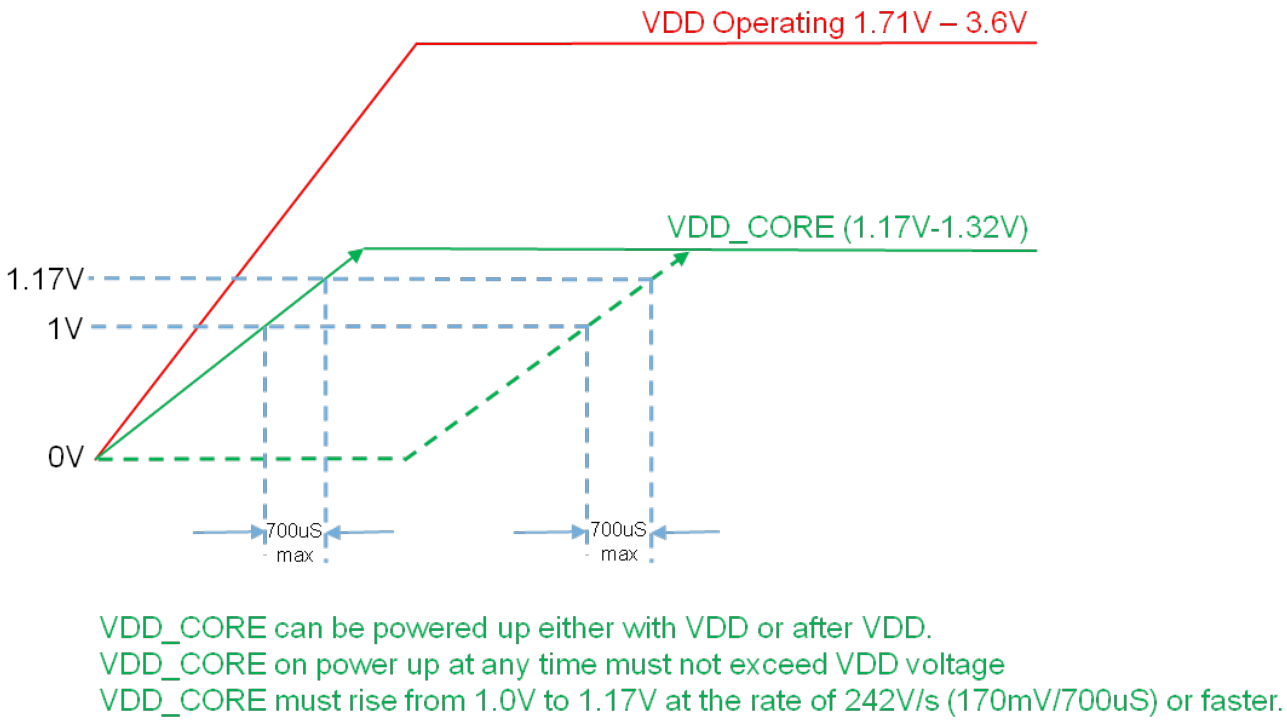

Figure 2. V_{DD_CORE}/ V_{DD} Powering sequence

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• VLLS2 –> RUN	—	103	µs	
	• VLLS3 –> RUN	—	103	µs	
	• LLS2 –> RUN	—	6.3	µs	
	• LLS3 –> RUN	—	6.3	µs	
	• VLPS –> RUN	—	5.4	µs	
	• STOP –> RUN	—	5.4	µs	

2.2.5 Power consumption operating behaviors

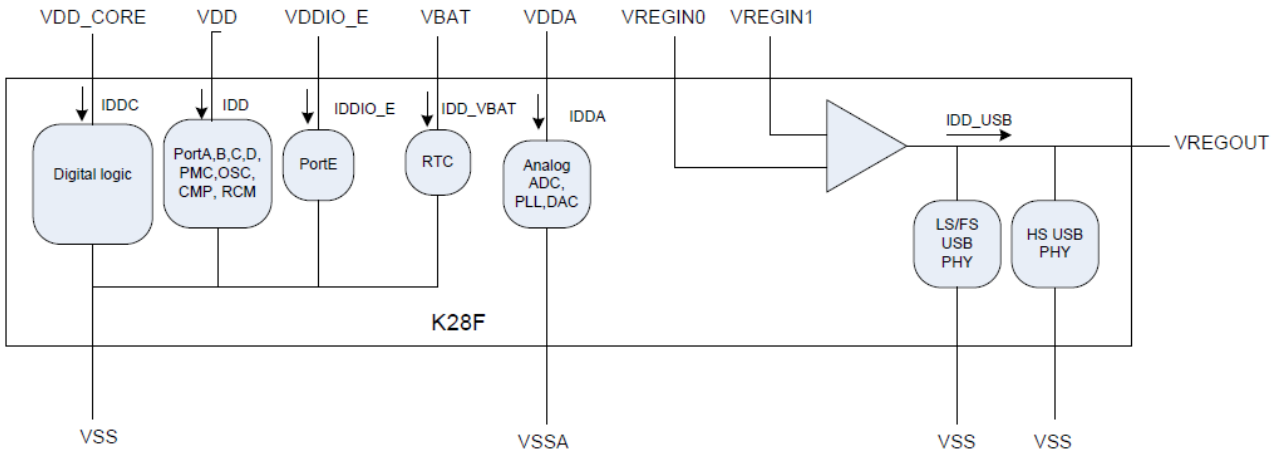

Figure 4. Power Supplies of K28F

The K28F device has several power supplies and the total current consumption of the device is the accumulative result of each individual power supplies' current consumption, dependent on the power mode of operation. (RUN, HSRUN, VLPR, Stop, VLLS3 etc.).

IDD_MCU_total = IDDC + IDD + IDDIO_E + IDD_VBAT + IDDA + IDD_USB

When calculating the total MCU current consumption considerations to external loads on the following should be made:

- On top of the device's IDD current consumption, external loads applied to Ports A,B,C and D need to be considered

Table 6. Power consumption operating behaviors (through VDD_CORE) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDC_VLPS}	Very-low-power stop mode current at 1.2 V					
	• @ 25°C	—	0.452	1.2	mA	
	• @ 70°C	—	2.2	4.9		
	• @ 85°C	—	3.4	7.4		
	• @ 105°C	—	5.8	12.4		
I_{DDC_LLS3}	Low leakage stop mode current at 1.2 V					
	• @ 25°C	—	15.6	30.3	µA	
	• @ 70°C	—	129.0	189.5		
	• @ 85°C	—	244.9	347.8		
	• @ 105°C	—	535.0	737.3		
I_{DDC_LLS2}	Low leakage stop mode current at 1.2 V					8
	• @ 25°C	—	4.3	8.7	µA	
	• @ 70°C	—	33.8	57.3		
	• @ 85°C	—	62.8	104.0		
	• @ 105°C	—	135.6	205.8		
I_{DDC_VLLS3}	Very low-leakage stop mode 3 current at 1.2 V					
	• @ 25°C	—	13.5	26.0	µA	
	• @ 70°C	—	112.1	159.7		
	• @ 85°C	—	212.5	294.7		
	• @ 105°C	—	460.2	621.6		
I_{DDC_VLLS2}	Very low-leakage stop mode 2 current at 1.2 V					8
	• @ 25°C	—	0.552	0.9	µA	
	• @ 70°C	—	6.1	8.2		
	• @ 85°C	—	10.5	14.2		
	• @ 105°C	—	24.7	32.3		
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled @ 3.0 V					
	• @ 25°C	—	0.266	0.319	µA	
	• @ 70°C	—	0.595	0.750		
	• @ 85°C	—	0.933	1.3		
	• @ 105°C	—	2.2	2.8		
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers @ 1.8 V				µA	9

Table 7. Power consumption operating behaviors (through VDD) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 85°C	—	39.6	84.3		
	• @ 105°C	—	63.9	157.5		
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ 25°C	—	159.3	279.3	μA	
	• @ 70°C	—	173.8	341.8		
	• @ 85°C	—	181.4	358.4		
	• @ 105°C	—	251.2	735.0		
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ 25°C	—	3.1	5.6	μA	
	• @ 70°C	—	8.5	12.0		
	• @ 85°C	—	15.2	19.4		
	• @ 105°C	—	36.9	43.9		
I_{DD_LLS3}	Low leakage stop mode current at 3.0 V					
	• @ 25°C	—	2.9	4.7	μA	
	• @ 70°C	—	7.2	9.2		
	• @ 85°C	—	13.2	16.1		
	• @ 105°C	—	33.4	39.4		
I_{DD_LLS2}	Low leakage stop mode current at 3.0 V					7
	• @ 25°C	—	2.9	4.7	μA	
	• @ 70°C	—	7.2	9.2		
	• @ 85°C	—	13.2	16.1		
	• @ 105°C	—	33.4	39.4		
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ 25°C	—	2.2	3.4	μA	
	• @ 70°C	—	4.7	6.4		
	• @ 85°C	—	8.1	10.6		
	• @ 105°C	—	18.8	23.8		
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					7
	• @ 25°C	—	2.2	3.3	μA	
	• @ 70°C	—	4.5	6.1		

Table 7. Power consumption operating behaviors (through VDD)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 85°C	—	7.7	10.0		
	• @ 105°C	—	17.5	22.0		

1. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode.
2. MCG configured for PEE mode.
3. 150 MHz core and system clock, 50 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for PEE mode.
4. 25 MHz core and system clock, 25 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for FEI mode.
5. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. Code executing from flash.
6. MCG configured for BLPE mode.
7. By default, this mode has only 32K of SRAM enabled.

Below table list the current consumption adders for different SRAM configurations from the LLS2/VLLS2 (TYP) IDD values using a 32 KB SRAM retention referenced in Table 6.

Table 8. LLS2/VLLS2 additional Typical IDDC current consumption Adders

RAM array retained		@ 25°C	@ 85°C	@ 105°C	Unit
LLS2	RAM2: 32 KB	0.5	10.8	21.3	µA
	RAM3: 32 KB	0.5	11.0	21.5	µA
	RAM4: 32 KB	0.4	10.7	21.0	µA
	RAM5: 128 KB	1.4	28.1	57.6	µA
	RAM6: 64 KB	0.6	15.2	30.5	µA
	RAM7: 192 KB	2.1	41.1	85.1	µA
	RAM8: 256 KB	2.8	53.0	109.9	µA
	RAM9: 256 KB	2.3	53.5	110.9	µA
VLLS2	RAM2: 32 KB	0.5	9.1	19.7	µA
	RAM3: 32 KB	0.5	8.5	18.0	µA
	RAM4: 32 KB	0.5	8.1	16.8	µA
	RAM5: 128 KB	1.5	26.6	57.1	µA
	RAM6: 64 KB	0.8	12.9	27.1	µA
	RAM7: 192 KB	2.3	40.2	86.6	µA
	RAM8: 256 KB	3.0	52.9	114.3	µA
	RAM9: 256 KB	3.0	53.1	114.8	µA

Table 18. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	• JTAG and CJTAG • Serial Wire Debug	25 12.5	— —	ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	30.6	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	19.0	ns
J12	TCLK low to TDO high-Z	—	17.0	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

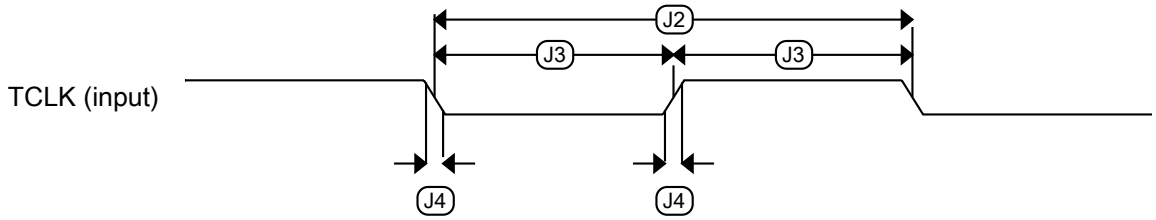

Figure 7. Test clock input timing

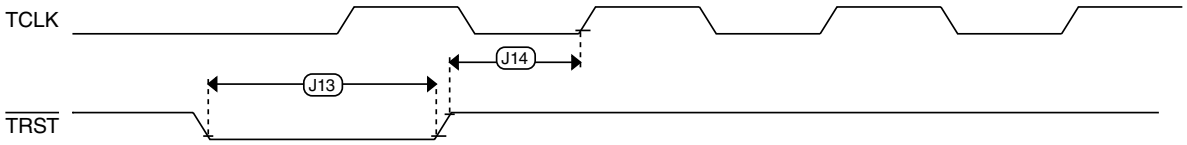

Figure 10. $\overline{\text{TRST}}$ timing

3.2 Clock modules

3.2.1 MCG specifications

Table 19. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
I_{ints}	Internal reference (slow clock) current	—	20	—	µA	
$t_{irefsts}$	[O:] Internal reference (slow clock) startup time	—	32	—	µs	
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	±1	± 2	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.5	± 1	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
I_{intf}	Internal reference (fast clock) current	—	25	—	µA	
$t_{irefsts}$	[L:] Internal reference startup time (fast clock)	—	10	15	µs	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00 ext clk freq: above (3/5)f_{int} never reset	(3/5) x f_{ints_t}	—	—	kHz	

Table continues on the next page...

2. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.2.4 32 kHz oscillator electrical characteristics

3.2.4.1 32 kHz oscillator DC electrical specifications

Table 23. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.2.4.2 32 kHz oscillator frequency specifications

Table 24. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

3.3 Memories and memory interfaces

3.3.1 QuadSPI AC specifications

- All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing diagrams in this section.
- Measurements are with a load of 15 pf (1.8 V) and 35 pf (3 V) on output pins. Input slew: 1 ns
- Timings assume a setting of 0x0000_000x for QuadSPI _SMPR register (see the reference manual for details).

The following table lists the QuadSPI delay chain read/write settings. Refer the device reference manual for register and bit descriptions.

Table 25. QuadSPI delay chain read/write settings

Mode	QuadSPI registers				Notes
	QuadSPI_MCR[DQS_EN]	QuadSPI_SOCCR[SOCCFG]	QuadSPI_MCR[SCLKCFG]	QuadSPI_FLSHCR[TDH]	
SDR	Yes	3Fh	5	No	Delay of 63 buffer and 64 mux
DDR	Yes	3Fh	1	2	Delay of 63 buffer and 64 mux
Hyperflash	RDS driven from Flash	0h	No	2	Delay of 1 mux

SDR mode

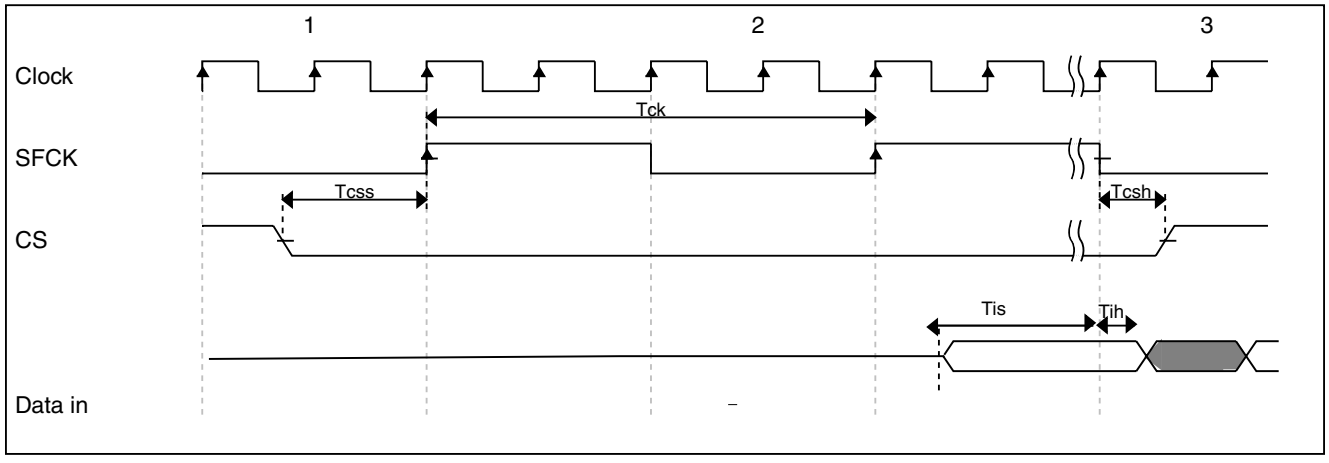

Figure 11. QuadSPI input timing (SDR mode) diagram

NOTE

- The below timing values are with default settings for sampling registers like QuadSPI_SMPR.

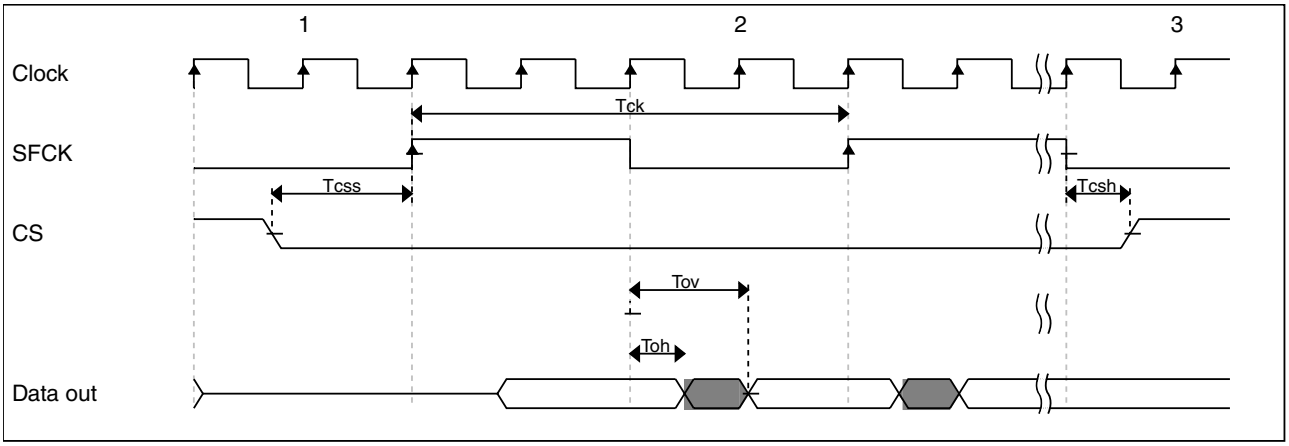

Figure 14. QuadSPI output timing (DDR mode) diagram

Table 29. QuadSPI output timing (DDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	-	4.5	ns
T_{oh}	Output Data Hold	1.5	-	ns
T_{ck}	SCK clock period	-	75 (with learning)	MHz
		-	45 (without learning)	
T_{css}	Chip select output setup time	2	-	Clk(sck)
T_{csh}	Chip select output hold time	-1	-	Clk(sck)

Hyperflash mode

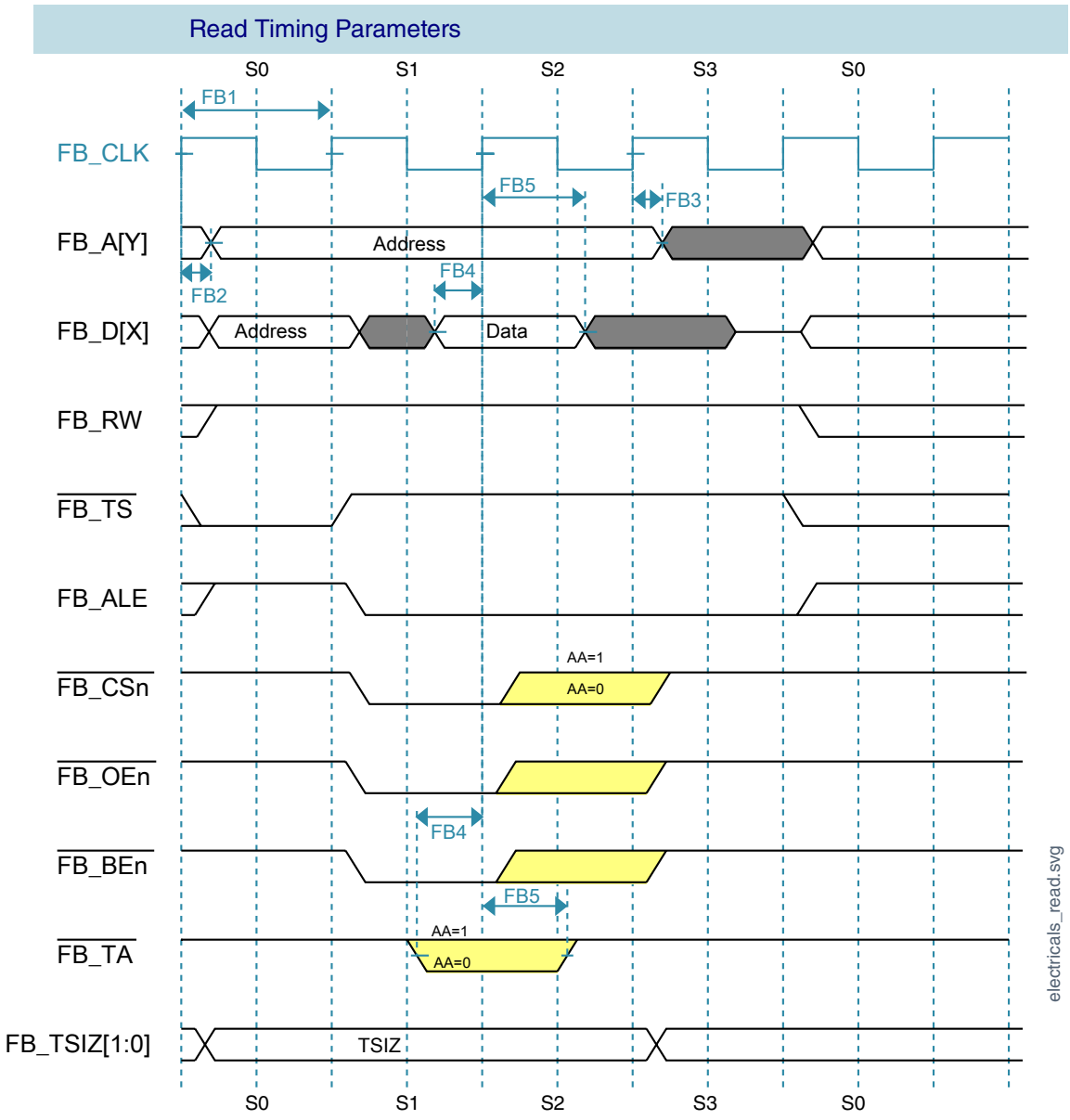

Figure 17. FlexBus read timing diagram

3.4.1.1 ADC operating conditions

Table 40. ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 × VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 8-bit / 10-bit / 12-bit modes	—	4	5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	kS/s	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

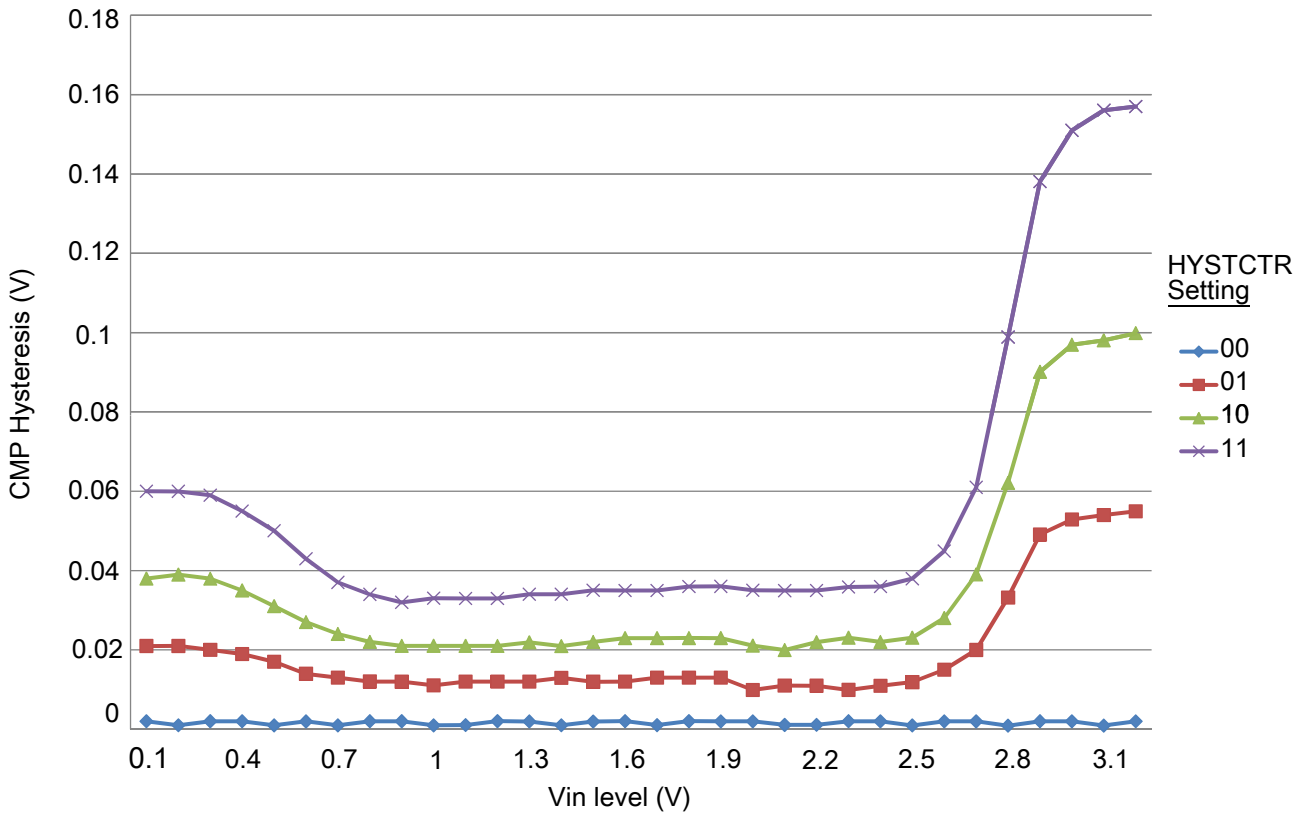

Figure 24. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.4.3 12-bit DAC electrical characteristics

3.4.3.1 12-bit DAC operating requirements

Table 43. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

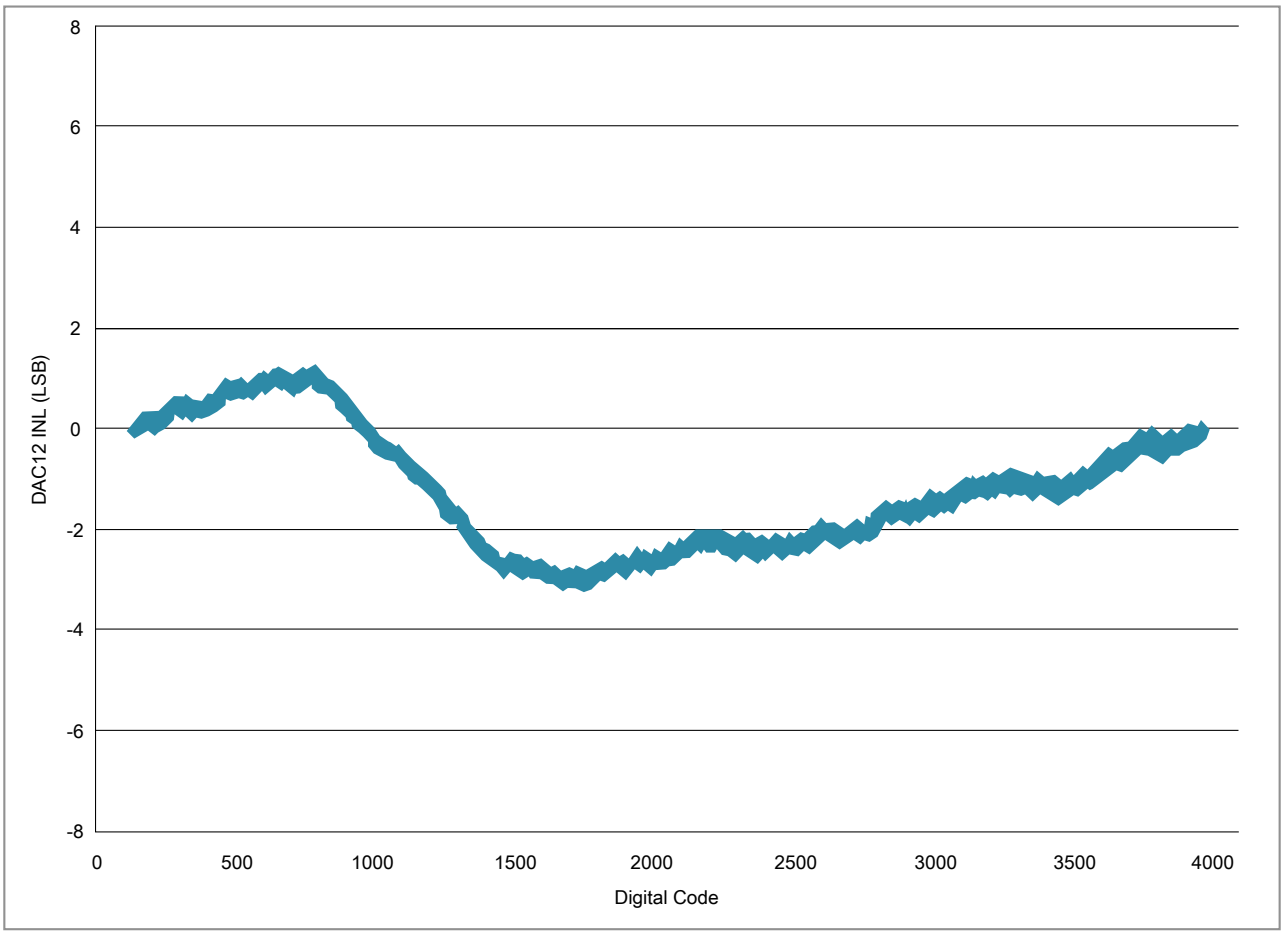

Figure 25. Typical INL error vs. digital code

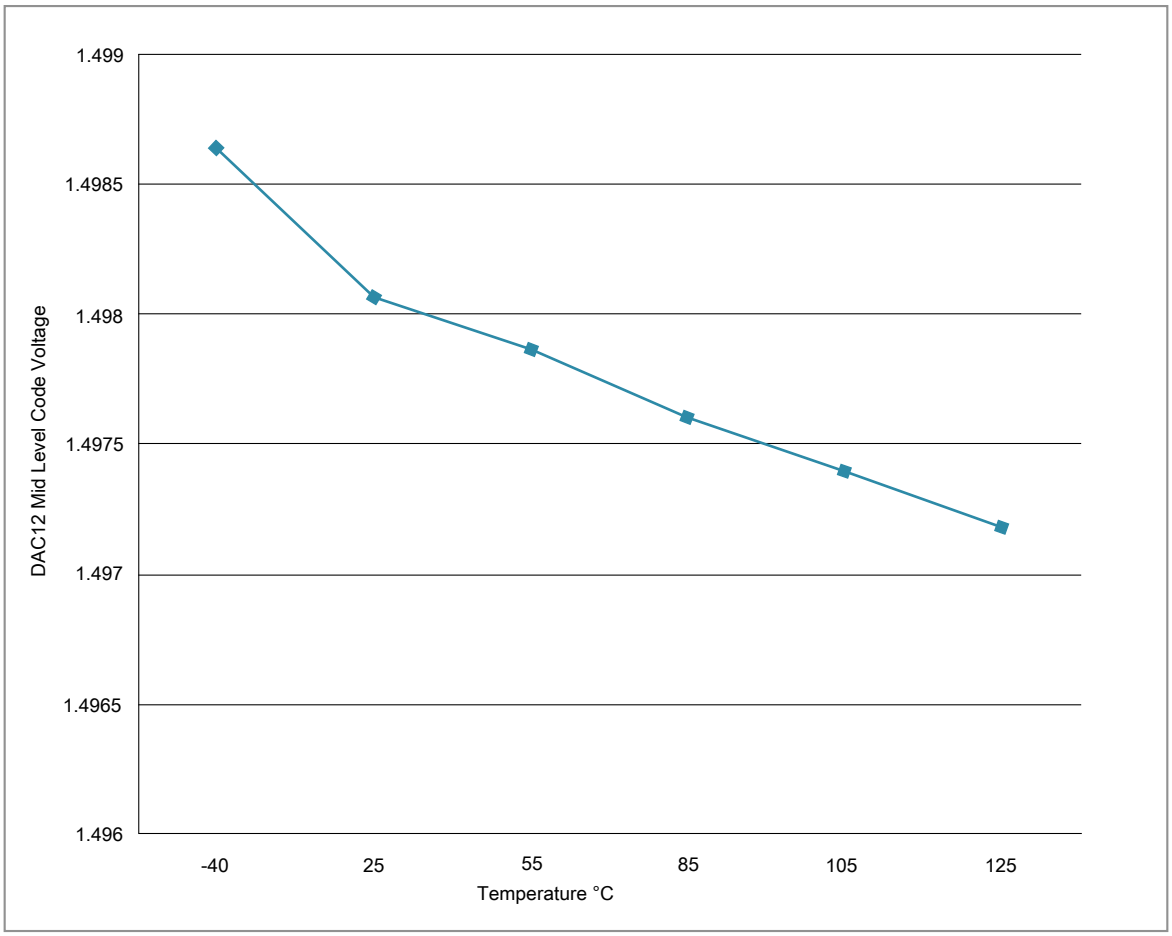

Figure 26. Offset at half scale vs. temperature

3.4.4 Voltage reference electrical specifications

Table 45. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

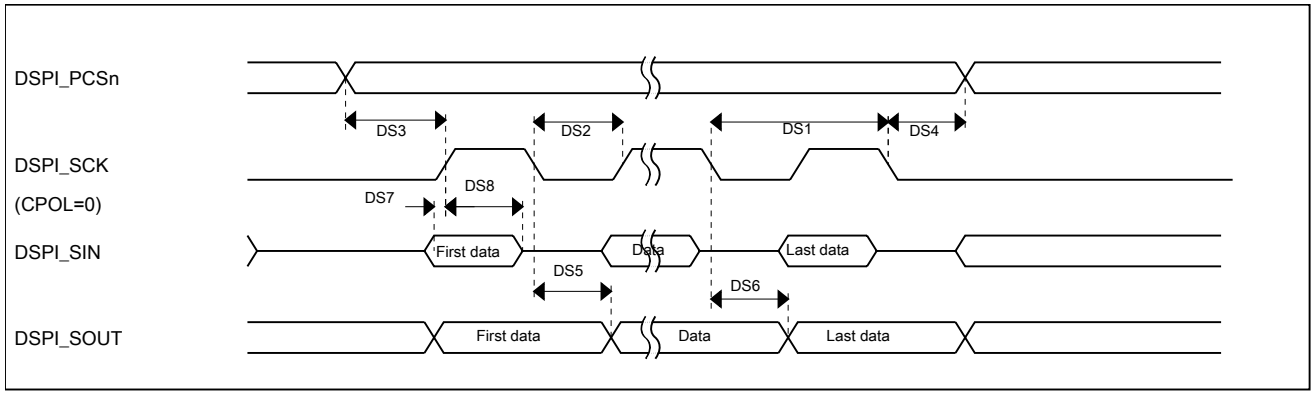

Figure 27. DSPI classic SPI timing — master mode

Table 52. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation	—	15 [1]	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	23.0	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.7	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	13	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	13	ns

1. The maximum operating frequency is measured with non-continuous CS and SCK. When DSPI is configured with continuous CS and SCK, there is a constraint that SPI clock should not be greater than 1/6 of bus clock, for example, when bus clock is 60MHz, SPI clock should not be greater than 10MHz.

Table 60. I²C 1 Mbps timing (continued)

Characteristic	Symbol	Minimum	Maximum	Unit
Set-up time for STOP condition	t_{SU}; STO	0.26	—	µs
Bus free time between STOP and START condition	t_{BUF}	0.5	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

1. The maximum SCL clock frequency of 1 Mbps can support maximum bus loading when using the High drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

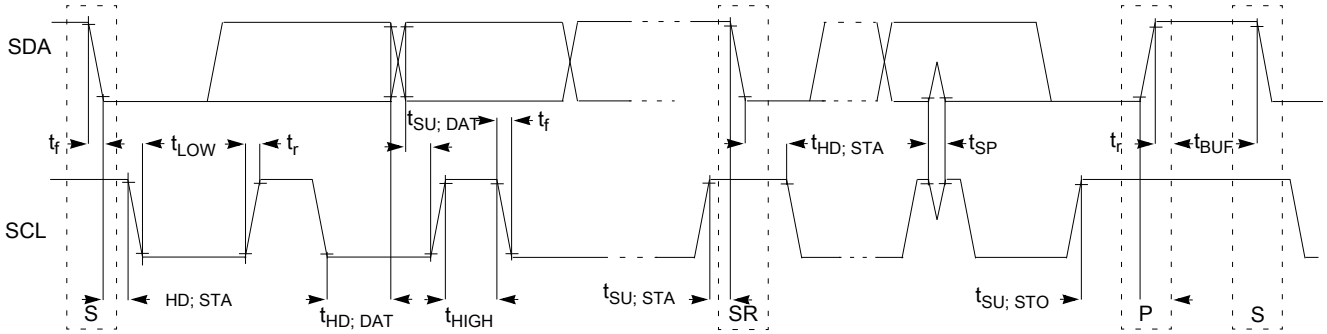

Figure 31. Timing definition for devices on the I²C bus

3.6.7 LPUART switching specifications

See General switching specifications.

3.6.8 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 61. SDHC full voltage range switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
		Card input clock			
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25/45	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	25/45	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz

Table continues on the next page...

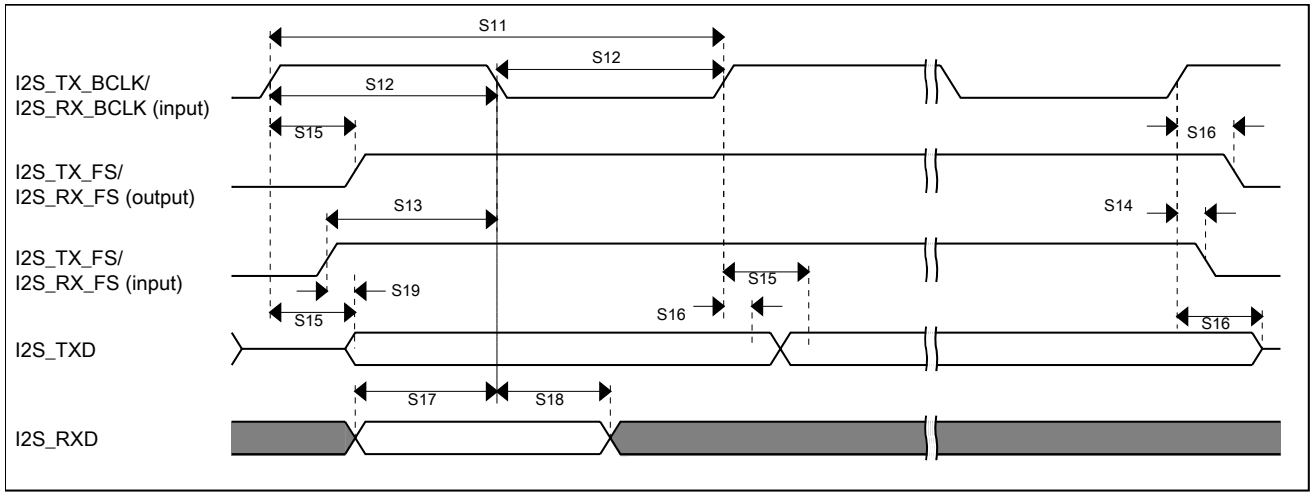

Figure 38. I2S/SAI timing — slave modes

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
169-pin MAPBGA	98ASA00628D
210-pin WLCSP	98ASA01002D

For additional packaging assembly information on MAPBGA, refer to applications note AN4982.

For additional packaging assembly information on WLCSP, refer to applications note AN3846.

5 Pinout

Table 69. Recommended connection for unused analog interfaces (continued)

Pin Type	K28F	Short recommendation	Detailed recommendation
USB	USB0_DM	Float	Float
USB	VREG_OUT	Tie to input and ground through 10 kΩ	Tie to input and ground through 10 kΩ
USB	VREG_IN0	Tie to output and ground through 10 kΩ	Tie to output and ground through 10 kΩ
USB	VREG_IN1	Tie to output and ground through 10 kΩ	Tie to output and ground through 10 kΩ
USB	USB1VSS	Always connect to VSS	Always connect to VSS
USB	USB1_DP	Float	Float
USB	USB1_DM	Float	Float
USB	USB_VBUS	Float	Float
V_{BAT}	V_{BAT}	Float	Float
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential

5.3 K28F Pinouts

The pinout diagrams are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the respective package tab.

Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

6 Ordering parts