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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, I²C, QSPI, SDHC, SPI, UART/USART, USB
Peripherals	DMA, I²S, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16b SAR; D/A 2x6b, 1x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-MAPBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk28fn2m0avmi15

Security

- Hardware random-number generator
- Memory Mapped Crypto Acceleration Unit(MMCAU): DES, 3-DES, AES, SHA-1, SHA-256 and MD5 accelerator
- Cyclic Redundancy Check (CRC)

Target Applications

- Wearables
- Low-end graphic display system
- Cost-optimized multi-standard wireless smart home hubs
- Home Automation devices
- Consumer accessories

- Main V_{DD} Voltage and Flash write voltage range:1.71 V–3.6 V
- V_{DD_CORE}: 1.17 V–1.47 V
- Independent V_{DDIO_E} (QuadSPI):1.71 V–3.6 V
- Independent V_{BAT} (RTC): 1.71 V–3.6 V
- I/O Voltage range (V_{DD}): 1.71 V–3.6 V

Communication interfaces

- Two USB controllers:Crystal-less Full-/low-speed + transceiver Host and Device; High-/Full-/low-speed + PHY Host and Device
- Secure Digital Host Controller (SDHC)
- Two I2S modules, four I2C modules and five Low-Power UART modules
- Four SPI modules (SPI3 supports more than 40 Mbps)
- 32-ch Programmable module (FlexIO) to emulate various serial, parallel or custom interfaces

Ordering Information 1

Part Number	Embedded Memory		Package Type	Maximum number of I\O's
	Flash	SRAM		
MK28FN2M0VMI15	2 MB	1 MB	169 MAPBGA	120
MK28FN2M0CAU15R	2 MB	1 MB	210 WLCSP	120

1. To confirm current availability of orderable part numbers, go to http://www.nxp.com and perform a part number search.

Device Revision Number

Device Mask Set Number	SIM_SDID[REVID]	JTAG ID Register[PRN]
2N96T	0010	0010

Related Resources

Type	Description	Resource
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	K2x Fact Sheet
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K28P210M150SF5RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_K_2N96T[1]
Package drawing	Package dimensions are provided in package drawings.	• MAPBGA 169-pin: 98ASA00628D[1] • WLCSP 210-pin: 98ASA01002D [1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level (for V-temp variant)	—	3	—	1
MSL	Moisture sensitivity level (for C-temp variant)	—	1	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current maximum ratings

Symbol	Description	Min.	Max.	Unit
V_{DD_CORE}[1]	Internal digital logic supply voltage	– 0.3	1.47	V
V_{DD}	Digital supply voltage for Ports A, B,C,D	–0.3	3.8	V
V_{DDA}	Analog supply voltage	– 0.3	3.8	V
V_{DDIO_E}	V_{DDIO_E} is an independent voltage supply for PORTE [2]	–0.3	3.8	V
V_{BAT}	RTC supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
I_D	Maximum current single pin limit (digital output pins)	–25	25	mA
V_{REGIN}	USB regulator input	–0.3	6.0	V
V_{USB0_Dx}	USB0_DP and USB_DM input voltage	–0.3	3.63	V
V_{USB1_DPx}	USB1_DP and USB1_DM input voltage	–0.3	3.63	V

1. V_{DD_CORE} must not exceed V_{DD} on power up or power down
2. V_{DDIO_E} is independent of the V_{DD} domain and can operate at a voltage independent of V_{DD}.

1.4.1 Recommended Power-On-Reset (POR) Sequencing

- V_{DD}/V_{DDIO_E} and V_{DD_CORE}

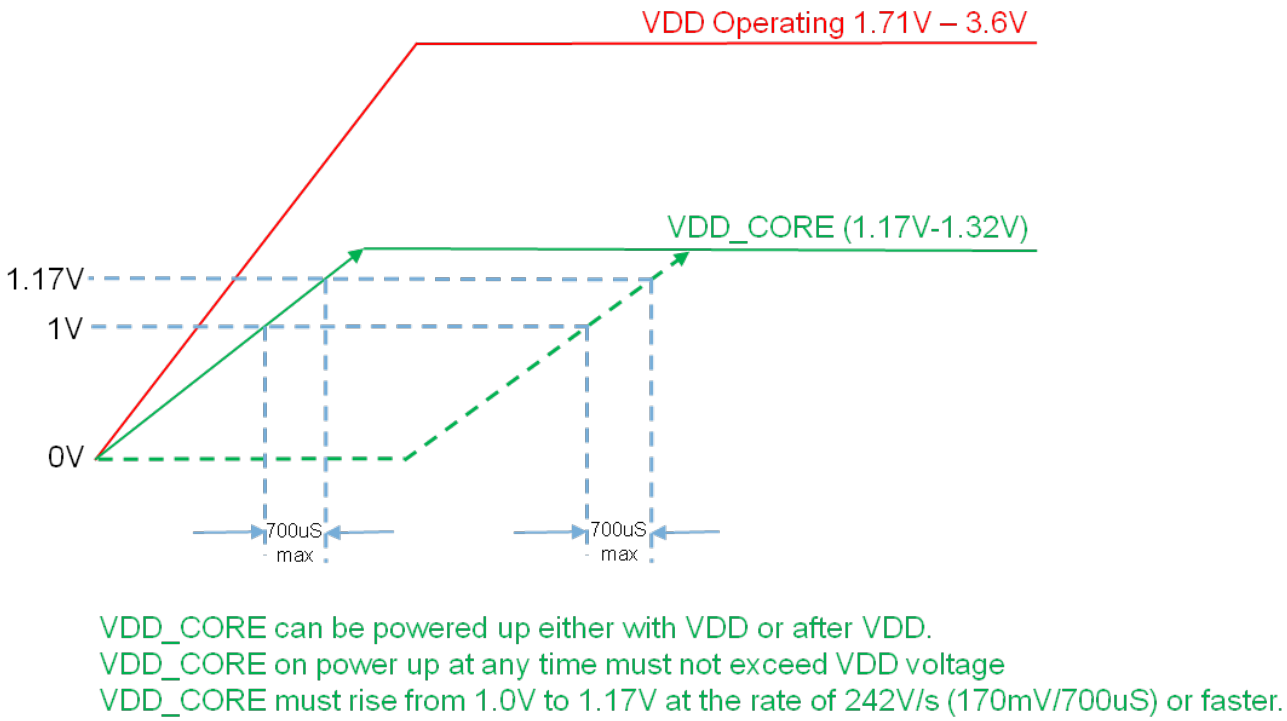

Figure 2. V_{DD_CORE}/ V_{DD} Powering sequence

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	V_{DD} domain pins • $V_{SS} \le V_{IN} \le V_{DD}$	— —	0.002 0.002	0.5 0.5	µA µA	
	PORTE pins • $V_{SS} \le V_{IN} \le V_{DDIO\_E}$	—	0.002	0.5	µA	
	V_{BAT} domain pins • $V_{SS} \le V_{IN} \le V_{BAT}$					
R_{PU}	Internal pullup resistors(except RTC_WAKEUP pins)	20	—	50	kΩ	9
R_{PD}	Internal pulldown resistors (except RTC_WAKEUP pins)	20	—	50	kΩ	10

1. Typical values characterized at 25°C and V_{DD} = 3.6V unless otherwise noted.
2. IO Group 1 includes V_{BAT} domain pins: RTC_WAKEUP_b. IO Group 2 includes V_{DD} domain pins: PORTA, PORTB, PORTC, and PORTD, except PTA4. IO Group 3 includes V_{DD} domain pins: PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7. IO Group 4 includes V_{DDIO_E} domain pins: PORTE.
3. PTA4 has lower drive strength: I_{OH} = -5 mA for high V_{DD} range; I_{OH} = -2.5 mA for low V_{DD} range.
4. Open drain outputs must be pulled to V_{DD}.
5. PTA4 has lower drive strength: I_{OL} = 5mA for high V_{DD} range; I_{OL} = 2.5mA for low V_{DD} range.
6. V_{DD} domain pins include ADC, CMP, and RESET_b inputs. Measured at V_{DD} = 3.6V.
7. PORTE analog input voltages cannot exceed V_{DDIO_E} supply when $V_{DD} \ge V_{DDIO\_E}$. PORTE analog input voltages cannot exceed V_{DD} supply when $V_{DD} < V_{DDIO\_E}$.
8. V_{BAT} domain pins include EXTAL32, XTAL32, and RTC_WAKEUP_b pins.
9. Measured at minimum supply voltage and $V_{IN} = V_{SS}$
10. Measured at minimum supply voltage and $V_{IN} = V_{DD}$

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx –> RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode=FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V and VDD_CORE reaches 1.17 V to execution of the first instruction across the operating temperature range of the chip.	—	1200	µs	

Table continues on the next page...

Table 7. Power consumption operating behaviors (through VDD) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 85°C	—	1.6	1.7		
	• @ 105°C	—	1.6	1.7		
I_{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code of while(1) loop executing from internal flash @ 3.0 V	—	2.0	2.1	mA	3
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
I_{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code of while(1) loop executing from internal flash @ 3.0 V	—	2.0	2.1	mA	3
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
$I_{DD\_HSRUNCO}$	HSRun mode current in compute operation – 150 MHz core/ 25 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0 V				mA	2
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	2.0	2.1	mA	1
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	2.0	2.1	mA	4
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					

Table continues on the next page...

Table 12. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• 1.71 ≤ V_{DD} ≤ 2.7 V • 2.7 ≤ V_{DD} ≤ 3.6 V	—	16	ns	
	• Slew disabled • 1.71 ≤ V_{DD} ≤ 2.7 V • 2.7 ≤ V_{DD} ≤ 3.6 V	— —	7 5	ns ns	
	Port rise and fall time (high drive strength) • Slew enabled • 1.71 ≤ V_{DDIO_E} ≤ 2.7 V • 2.7 ≤ V_{DDIO_E} ≤ 3.6 V • Slew disabled • 1.71 ≤ V_{DDIO_E} ≤ 2.7 V • 2.7 ≤ V_{DDIO_E} ≤ 3.6 V	— — — —	34 16 7 5	ns ns ns ns	5, 8
	Port rise and fall time (low drive strength) • Slew enabled • 1.71 ≤ V_{DDIO_E} ≤ 2.7 V • 2.7 ≤ V_{DDIO_E} ≤ 3.6 V • Slew disabled • 1.71 ≤ V_{DDIO_E} ≤ 2.7 V • 2.7 ≤ V_{DDIO_E} ≤ 3. 6V	— — — —	34 16 7 5	ns ns ns ns	7, 8

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry in run modes.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7.
5. 75 pF load.
6. Ports A, B, C, and D.
7. 25 pF load.
8. Port E pins only.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 13. Thermal operating requirements (for V-Temp range)

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is:

   $T_J = T_A + R\theta_{JA}$ x chip power dissipation

Table 14. Thermal operating requirements (for C-Temp range)

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	95	°C	
T_A	Ambient temperature	–40	85	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is:

   $T_J = T_A + R\theta_{JA}$ x chip power dissipation

2.4.2 Thermal attributes

Table 15. Thermal attributes

Board type	Symbol	Description	210 WLCSP	169 MAPBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	68.5	56.8	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	32.1	27.1	°C/W	1
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52.3	41	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	27.2	22.4	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	16.0	10.4	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.3	7.1	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	0.2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.

3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Debug trace timing specifications

Table 16. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	1.5	—	ns
T_h	Data hold	1.0	—	ns

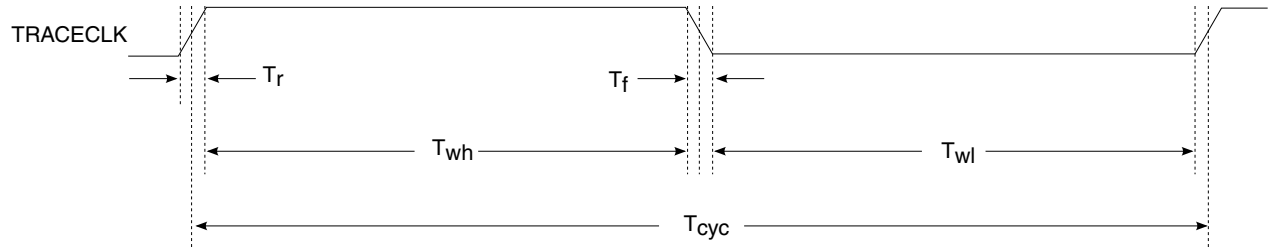

Figure 5. TRACE_CLKOUT specifications

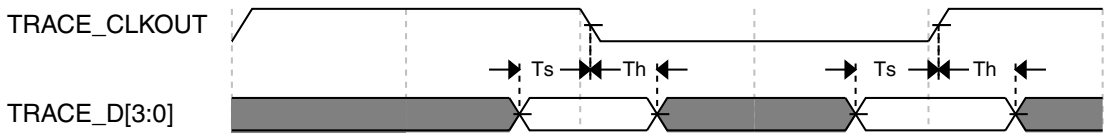

Figure 6. Trace data specifications

2. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.2.4 32 kHz oscillator electrical characteristics

3.2.4.1 32 kHz oscillator DC electrical specifications

Table 23. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.2.4.2 32 kHz oscillator frequency specifications

Table 24. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

3.3 Memories and memory interfaces

- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.
- The below timing are for a load of 15 pf (1.8 V) and 35 pf (3 V) or output pads
- All board delays need to be added appropriately
- Input hold time being negative does not have any implication or max achievable frequency

Table 26. QuadSPI input timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4	-	ns
T_{ih}	Hold time requirement for incoming data	1.5	-	ns

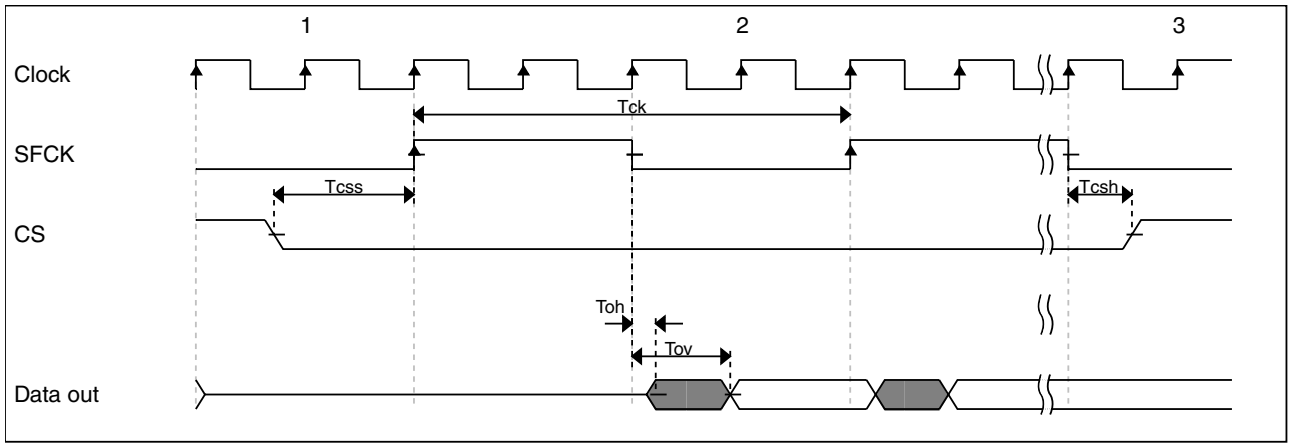

Figure 12. QuadSPI output timing (SDR mode) diagram

Table 27. QuadSPI output timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	-	2.8	ns
T_{oh}	Output Data Hold	-1.4	-	ns
T_{ck}	SCK clock period	-	100	MHz
T_{css}	Chip select output setup time	2	-	ns
T_{csh}	Chip select output hold time	-1	-	ns

NOTE

For any frequency setup and hold specifications of the memory should be met.

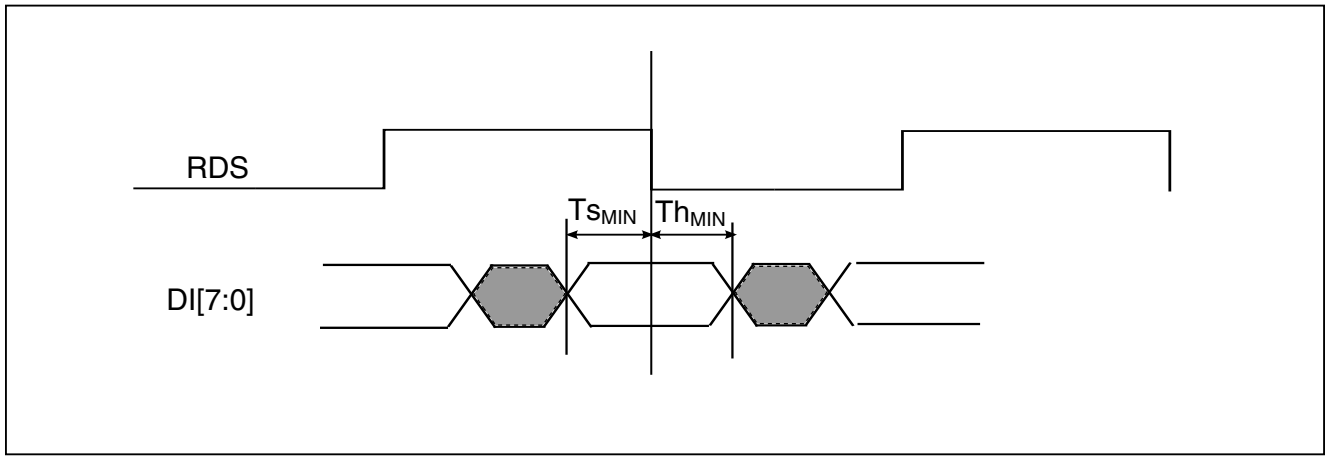

Figure 15. QuadSPI input timing (Hyperflash mode) diagram

Table 30. QuadSPI input timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Ts_{MIN}	Setup time for incoming data	2	-	ns
Th_{MIN}	Hold time requirement for incoming data	2	-	ns

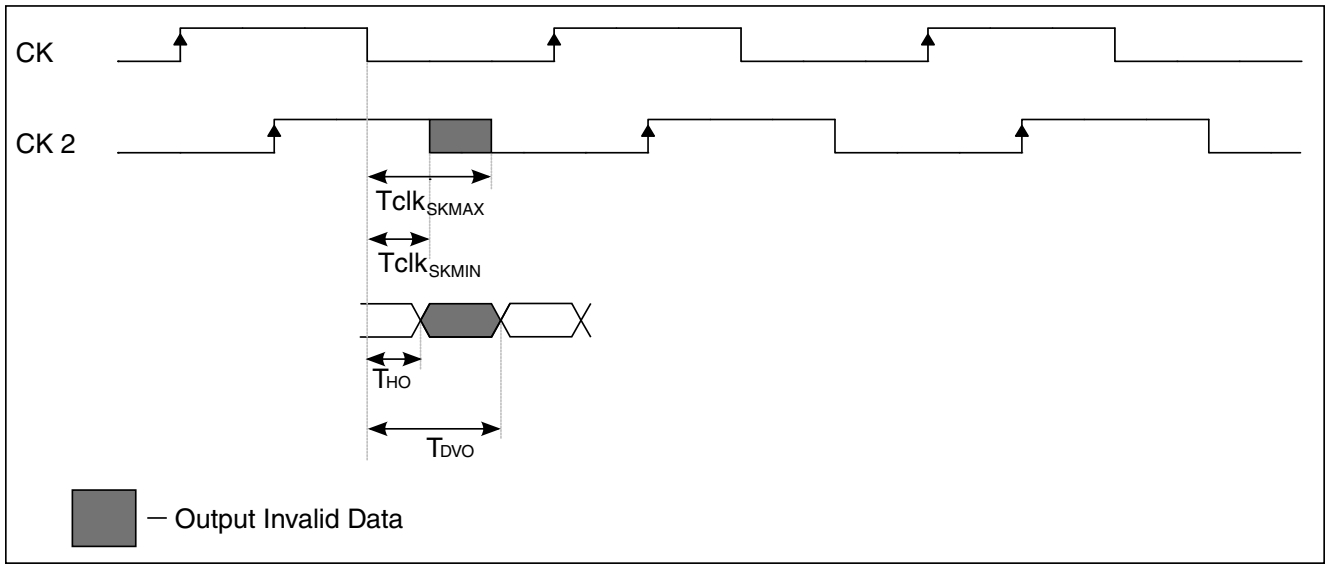

Figure 16. QuadSPI output timing (Hyperflash mode) diagram

Table 31. QuadSPI output timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Tdv_{MAX}	Output Data Valid	-	4.3	ns

Table continues on the next page...

Table 31. QuadSPI output timing (Hyperflash mode) specifications (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Tho	Output Data Hold	1.3	-	ns
$Tclk_{SKMAX}$	Ck to Ck2 skew max	-	T/4 + 0.5	ns
$Tclk_{SKMIN}$	Ck to Ck2 skew min	T/4 - 0.5	-	ns

NOTE

Maximum clock frequency = 75 MHz.

3.3.2 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.3.2.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 32. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk512k}$	Erase Flash Block high-voltage time for 512 KB	—	413	3616	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.3.2.2 Flash timing specifications — commands

Table 33. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk512k}$	Read 1s Block execution time • 512 KB program flash	—	—	1.8	ms	
$t_{rd1sec4k}$	Read 1s Section execution time (4 KB flash)	—	—	100	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
	Erase Flash Block execution time					2

Table continues on the next page...

Table 33. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{ersblk512k}$	• 512 KB program flash	—	435	3700	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec1k}$	Program Section execution time (1 KB flash)	—	5	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	6.7	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	1750	14,800	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	1750	14,800	ms	2
	Swap Control execution time					
$t_{swapx01}$	• control code 0x01	—	200	—	µs	
$t_{swapx02}$	• control code 0x02	—	90	150	µs	
$t_{swapx04}$	• control code 0x04	—	90	150	µs	
$t_{swapx08}$	• control code 0x08	—	—	30	µs	
$t_{swapx10}$	• control code 0x10	—	90	150	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.3.2.3 Flash high voltage current behaviors

Table 34. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.3.2.4 Reliability specifications

Table 35. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

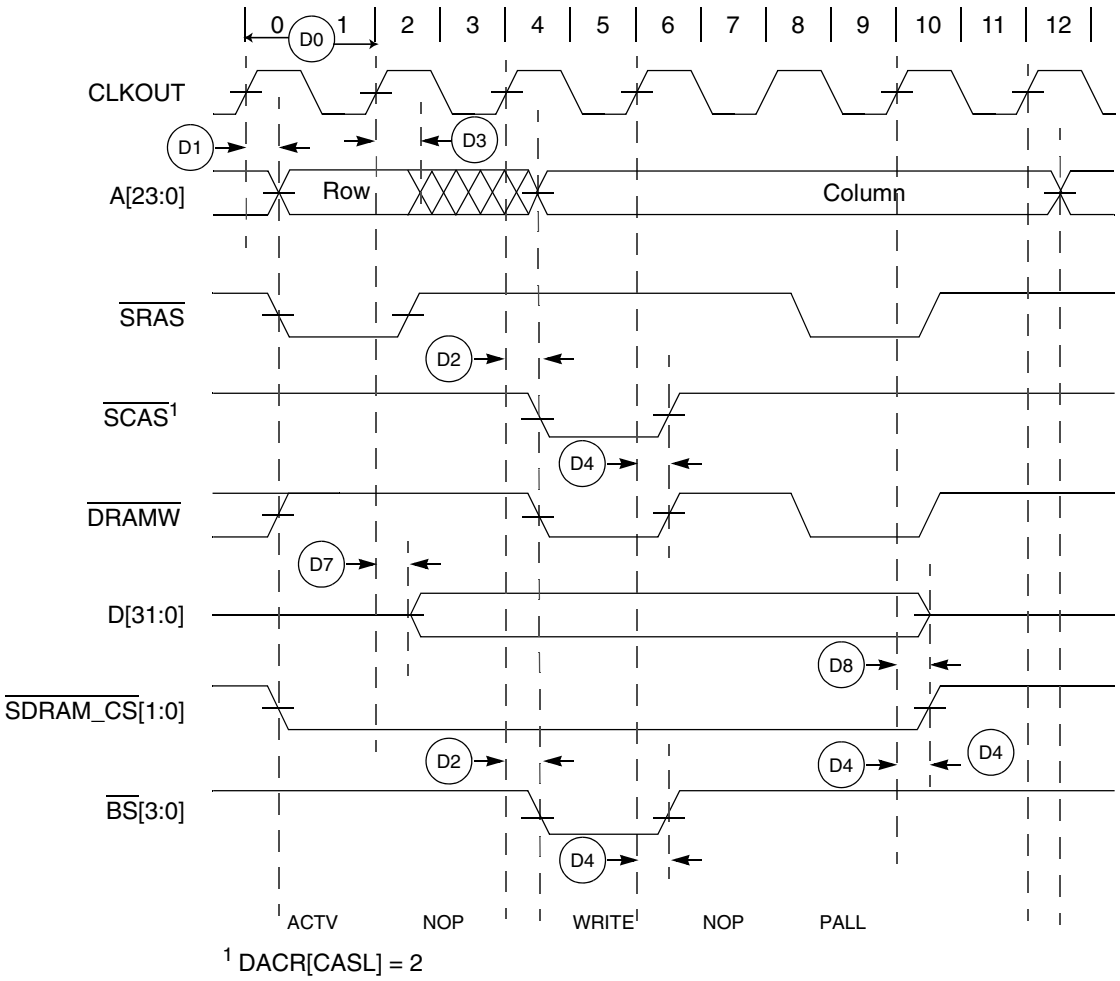

Figure 20. SDRAM write timing diagram

3.4 Analog

3.4.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 40 and Table 41 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.4.1.1 ADC operating conditions

Table 40. ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 × VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 8-bit / 10-bit / 12-bit modes	—	4	5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	kS/s	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

3.6.1 USB Voltage Regulator electrical specifications

Table 49. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREG_IN0 VREG_IN1	Regulator selectable input supply voltages	2.7	—	5.5	V	2
I_{DDon} VREG_IN0 VREG_IN1	Quiescent current — Run mode, load current equal zero, input supply (VREG_IN*) > 3.6 V	 — —	 157 157	 — —	µA	
I_{DDstby} VREG_IN0 VREG_IN1	Quiescent current — Standby mode, load current equal zero	 — —	2 2	— —	µA	
I_{DDoff} VREG_IN0 VREG_IN1	Quiescent current — Shutdown mode • VREG_IN*= 5.0 V and temperature=25 °C	 — —	 680 920	 — —	nA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	150	mA	3
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{DROPOUT}$	Regulator drop-out voltage — Run mode at maximum load current with inrush current limit disabled	300	—	—	mV	
VREG_OUT	Regulator programmable output target voltage — Selected input supply > programmed output target voltage + $V_{DROPOUT}$ • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	4
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	350	—	mA	5
I_{INRUSH}	Inrush current limit	40	—	100	mA	6, 7, 8, 9

1. Typical values assume the selected input supply is 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operation range is 2.7 V to 5.5 V; tolerance voltage is up to 6 V.
3. 150mA is inclusive of the run mode current of the on-chip USB modules. Available load outside of the chip depends on USB operation and device power dissipation limits.
4. The target voltage for the regulator is programmable, accounting for the range of the max and min values.
5. Current limit disabled.
6. Current limit should be disabled after the powers have stabilized to allow full functionality of the regulator.
7. Limited Characterization
8. I_{INRUSH} with VREGINx=4.0 V to 5.5 V
9. Total current load on startup should be less than I_{INRUSH} min over full input voltage range of the regulator.

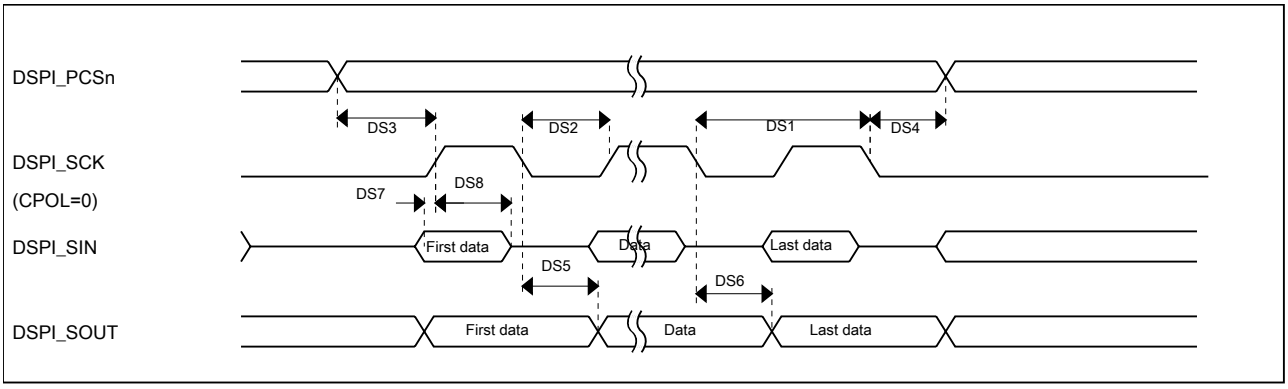

Figure 29. DSPI classic SPI timing — master mode

Table 56. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	23.1	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	13.0	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	13.0	ns

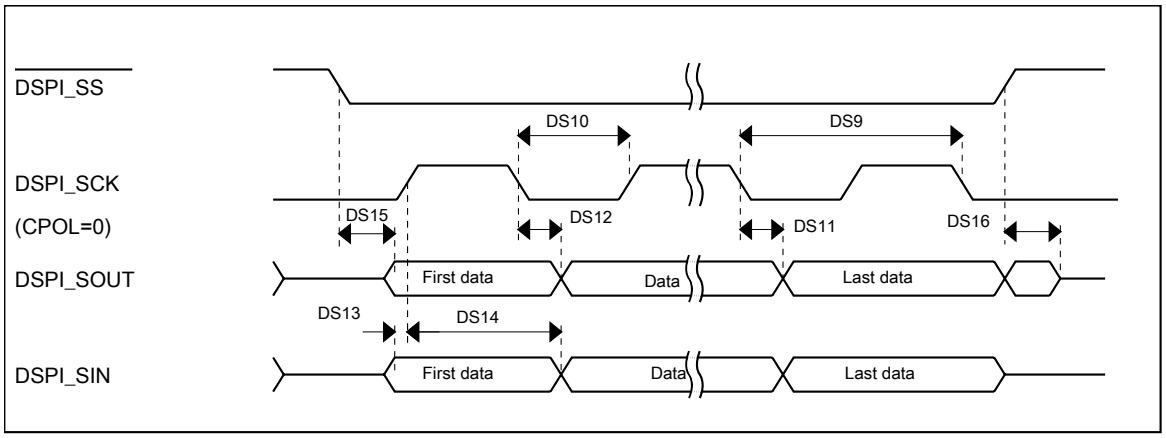

Figure 30. DSPI classic SPI timing — slave mode

Table 61. SDHC full voltage range switching specifications (continued)

Num	Symbol	Description	Min.	Max.	Unit
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	0	8.1	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

Table 62. SDHC limited voltage range switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	2.7	3.6	V
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	0	7	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

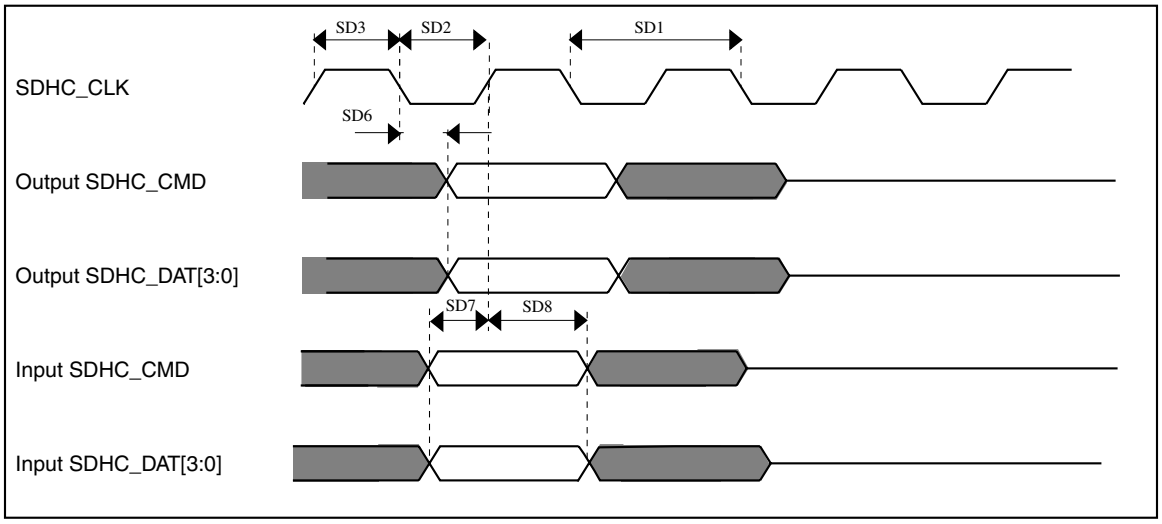

Figure 32. SDHC timing

3.6.9 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 63. I2S master mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	80	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	0	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	15	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

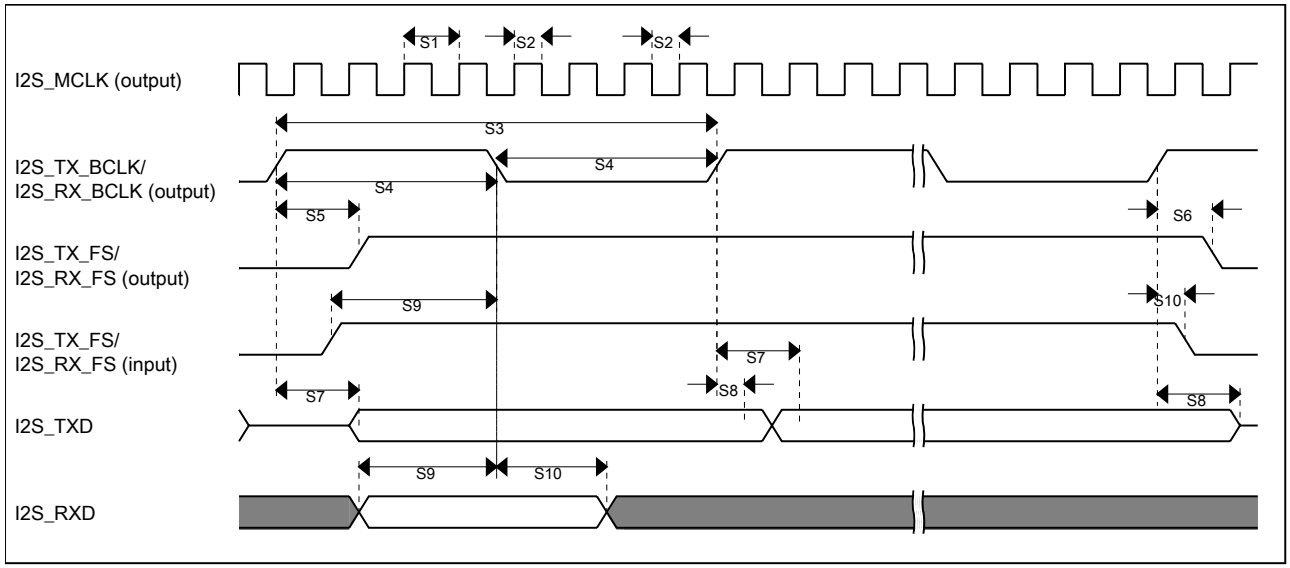

Figure 37. I2S/SAI timing — master modes

Table 68. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	5	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	56.5	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	5	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear