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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, I²C, QSPI, SDHC, SPI, UART/USART, USB
Peripherals	DMA, I²S, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16b SAR; D/A 2x6b, 1x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	210-UFBGA, WLCSP
Supplier Device Package	210-WLCSP (6.94x6.94)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk28fn2m0cau15r

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Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Digital supply voltage for Ports A, B, C,D	1.71	3.6	V	
V_{DDIO_E}	Digital Supply voltage for Port E	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{IH_E}	Input high voltage • 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V • 1.7 V ≤ V_{DDIO_E} ≤ 2.7 V	0.7 × V_{DDIO_E} 0.75 × V_{DDIO_E}	— —	V V	
V_{IL_E}	Input low voltage • 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V • 1.7 V ≤ V_{DDIO_E} ≤ 2.7 V	— —	0.35 × V_{DDIO_E} 0.3 × V_{DDIO_E}	V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
V_{HYS_E}	Input hysteresis	0.06 × V_{DDIO_E}	—	V	
I_{ICIO}	I/O pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Pseudo Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD_CORE} voltage required to retain RAM	1.14	1.47	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD} or V_{DDIO_E}. If V_{IN} is less than -0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(-0.3-V_{IN})/|I_{ICIO}|$. The actual resistor value should be an order of magnitude higher to tolerate transient voltages.
2. Open drain outputs must be pulled to VDD.

Table 6. Power consumption operating behaviors (through VDD_CORE) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDC_VLPR}	Very-low-power run mode current at 1.2 V — all peripheral clocks enabled, code of while(1) loop executing out of internal flash				mA	6
	• @ 25°C	—	1.7	5.5		
	• @ 70°C	—	3.1	8.5		
	• @ 85°C	—	4.3	11.0		
	• @ 105°C	—	6.7	16.2		
I_{DDC_VLPRCO}	Very-low-power run mode current in compute operation - 4 MHz core / 1 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 1.2 V				mA	7
	• @ 25°C	—	1.1	3.6		
	• @ 70°C	—	2.5	6.9		
	• @ 85°C	—	3.7	9.5		
	• @ 105°C	—	6.1	14.8		
I_{DDC_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 1.2 V				mA	3
	• @ 25°C	—	4.4	14.2		
	• @ 70°C	—	9.8	26.5		
	• @ 85°C	—	13.0	33.4		
	• @ 105°C	—	15.7	37.9		
I_{DDC_VLPW}	Very-low-power wait mode current at 1.2 V — all peripheral clocks disabled				mA	6
	• @ 25°C	—	0.759	2.5		
	• @ 70°C	—	2.2	5.9		
	• @ 85°C	—	3.3	8.6		
	• @ 105°C	—	5.8	14.0		
I_{DDC_VLPW}	Very-low-power wait mode current at 1.2 V— all peripheral clocks enabled				mA	6
	• @ 25°C	—	1.2	4.0		
	• @ 70°C	—	2.7	7.2		
	• @ 85°C	—	3.8	9.8		
	• @ 105°C	—	6.3	15.1		
I_{DDC_STOP}	Stop mode current at 1.2 V				mA	
	• @ 25°C	—	0.749	1.9		
	• @ 70°C	—	3.4	7.5		
	• @ 85°C	—	5.4	11.3		
	• @ 105°C	—	9.1	18.7		

Table continues on the next page...

Table 6. Power consumption operating behaviors (through VDD_CORE)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 25°C	—	0.454	0.546		
	• @ 70°C	—	0.724	0.897		
	• @ 85°C	—	1.1	1.4		
	• @ 105°C	—	2.0	2.6		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode.
3. MCG configured for PEE mode.
4. 150 MHz core and system clock, 50 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for PEE mode.
5. 25 MHz core and system clock, 25 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for FEI mode
6. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. Code executing from flash.
7. MCG configured for BLPE mode.
8. By default, this mode only has 32 K of SRAM enabled.
9. Includes 32 kHz oscillator current and RTC operation.

Table 7. Power consumption operating behaviors (through VDD)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code of while(1) loop executing from internal flash @ 3.0 V	—	2.0	2.1	mA	1
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code of while(1) loop executing from internal flash @ 3.0 V	—	2.0	2.1	mA	1
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
I_{DD_RUNCO}	Run mode current in compute operation - 120 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0 V				mA	2
	• @ 25°C	—	1.5	1.6		
	• @ 70°C	—	1.5	1.7		

Table continues on the next page...

Table 9. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							nA
	VLLS3	440	490	540	560	570	580	
	LLS2	490	490	540	560	570	680	
	LLS3	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I_{LPUART}	LPUART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA

Table 11. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
f_{B_CLK}	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, LPUART, CMT, timers, and I^2C signals.

Table 12. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	NMI_b pin interrupt pulse width (analog filter enabled) — Asynchronous path	100	—	ns	
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External RESET_b input pulse width (digital glitch filter disabled)	100	—	ns	
	Port rise and fall time (high drive strength) • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew disabled • $1.71 \le V_{DD} \le 2.7$ V • $2.7 \le V_{DD} \le 3.6$ V	 — — — —	 34 16 10 8	 ns ns ns ns	4, 5
	Port rise and fall time (low drive strength) • Slew enabled	 —	 34	 ns	6, 7

Table continues on the next page...

2.4.1 Thermal operating requirements

Table 13. Thermal operating requirements (for V-Temp range)

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is:

   $T_J = T_A + R\theta_{JA}$ x chip power dissipation

Table 14. Thermal operating requirements (for C-Temp range)

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	95	°C	
T_A	Ambient temperature	–40	85	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is:

   $T_J = T_A + R\theta_{JA}$ x chip power dissipation

2.4.2 Thermal attributes

Table 15. Thermal attributes

Board type	Symbol	Description	210 WLCSP	169 MAPBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	68.5	56.8	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	32.1	27.1	°C/W	1
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52.3	41	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	27.2	22.4	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	16.0	10.4	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.3	7.1	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	0.2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.

Table 18. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	• JTAG and CJTAG • Serial Wire Debug	25 12.5	— —	ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	30.6	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	19.0	ns
J12	TCLK low to TDO high-Z	—	17.0	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

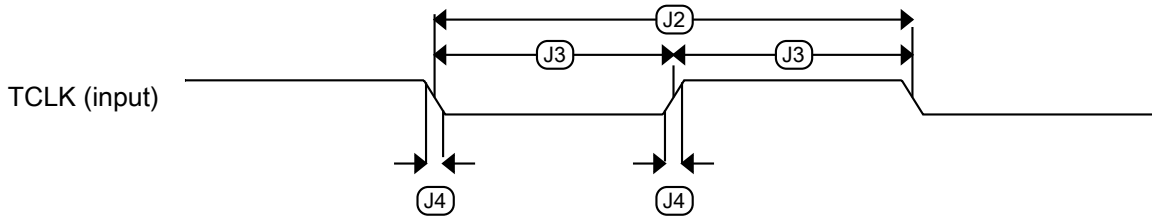

Figure 7. Test clock input timing

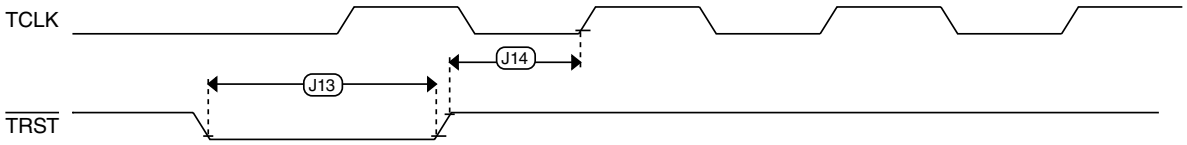

Figure 10. $\overline{\text{TRST}}$ timing

3.2 Clock modules

3.2.1 MCG specifications

Table 19. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
I_{ints}	Internal reference (slow clock) current	—	20	—	µA	
$t_{irefsts}$	[O:] Internal reference (slow clock) startup time	—	32	—	µs	
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	±1	± 2	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.5	± 1	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
I_{intf}	Internal reference (fast clock) current	—	25	—	µA	
$t_{irefsts}$	[L:] Internal reference startup time (fast clock)	—	10	15	µs	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00 ext clk freq: above (3/5)f_{int} never reset	(3/5) x f_{ints_t}	—	—	kHz	

Table continues on the next page...

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. This applies when SCTRIM at value (0x80) and SCFTRIM control bit at value (0x0).
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.2.2 IRC48M specifications

Table 20. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	520	—	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71 V-1.89 V) over temperature • Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0) • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	— —	± 0.5 ± 0.5	± 1.0 ± 1.5	$\%f_{irc48m}$	
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89 V-3.6 V) over temperature • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.5	± 1.0	$\%f_{irc48m}$	
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	1
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	µs	2

1. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
2. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
   - USB_CLK_RECOVER_IRC_EN[IRC_EN]=1, or
   - MCG_C7[OSCSEL]=10, or
   - SIM_SOPT2[PLLFLLSEL]=11

3.3.1 QuadSPI AC specifications

- All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing diagrams in this section.
- Measurements are with a load of 15 pf (1.8 V) and 35 pf (3 V) on output pins. Input slew: 1 ns
- Timings assume a setting of 0x0000_000x for QuadSPI _SMPR register (see the reference manual for details).

The following table lists the QuadSPI delay chain read/write settings. Refer the device reference manual for register and bit descriptions.

Table 25. QuadSPI delay chain read/write settings

Mode	QuadSPI registers				Notes
	QuadSPI_MCR[DQS_EN]	QuadSPI_SOCCR[SOCCFG]	QuadSPI_MCR[SCLKCFG]	QuadSPI_FLSHCR[TDH]	
SDR	Yes	3Fh	5	No	Delay of 63 buffer and 64 mux
DDR	Yes	3Fh	1	2	Delay of 63 buffer and 64 mux
Hyperflash	RDS driven from Flash	0h	No	2	Delay of 1 mux

SDR mode

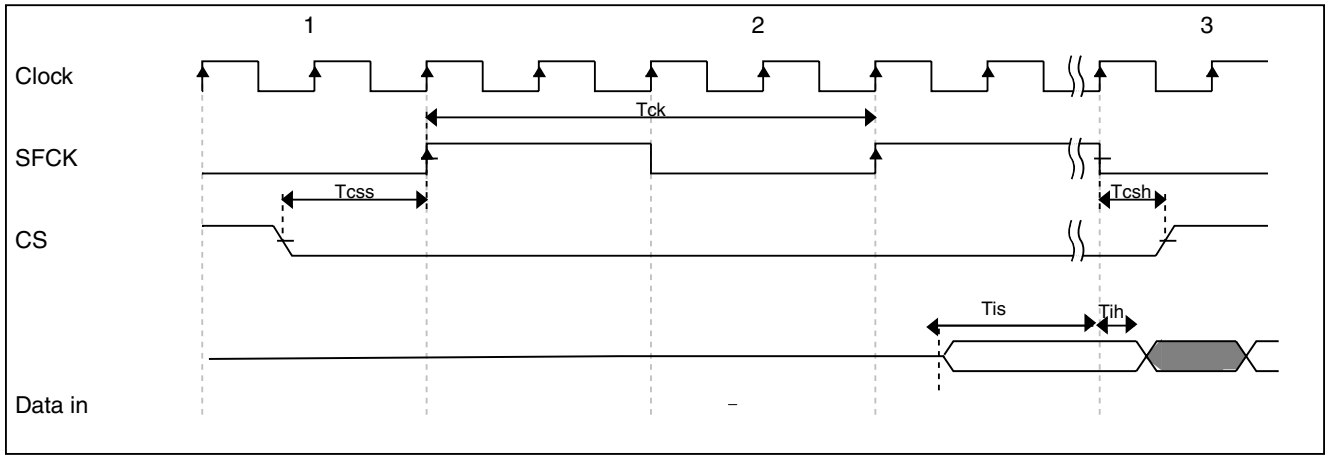

Figure 11. QuadSPI input timing (SDR mode) diagram

NOTE

- The below timing values are with default settings for sampling registers like QuadSPI_SMPR.

- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.
- The below timing are for a load of 15 pf (1.8 V) and 35 pf (3 V) or output pads
- All board delays need to be added appropriately
- Input hold time being negative does not have any implication or max achievable frequency

Table 26. QuadSPI input timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4	-	ns
T_{ih}	Hold time requirement for incoming data	1.5	-	ns

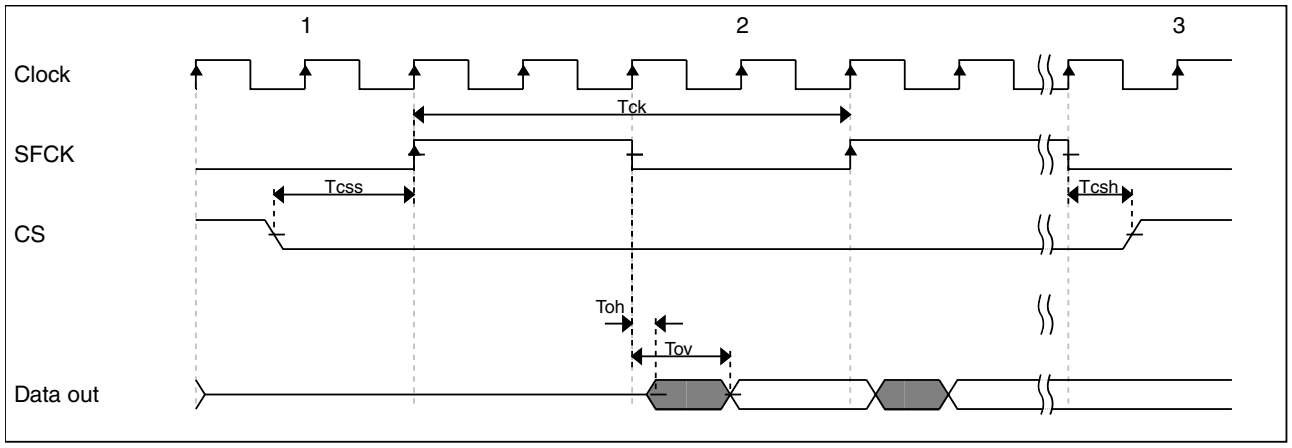

Figure 12. QuadSPI output timing (SDR mode) diagram

Table 27. QuadSPI output timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	-	2.8	ns
T_{oh}	Output Data Hold	-1.4	-	ns
T_{ck}	SCK clock period	-	100	MHz
T_{css}	Chip select output setup time	2	-	ns
T_{csh}	Chip select output hold time	-1	-	ns

NOTE

For any frequency setup and hold specifications of the memory should be met.

DDR Mode

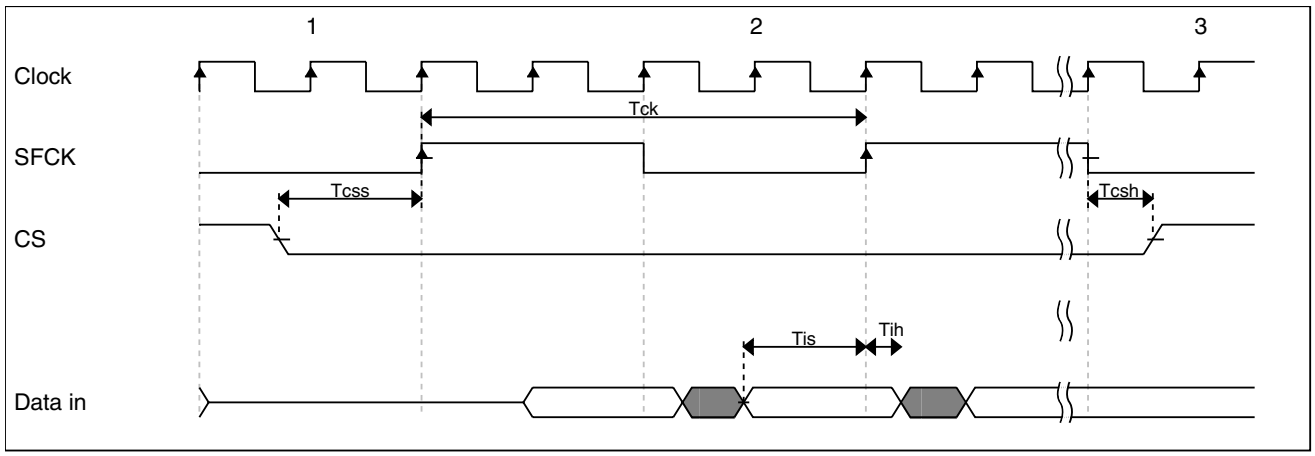

Figure 13. QuadSPI input timing (DDR mode) diagram

NOTE

- Numbers are for a load of 15 pf (1.8 V) and 35 pf (3 V)
- The numbers are for setting of hold condition in register QuadSPI_SMPR[DDRSNP]

Table 28. QuadSPI input timing (DDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4 (Without learning)	-	ns
		1 (With learning)		
T_{ih}	Hold time requirement for incoming data	1.5	-	ns

Table 31. QuadSPI output timing (Hyperflash mode) specifications (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Tho	Output Data Hold	1.3	-	ns
$Tclk_{SKMAX}$	Ck to Ck2 skew max	-	T/4 + 0.5	ns
$Tclk_{SKMIN}$	Ck to Ck2 skew min	T/4 - 0.5	-	ns

NOTE

Maximum clock frequency = 75 MHz.

3.3.2 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.3.2.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 32. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk512k}$	Erase Flash Block high-voltage time for 512 KB	—	413	3616	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.3.2.2 Flash timing specifications — commands

Table 33. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk512k}$	Read 1s Block execution time • 512 KB program flash	—	—	1.8	ms	
$t_{rd1sec4k}$	Read 1s Section execution time (4 KB flash)	—	—	100	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
	Erase Flash Block execution time					2

Table continues on the next page...

3.6.1 USB Voltage Regulator electrical specifications

Table 49. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREG_IN0 VREG_IN1	Regulator selectable input supply voltages	2.7	—	5.5	V	2
I_{DDon} VREG_IN0 VREG_IN1	Quiescent current — Run mode, load current equal zero, input supply (VREG_IN*) > 3.6 V	 — —	 157 157	 — —	µA	
I_{DDstby} VREG_IN0 VREG_IN1	Quiescent current — Standby mode, load current equal zero	 — —	2 2	— —	µA	
I_{DDoff} VREG_IN0 VREG_IN1	Quiescent current — Shutdown mode • VREG_IN*= 5.0 V and temperature=25 °C	 — —	 680 920	 — —	nA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	150	mA	3
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{DROPOUT}$	Regulator drop-out voltage — Run mode at maximum load current with inrush current limit disabled	300	—	—	mV	
VREG_OUT	Regulator programmable output target voltage — Selected input supply > programmed output target voltage + $V_{DROPOUT}$ • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	4
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	350	—	mA	5
I_{INRUSH}	Inrush current limit	40	—	100	mA	6, 7, 8, 9

1. Typical values assume the selected input supply is 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operation range is 2.7 V to 5.5 V; tolerance voltage is up to 6 V.
3. 150mA is inclusive of the run mode current of the on-chip USB modules. Available load outside of the chip depends on USB operation and device power dissipation limits.
4. The target voltage for the regulator is programmable, accounting for the range of the max and min values.
5. Current limit disabled.
6. Current limit should be disabled after the powers have stabilized to allow full functionality of the regulator.
7. Limited Characterization
8. I_{INRUSH} with VREGINx=4.0 V to 5.5 V
9. Total current load on startup should be less than I_{INRUSH} min over full input voltage range of the regulator.

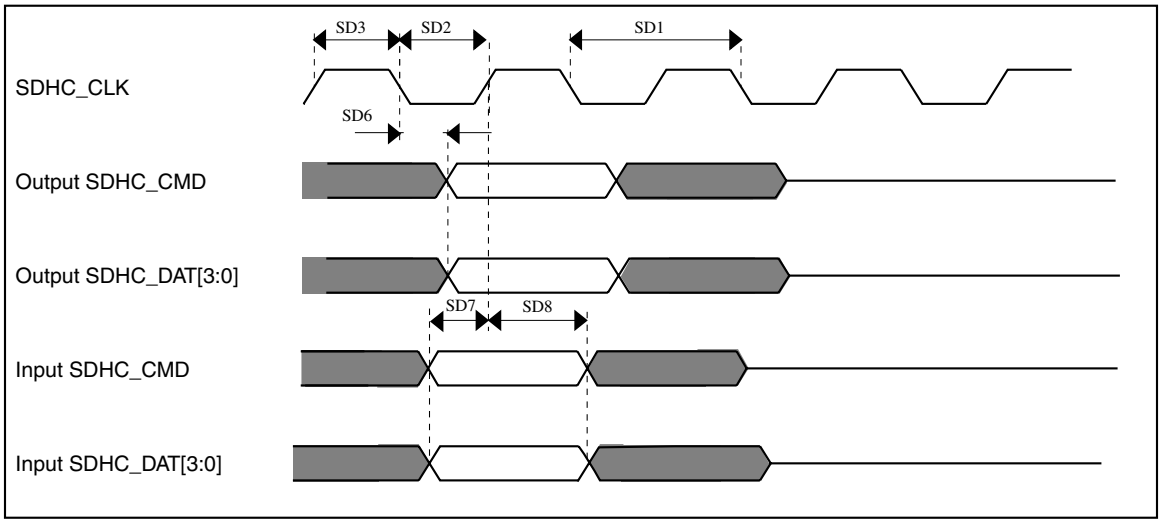

Figure 32. SDHC timing

3.6.9 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 63. I2S master mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	80	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	0	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	15	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

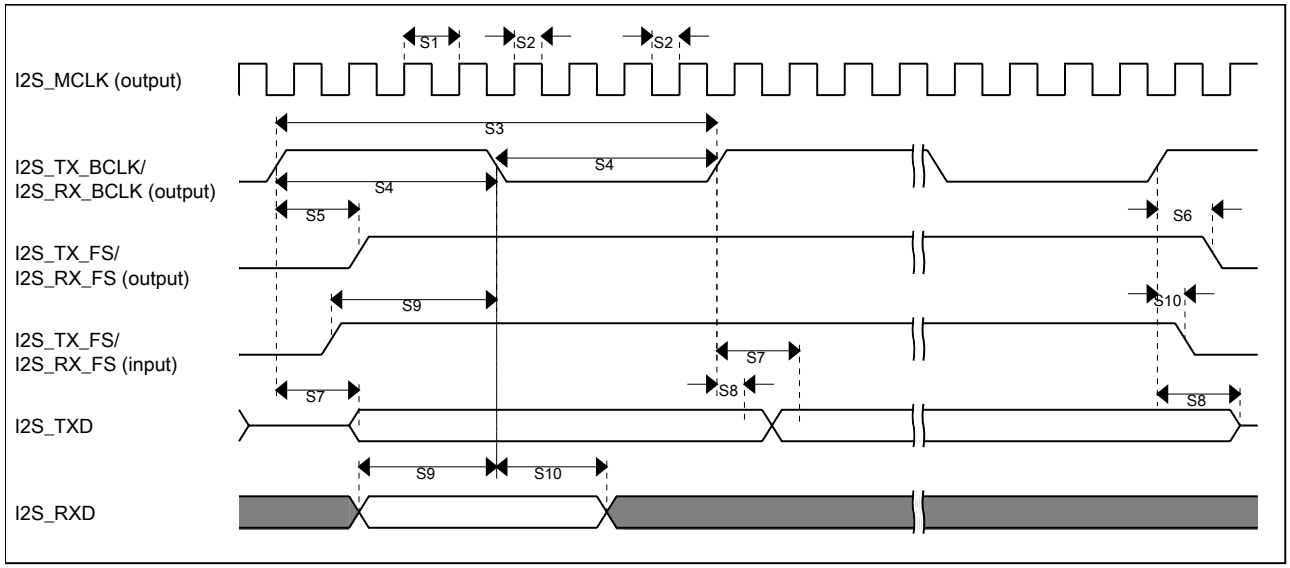

Figure 35. I2S/SAI timing — master modes

Table 66. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	23.1	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

5.1 K28F Signal Multiplexing and Pin Assignments

The signal multiplexing and pin assignments are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the “Pinout” tab.

The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

5.2 Recommended connection for unused analog and digital pins

Table 69 shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application

Table 69. Recommended connection for unused analog interfaces

Pin Type	K28F	Short recommendation	Detailed recommendation
Analog/non GPIO	ADCx/CMPx	Float	Analog input - Float
Analog/non GPIO	VREF_OUT	Float	Analog output - Float
Analog/non GPIO	DAC0_OUT, DAC1_OUT	Float	Analog output - Float
Analog/non GPIO	RTC_WAKEUP_B	Float	Analog output - Float
Analog/non GPIO	XTAL32	Float	Analog output - Float
Analog/non GPIO	EXTAL32	Float	Analog input - Float
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Digital	PTA0/JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	PTA1/JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA2/JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA3/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA4/NMI_b	10kΩ pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
USB	USB0_DP	Float	Float

Table continues on the next page...

Term	Definition
	• *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

Table 70. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated the symbol of Digital Supply voltage for Port E to V_{DDIO_E} and maximum value of V_{BAT} to 3.6 in Voltage and current operating requirements table • Updated the values of Power mode transition operating behaviors table • Updated the values of Power consumption operating behaviors (through VDD_CORE) table and Power consumption operating behaviors (through VDD) table in Power consumption operating behaviors section • Added power supplies figure and updated the verbiage in Power consumption operating behaviors section • Removed the footnote associated with Die junction Temperature in Thermal operating requirements (for V-Temp range) table and Thermal operating requirements (for C-Temp range) table in Thermal operating requirements section • Updated the values of Table 8 • Removed Low Voltage Detect of V_{DD_CORE} supply table • Removed the row that had entry of TSI0x in Recommended connection for unused analog interfaces table • Removed UART switching specifications section • Added statement about the package assembly information in Obtaining package dimensions section
4	03/2017	• Updated RAM array retained column by adding size in LLS2/VLLS2 additional Typical IDDC current consumption Adders table in Power consumption operating behaviors • Removed $f_{FlexCAN\_ERCLK}$ entry from Device clock specifications • Updated Pinout excel sheet