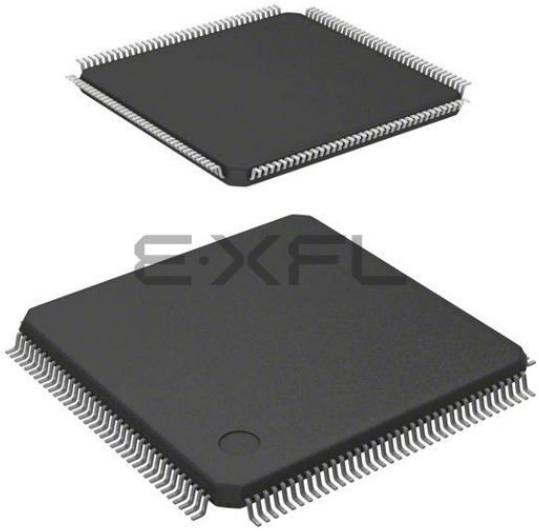


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 115 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 40x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l162zct6 |

# Contents

## 2.1 Device overview

**Table 2. Ultra-low-power STM32L162xC/C-A device features and peripheral counts**

| Peripheral | | STM32L162RC-A | STM32L162VC-A | STM32L162QC | STM32L162ZC |
|---|---|---|---|---|---|
| Flash (Kbytes) | | 256 | | | |
| Data EEPROM (Kbytes) | | 8 | | | |
| RAM (Kbytes) | | 32 | | | |
| AES | | 1 | | | |
| Timers | 32 bit | 1 | | | |
| | General-purpose | 6 | | | |
| | Basic | 2 | | | |
| Communi-cation interfaces | SPI | 8(3)(1) | | | |
| | $I^2S$ | 2 | | | |
| | $I^2C$ | 2 | | | |
| | USART | 3 | | | |
| | USB | 1 | | | |
| GPIOs | | 51 | 83 | 109 | 115 |
| Operation amplifiers | | 2 | | | |
| 12-bit synchronized ADC<br>Number of channels | | 1<br>21 | 1<br>25 | 1<br>40 | 1<br>40 |
| 12-bit DAC<br>Number of channels | | 2<br>2 | | | |
| LCD (STM32L152xx devices only)<br>COM x SEG | | 1<br>4x32 or 8x28 | 1<br>4x44 or 8x40 | | |
| Comparators | | 2 | | | |
| Capacitive sensing channels | | 23 | | | |
| Max. CPU frequency | | 32 MHz | | | |
| Operating voltage | | 1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option<br>1.65 V to 3.6 V without BOR option | | | |
| Operating temperatures | | Ambient operating temperature: -40 °C to 85 °C / -40 °C to 105 °C<br>Junction temperature: –40 to + 110 °C | | | |
| Packages | | LQFP64 | LQFP100 | UFBGA132 | LQFP144 |

1. 5 SPIs are USART configured in synchronous mode emulating SPI master.

**Table 5. Functionalities depending on the working mode (from Run/active down to standby)**

| Ips | Run/Active | Sleep | Low-power Run | Low-power Sleep | Stop | | Standby | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Wakeup capability | | Wakeup capability |
| CPU | Y | -- | Y | -- | -- | -- | -- | -- |
| Flash | Y | Y | Y | Y | -- | -- | -- | -- |
| RAM | Y | Y | Y | Y | Y | -- | -- | -- |
| Backup Registers | Y | Y | Y | Y | Y | -- | Y | -- |
| EEPROM | Y | Y | Y | Y | Y | -- | -- | -- |
| Brown-out rest (BOR) | Y | Y | Y | Y | Y | Y | Y | -- |
| DMA | Y | Y | Y | Y | -- | -- | -- | -- |
| Programmable Voltage Detector (PVD) | Y | Y | Y | Y | Y | Y | Y | -- |
| Power On Reset (POR) | Y | Y | Y | Y | Y | Y | Y | -- |
| Power Down Rest (PDR) | Y | Y | Y | Y | Y | -- | Y | -- |
| High Speed Internal (HSI) | Y | Y | -- | -- | -- | -- | -- | -- |
| High Speed External (HSE) | Y | Y | -- | -- | -- | -- | -- | -- |
| Low Speed Internal (LSI) | Y | Y | Y | Y | Y | -- | Y | -- |
| Low Speed External (LSE) | Y | Y | Y | Y | Y | -- | Y | -- |
| Multi-Speed Internal (MSI) | Y | Y | Y | Y | -- | -- | -- | -- |
| Inter-Connect Controller | Y | Y | Y | Y | -- | -- | -- | -- |
| RTC | Y | Y | Y | Y | Y | Y | Y | -- |
| RTC Tamper | Y | Y | Y | Y | Y | Y | Y | Y |
| Auto WakeUp (AWU) | Y | Y | Y | Y | Y | Y | Y | Y |
| LCD | Y | Y | Y | Y | Y | -- | -- | -- |
| USB | Y | Y | -- | -- | -- | Y | -- | -- |
| USART | Y | Y | Y | Y | Y | (1) | -- | -- |
| SPI | Y | Y | Y | Y | -- | -- | -- | -- |
| I2C | Y | Y | Y | Y | -- | (1) | -- | -- |

Table 8. STM32L162xC/C-A pin definitions (continued)

| Pins | | | | | Pin name | Pin Type(1) | I / O structure | Main function(2) (after reset) | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP144 | UFBGA132 | LQFP100 | LQFP64 | WLCSP64 | | | | | Alternate functions | Additional functions |
| 7 | C1 | 7 | 2 | C8 | PC13-WKUP2 | I/O | FT | PC13 | - | WKUP2/ RTC_TAMP1/ RTC_TS/ RTC_OUT |
| 8 | D1 | 8 | 3 | B8 | PC14-OSC32_IN(4) | I/O | TC | PC14 | - | OSC32_IN |
| 9 | E1 | 9 | 4 | B7 | PC15-OSC32_OUT | I/O | TC | PC15 | - | OSC32_OUT |
| 10 | D6 | - | - | - | PF0 | I/O | FT | PF0 | - | - |
| 11 | D5 | - | - | - | PF1 | I/O | FT | PF1 | - | - |
| 12 | D4 | - | - | - | PF2 | I/O | FT | PF2 | - | - |
| 13 | E4 | - | - | - | PF3 | I/O | FT | PF3 | - | - |
| 14 | F3 | - | - | - | PF4 | I/O | FT | PF4 | - | - |
| 15 | F4 | - | - | - | PF5 | I/O | FT | PF5 | - | - |
| 16 | F2 | 10 | - | - | $V_{SS\_5}$ | S | - | $V_{SS\_5}$ | - | - |
| 17 | G2 | 11 | - | - | $V_{DD\_5}$ | S | - | $V_{DD\_5}$ | - | - |
| 18 | G3 | - | - | - | PF6 | I/O | FT | PF6 | TIM5_CH1/TIM5_ETR | ADC_IN27 |
| 19 | G4 | - | - | - | PF7 | I/O | FT | PF7 | TIM5_CH2 | ADC_IN28/ COMP1_INP |
| 20 | H4 | - | - | - | PF8 | I/O | FT | PF8 | TIM5_CH3 | ADC_IN29/ COMP1_INP |
| 21 | J6 | - | - | - | PF9 | I/O | FT | PF9 | TIM5_CH4 | ADC_IN30/ COMP1_INP |
| 22 | - | - | - | - | PF10 | I/O | FT | PF10 | - | ADC_IN31/ COMP1_INP |
| 23 | F1 | 12 | 5 | D8 | PH0-OSC_IN(5) | I/O | TC | PH0 | - | OSC_IN |
| 24 | G1 | 13 | 6 | D7 | PH1-OSC_OUT(5) | I/O | TC | PH1 | - | OSC_OUT |
| 25 | H2 | 14 | 7 | C7 | NRST | I/O | RST | NRST | - | - |
| 26 | H1 | 15 | 8 | E8 | PC0 | I/O | FT | PC0 | LCD_SEG18 | ADC_IN10/ COMP1_INP |

Table 8. STM32L162xC/C-A pin definitions (continued)

| Pins | | | | | Pin name | Pin Type(1) | I / O structure | Main function(2) (after reset) | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP144 | UFBGA132 | LQFP100 | LQFP64 | WLCSP64 | | | | | Alternate functions | Additional functions |
| 96 | E12 | 63 | 37 | E1 | PC6 | I/O | FT | PC6 | TIM3_CH1/I2S2_MCK/ LCD_SEG24 | - |
| 97 | E11 | 64 | 38 | E2 | PC7 | I/O | FT | PC7 | TIM3_CH2/I2S3_MCK/ LCD_SEG25 | - |
| 98 | E10 | 65 | 39 | E3 | PC8 | I/O | FT | PC8 | TIM3_CH3/LCD_SEG26 | - |
| 99 | D12 | 66 | 40 | D1 | PC9 | I/O | FT | PC9 | TIM3_CH4/LCD_SEG27 | - |
| 100 | D11 | 67 | 41 | E4 | PA8 | I/O | FT | PA8 | USART1_CK/MCO/ LCD_COM0 | - |
| 101 | D10 | 68 | 42 | D2 | PA9 | I/O | FT | PA9 | USART1_TX / LCD_COM1 | - |
| 102 | C12 | 69 | 43 | D3 | PA10 | I/O | FT | PA10 | USART1_RX / LCD_COM2 | - |
| 103 | B12 | 70 | 44 | C1 | PA11 | I/O | FT | PA11 | USART1_CTS/ SPI1_MISO | USB_DM |
| 104 | A12 | 71 | 45 | C2 | PA12 | I/O | FT | PA12 | USART1_RTS/ SPI1_MOSI | USB_DP |
| 105 | A11 | 72 | 46 | D4 | PA13 | I/O | FT | JTMS-SWDIO | JTMS-SWDIO | - |
| 106 | C11 | 73 | - | - | PH2 | I/O | FT | PH2 | - | - |
| 107 | F11 | 74 | 47 | B1 | $V_{SS\_2}$ | S | - | $V_{SS\_2}$ | - | - |
| 108 | G11 | 75 | 48 | A1 | $V_{DD\_2}$ | S | - | $V_{DD\_2}$ | - | - |
| 109 | A10 | 76 | 49 | B2 | PA14 | I/O | FT | JTCK-SWCLK | JTCK-SWCLK | - |
| 110 | A9 | 77 | 50 | C3 | PA15 | I/O | FT | JTDI | TIM2_CH1_ETR/ SPI1_NSS/SPI3_NSS/ I2S3_WS/LCD_SEG17/ JTDI | - |
| 111 | B11 | 78 | 51 | A2 | PC10 | I/O | FT | PC10 | SPI3_SCK/I2S3_CK/ USART3_TX/ LCD_SEG28/LCD_SEG40/ LCD_COM4 | - |
| 112 | C10 | 79 | 52 | B3 | PC11 | I/O | FT | PC11 | SPI3_MISO/USART3_RX/ LCD_SEG29/LCD_SEG41/ LCD_COM5 | - |

Table 9. Alternate function input/output (continued)

| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFIO6 | AFIO7 | AFIO8 | .. | AFIO11 | AFIO12 | .. | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4/5 | TIM9/ 10/11 | I2C1/2 | SPI1/2 | SPI3 | USART1/2/3 | - | | LCD | - | | CPRI | SYSTEM |
| PG5 | - | - | - | - | - | - | - | - | - | | - | | | - | EVENT OUT |
| PG6 | - | - | - | - | - | - | - | - | - | | - | - | | - | EVENT OUT |
| PG7 | - | - | - | - | - | - | - | - | - | | - | - | | - | EVENT OUT |
| PG8 | - | - | - | - | - | - | - | - | - | | - | - | | - | EVENT OUT |
| PG9 | - | - | - | - | - | - | - | - | - | | - | | | - | EVENT OUT |
| PG10 | - | - | - | - | - | - | - | - | - | | - | | | - | EVENT OUT |
| PG11 | - | - | - | - | - | - | - | - | - | | - | - | | - | EVENT OUT |
| PG12 | - | - | - | - | - | - | - | - | - | | - | | | - | EVENT OUT |
| PG13 | - | - | - | - | - | - | - | - | - | | - | | | - | EVENT OUT |
| PG14 | - | - | - | - | - | - | - | - | - | | - | | | - | EVENT OUT |
| PG15 | - | - | - | - | - | - | - | - | - | | - | - | | - | EVENT OUT |
| PH0OSC_IN | - | - | - | - | - | - | - | - | - | | - | - | | - | - |
| PH1OSC_OUT | - | - | - | - | - | - | - | - | - | | - | - | | - | - |
| PH2 | - | - | - | - | - | - | - | - | - | | - | | | - | - |

4. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 10* for maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 10: Voltage characteristics* for the maximum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 12. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

# 6.3 Operating conditions

## 6.3.1 General operating conditions

**Table 13. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 0 | 32 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | 32 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | 32 | |
| $V_{DD}$ | Standard operating voltage | BOR detector disabled | 1.65 | 3.6 | V |
| | | BOR detector enabled, at power on | 1.8 | 3.6 | |
| | | BOR detector disabled, after power on | 1.65 | 3.6 | |
| $V_{DDA}$(1) | Analog operating voltage (ADC and DAC not used) | Must be the same voltage as $V_{DD}$(2) | 1.65 | 3.6 | V |
| | Analog operating voltage (ADC or DAC used) | | 1.8 | 3.6 | |
| $V_{IN}$ | I/O input voltage | FT pins; 2.0 V ≤$V_{DD}$ | -0.3 | 5.5(3) | V |
| | | FT pins; $V_{DD}$ < 2.0 V | -0.3 | 5.25(3) | |
| | | BOOT0 pin | 0 | 5.5 | |
| | | Any other pin | -0.3 | $V_{DD}$+0.3 | |
| $P_D$ | Power dissipation at TA = 85 °C for suffix 6 or TA = 105 °C for suffix 7(4) | UFBGA132 package | - | 333 | mW |
| | | LQFP144 package | - | 500 | |
| | | LQFP100 package | - | 465 | |
| | | LQFP64 package | - | 435 | |
| $T_A$ | Ambient temperature for 6 suffix version | Maximum power dissipation(5) | –40 | 85 | °C |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | –40 | 105 | |

**Table 19. Current consumption in Sleep mode**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(SLEEP)}$ | Supply current in Sleep mode, code executed from RAM, Flash switched OFF | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz, included $f_{HSE}$ = $f_{HCLK}$/2 above 16 MHz (PLL ON)(2) | Range3, Vcore=1.2 V VOS[1:0]=11 | 1 | 58 | 220 | µA |
| | | | | 2 | 96 | 300 | |
| | | | | 4 | 170 | 380 | |
| | | | Range2, Vcore=1.5 V VOS[1:0]=10 | 4 | 210 | 500 | |
| | | | | 8 | 400 | 700 | |
| | | | | 16 | 810 | 1100 | |
| | | | Range1, Vcore=1.8 V VOS[1:0]=01 | 8 | 485 | 800 | |
| | | | | 16 | 955 | 1250 | |
| | | | | 32 | 2100 | 2700 | |
| | | HSI clock source (16 MHz) | Range2, Vcore=1.5 V VOS[1:0]=10 | 16 | 835 | 1100 | |
| | | | Range1, Vcore=1.8 V VOS[1:0]=01 | 32 | 2100 | 2700 | |
| | | MSI clock, 65 kHZ | Range3, Vcore=1.2 V VOS[1:0]=11 | 0.065 | 18.5 | 72 | |
| | | MSI clock, 524 kHZ | | 0.524 | 37 | 92 | |
| | | MSI clock, 4.2 MHZ | | 4.2 | 180 | 273 | |
| | Supply current in Sleep mode, Flash switched ON | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz, included $f_{HSE}$ = $f_{HCLK}$/2 above 16MHz (PLL ON)(2) | Range3, Vcore=1.2 V VOS[1:0]=11 | 1 | 75 | 250 | |
| | | | | 2 | 115 | 300 | |
| | | | | 4 | 200 | 380 | |
| | | | Range2, Vcore=1.5 V VOS[1:0]=10 | 4 | 230 | 500 | |
| | | | | 8 | 430 | 700 | |
| | | | | 16 | 840 | 1120 | |
| | | | Range1, Vcore=1.8 V VOS[1:0]=01 | 8 | 500 | 800 | |
| | | | | 16 | 980 | 1300 | |
| | | | | 32 | 2100 | 2700 | |
| | | HSI clock source (16 MHz) | Range2, Vcore=1.5 V VOS[1:0]=10 | 16 | 860 | 1160 | |
| | | | Range1, Vcore=1.8 V VOS[1:0]=01 | 32 | 2150 | 2800 | |
| | | MSI clock, 65 kHZ | Range3, Vcore=1.2 V VOS[1:0]=11 | 0.065 | 33,5 | 90 | |
| | | MSI clock, 524 kHZ | | 0.524 | 53 | 110 | |
| | | MSI clock, 4.2 MHZ | | 4.2 | 200 | 290 | |

1. Guaranteed by characterization results, unless otherwise specified.

**Table 23. Typical and maximum current consumptions in Standby mode**

| Symbol | Parameter | Conditions | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ (Standby with RTC) | Supply current in Standby mode with RTC enabled | RTC clocked by LSI (no independent watchdog) | $T_A$ = -40 °C to 25 °C $V_{DD}$ = 1.8 V | 0.82 | - | µA |
| | | | $T_A$ = -40 °C to 25 °C | 1.15 | 1.9 | |
| | | | $T_A$ = 55 °C | 1.15 | 2.2 | |
| | | | $T_A$= 85 °C | 1.65 | 4 | |
| | | | $T_A$ = 105 °C | 2.75 | 8.3(2) | |
| | | RTC clocked by LSE external quartz (no independent watchdog)(3) | $T_A$ = -40 °C to 25 °C $V_{DD}$ = 1.8 V | 1.05 | - | |
| | | | $T_A$ = -40 °C to 25 °C | 1.35 | - | |
| | | | $T_A$ = 55 °C | 1.55 | - | |
| | | | $T_A$= 85 °C | 2.1 | - | |
| | | | $T_A$ = 105 °C | 3.3 | - | |
| $I_{DD}$ (Standby) | Supply current in Standby mode (RTC disabled) | Independent watchdog and LSI enabled | $T_A$ = -40 °C to 25 °C | 1 | 1.7 | |
| | | Independent watchdog and LSI OFF | $T_A$ = -40 °C to 25 °C | 0.305 | 0.6 | |
| | | | $T_A$ = 55 °C | 0.365 | 0.9 | |
| | | | $T_A$ = 85 °C | 0.66 | 2.75 | |
| | | | $T_A$ = 105 °C | 2 | 7(2) | |
| $I_{DD}$ (WU from Standby) | Supply current during wakeup time from Standby mode | - | $T_A$ = -40 °C to 25 °C | 1 | - | mA |

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

**Table 24. Peripheral current consumption(1)**

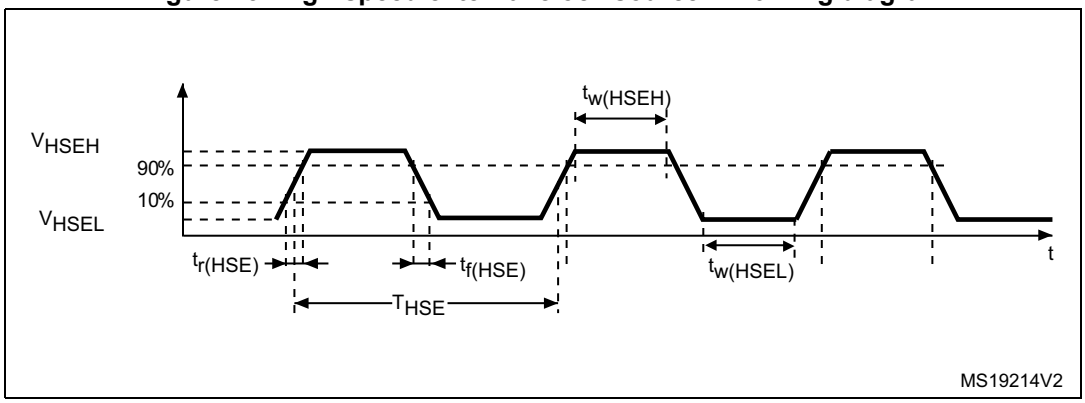
| Peripheral | | Typical consumption, $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | | | | Unit |
|---|---|---|---|---|---|---|
| | | Range 1, $V_{CORE}$= 1.8 V VOS[1:0] = 01 | Range 2, $V_{CORE}$= 1.5 V VOS[1:0] = 10 | Range 3, $V_{CORE}$= 1.2 V VOS[1:0] = 11 | Low-power sleep and run | |
| APB1 | TIM2 | 14.3 | 12.1 | 9.5 | 12.1 | µA/MHz ($f_{HCLK}$) |
| | TIM3 | 13.8 | 11.7 | 9.2 | 11.7 | |
| | TIM4 | 13.2 | 11.1 | 8.7 | 11.1 | |
| | TIM5 | 17.7 | 14.9 | 11.8 | 14.9 | |
| | TIM6 | 4.8 | 4.0 | 3.0 | 4.0 | |
| | TIM7 | 4.7 | 3.9 | 3.0 | 3.9 | |
| | LCD | 5.0 | 4.1 | 3.3 | 4.1 | |
| | WWDG | 3.5 | 2.9 | 2.3 | 2.9 | |
| | SPI2 | 8.9 | 7.4 | 5.8 | 7.4 | |
| | SPI3 | 7.3 | 6.0 | 4.8 | 6.0 | |
| | USART2 | 9.4 | 7.7 | 6.1 | 7.7 | |
| | USART3 | 9.4 | 7.6 | 6.0 | 7.6 | |
| | I2C1 | 8.9 | 7.4 | 5.8 | 7.4 | |
| | I2C2 | 7.9 | 6.4 | 5.1 | 6.4 | |
| | USB | 21.2 | 18.0 | 14.3 | 18.0 | |
| | PWR | 4.0 | 3.2 | 2.5 | 3.2 | |
| | DAC | 6.3 | 5.5 | 4.4 | 5.5 | |
| | COMP | 4.9 | 3.9 | 3.2 | 3.9 | |

**Table 26. High-speed external user clock characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{HSEH}$ | OSC_IN input pin high level voltage | - | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(HSEH)}$ $t_{w(HSEL)}$ | OSC_IN high or low time | | 12 | - | - | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time | | - | - | 20 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance | | - | 2.6 | - | pF |

1. Guaranteed by design.

**Figure 13. High-speed external clock source AC timing diagram**



## Flash memory and data EEPROM

**Table 35. Flash memory and data EEPROM characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage Read / Write / Erase | - | 1.65 | - | 3.6 | V |
| $t_{prog}$ | Programming/ erasing time for byte / word / double word / half-page | Erasing | - | 3.28 | 3.94 | ms |
| | | Programming | - | 3.28 | 3.94 | |
| $I_{DD}$ | Average current during the whole programming / erase operation | $T_A$ = 25 °C, $V_{DD}$ = 3.6 V | - | 600 | 900 | µA |
| | Maximum current (peak) during the whole programming / erase operation | | - | 1.5 | 2.5 | mA |

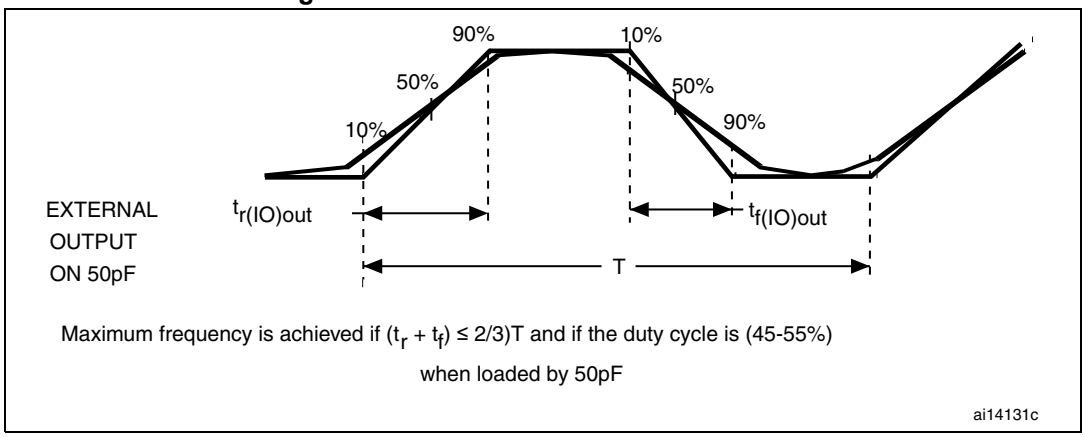
1. Guaranteed by design.

**Table 36. Flash memory and data EEPROM endurance and retention**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min(1) | Typ | Max | |
| $N_{CYC}$(2) | Cycling (erase / write) Program memory | $T_A$ = -40°C to 105 °C | 10 | - | - | kcycles |
| | Cycling (erase / write) EEPROM data memory | | 300 | - | - | |
| $t_{RET}$(2) | Data retention (program memory) after 10 kcycles at $T_A$ = 85 °C | $T_{RET}$ = +85 °C | 30 | - | - | years |
| | Data retention (EEPROM data memory) after 300 kcycles at $T_A$ = 85 °C | | 30 | - | - | |
| | Data retention (program memory) after 10 kcycles at $T_A$ = 105 °C | $T_{RET}$ = +105 °C | 10 | - | - | |
| | Data retention (EEPROM data memory) after 300 kcycles at $T_A$ = 105 °C | | 10 | - | - | |

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

**Figure 17. I/O AC characteristics definition**




## 6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 45*)

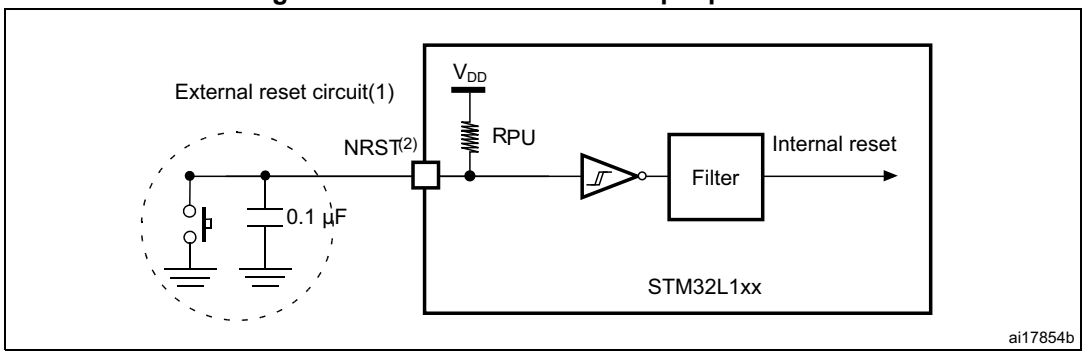
Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the conditions summarized in *Table 13*.

**Table 45. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST input low level voltage | - | - | - | 0.3 $V_{DD}$ | V |
| $V_{IH(NRST)}$(1) | NRST input high level voltage | - | 0.7 $V_{DD}$ | - | - | |
| $V_{OL(NRST)}$(1) | NRST output low level voltage | $I_{OL}$ = 2 mA 2.7 V < $V_{DD}$ < 3.6 V | - | - | 0.4 | |
| | | $I_{OL}$ = 1.5 mA 1.65 V < $V_{DD}$ < 2.7 V | - | - | | |
| $V_{hys(NRST)}$(1) | NRST Schmitt trigger voltage hysteresis | - | - | 10%$V_{DD}$(2) | - | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor(3) | $V_{IN}$ = $V_{SS}$ | 30 | 45 | 60 | kΩ |
| $V_{F(NRST)}$(1) | NRST input filtered pulse | - | - | - | 50 | ns |
| $V_{NF(NRST)}$(3) | NRST input not filtered pulse | - | 350 | - | - | ns |

1. Guaranteed by design.
2. With a minimum of 200 mV.
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

**Figure 18. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 45*. Otherwise the reset will not be taken into account by the device.

## 6.3.15 TIM timer characteristics

The parameters given in the *Table 46* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output ction characteristics (output compare, input capture, external clock, PWM output).

**Table 46. TIMx(1) characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | - | 1 | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | 31.25 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | - | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 32 MHz | 0 | 16 | MHz |
| $Res_{TIM}$ | Timer resolution | - | | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected (timer's prescaler disabled) | - | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | 0.0312 | 2048 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | - | 134.2 | s |

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

**Figure 20. SPI timing diagram - slave mode and CPHA = 0**

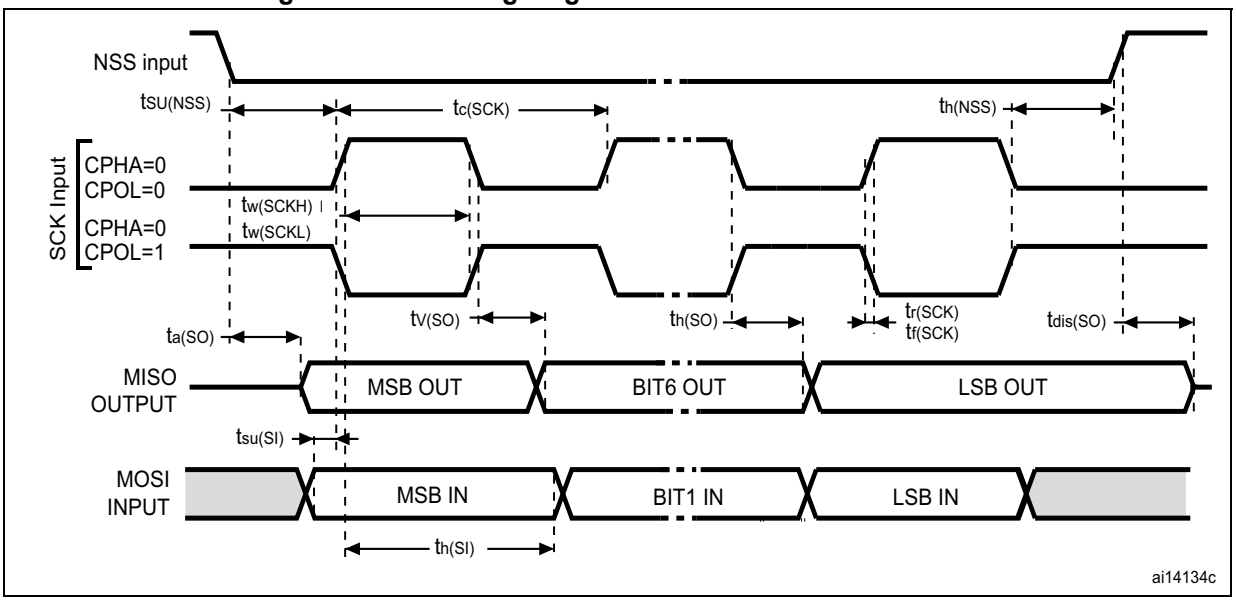
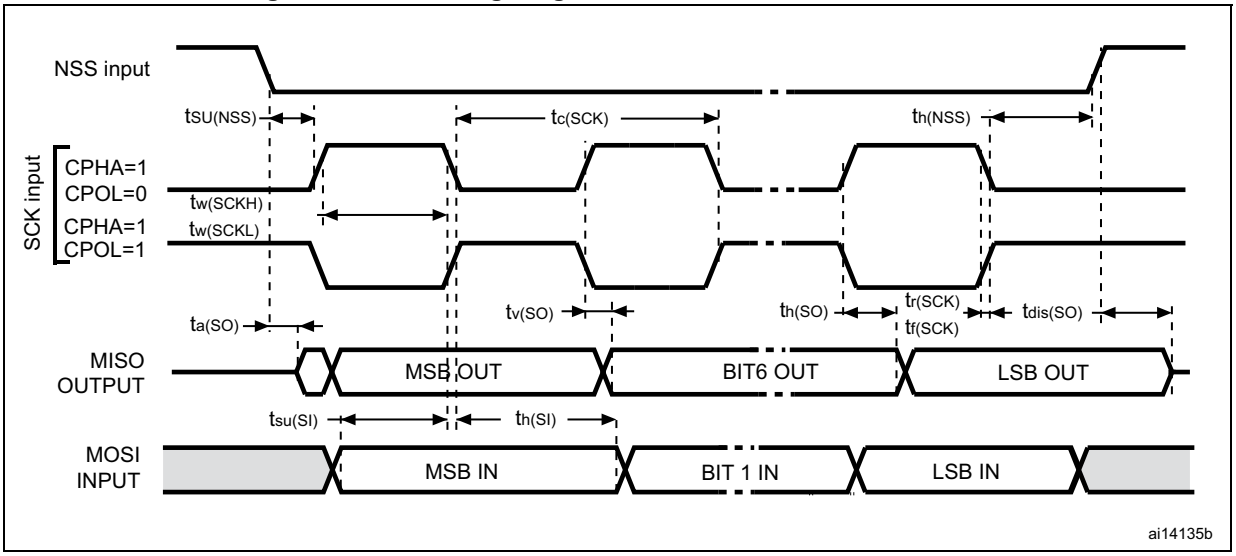



**Figure 21. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Table 52. USB: full speed electrical characteristics (continued)**

| Driver characteristics[1] | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | | 1.3 | 2.0 | V |

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

## I2S characteristics

**Table 53. I2S characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCK}$ | I2S Main Clock Output | | 256 x 8K | 256xFs (1) | MHz |
| $f_{CK}$ | I2S clock frequency | Master data: 32 bits | - | 64xFs | MHz |
| | | Slave data: 32 bits | - | 64xFs | |
| $D_{CK}$ | I2S clock frequency duty cycle | Slave receiver, 48KHz | 30 | 70 | % |
| $t_{r(CK)}$ | I2S clock rise time | Capacitive load CL=30pF | - | 8 | ns |
| $t_{f(CK)}$ | I2S clock fall time | | | 8 | |
| $t_{v(WS)}$ | WS valid time | Master mode | 4 | 24 | |
| $t_{h(WS)}$ | WS hold time | Master mode | 0 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 15 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 0 | - | |
| $t_{su(SD\_MR)}$ | Data input setup time | Master receiver | 8 | - | |
| $t_{su(SD\_SR)}$ | Data input setup time | Slave receiver | 9 | - | |
| $t_{h(SD\_MR)}$ | Data input hold time | Master receiver | 5 | - | |
| $t_{h(SD\_SR)}$ | | Slave receiver | 4 | - | |
| $t_{v(SD\_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 64 | |
| $t_{h(SD\_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 22 | - | |
| $t_{v(SD\_MT)}$ | Data output valid time | Master transmitter (after enable edge) | - | 12 | |
| $t_{h(SD\_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 8 | - | |

1. The maximum for 256xFs is 8 MHz

*Note: Refer to the I2S section of the product reference manual for more details about the sampling frequency (Fs), $f_{MCK}$, $f_{CK}$ and $D_{CK}$ values. These values reflect only the digital peripheral behavior, source clock precision might slightly change them. DCK depends mainly on the*

**Figure 28. Maximum dynamic current consumption on $V_{REF+}$ supply pin during ADC conversion**

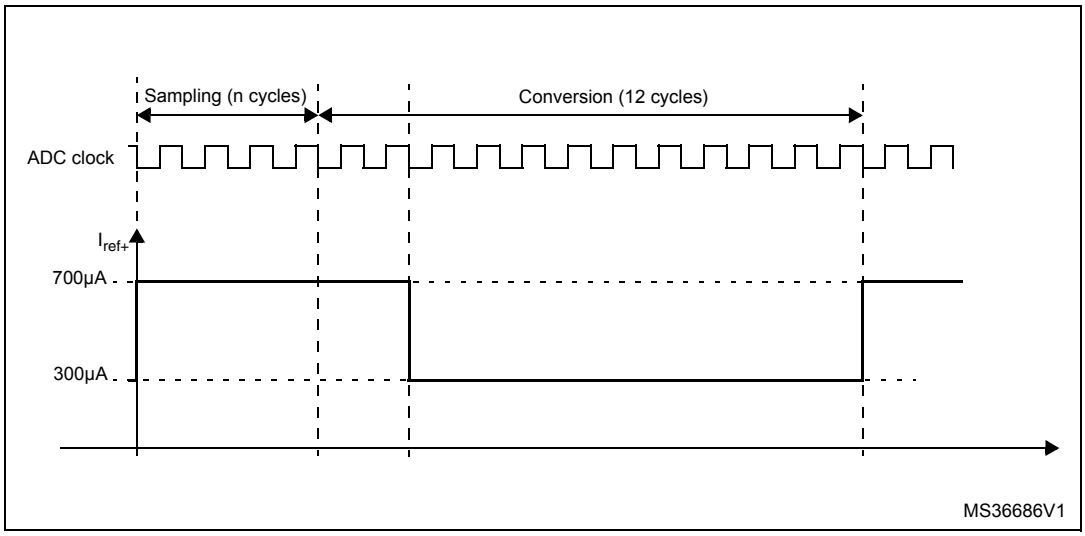



**Table 57. Maximum source impedance $R_{AIN}$ max(1)**

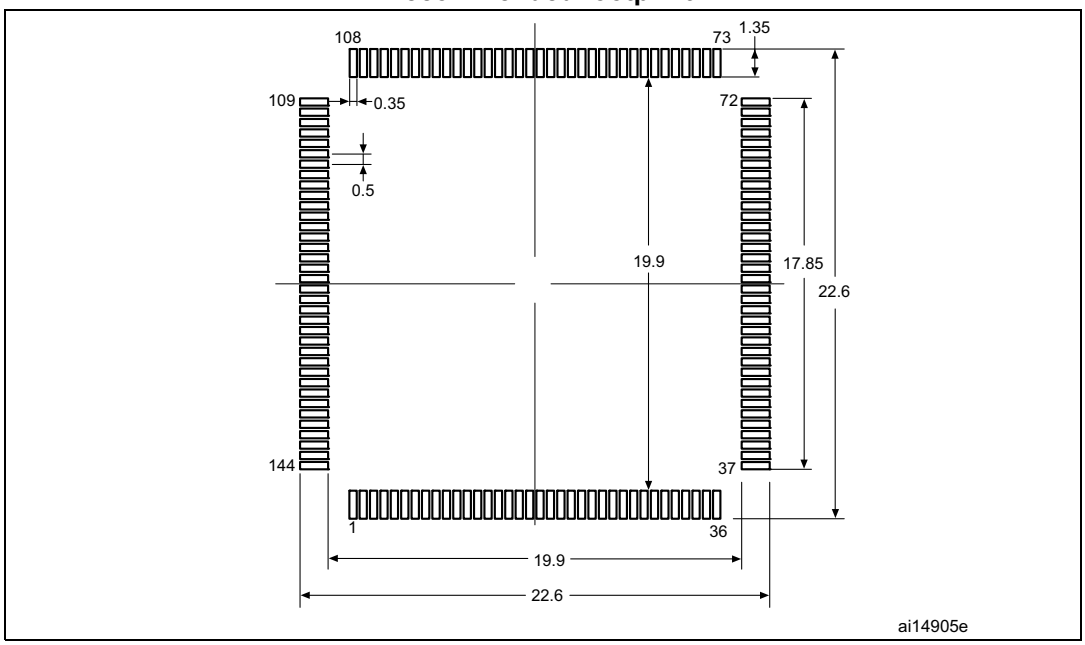
| Ts (µs) | $R_{AIN}$ max (kΩ) | | | | Ts (cycles) $f_{ADC}$=16 MHz(2) |
|---|---|---|---|---|---|
| | Multiplexed channels | | Direct channels | | |
| | 2.4 V < $V_{DDA}$ < 3.6 V | 1.8 V < $V_{DDA}$ < 2.4 V | 2.4 V < $V_{DDA}$ < 3.6 V | 1.8 V < $V_{DDA}$ < 2.4 V | |
| 0.25 | Not allowed | Not allowed | 0.7 | Not allowed | 4 |
| 0.5625 | 0.8 | Not allowed | 2.0 | 1.0 | 9 |
| 1 | 2.0 | 0.8 | 4.0 | 3.0 | 16 |
| 1.5 | 3.0 | 1.8 | 6.0 | 4.5 | 24 |
| 3 | 6.8 | 4.0 | 15.0 | 10.0 | 48 |
| 6 | 15.0 | 10.0 | 30.0 | 20.0 | 96 |
| 12 | 32.0 | 25.0 | 50.0 | 40.0 | 192 |
| 24 | 50.0 | 50.0 | 50.0 | 50.0 | 384 |

1. Guaranteed by design.
2. Number of samples calculated for $f_{ADC}$ = 16 MHz. For $f_{ADC}$ = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (µs),

## General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10*. The applicable procedure depends on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

**Figure 31. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint**

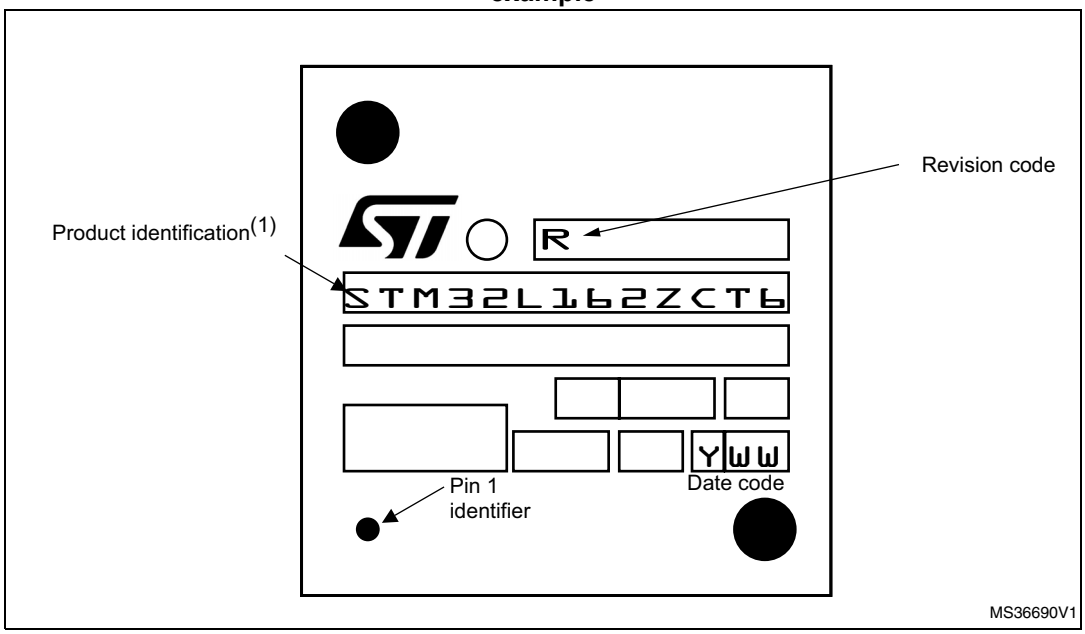



1. Dimensions are in millimeters.

## Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 32. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package top view example**



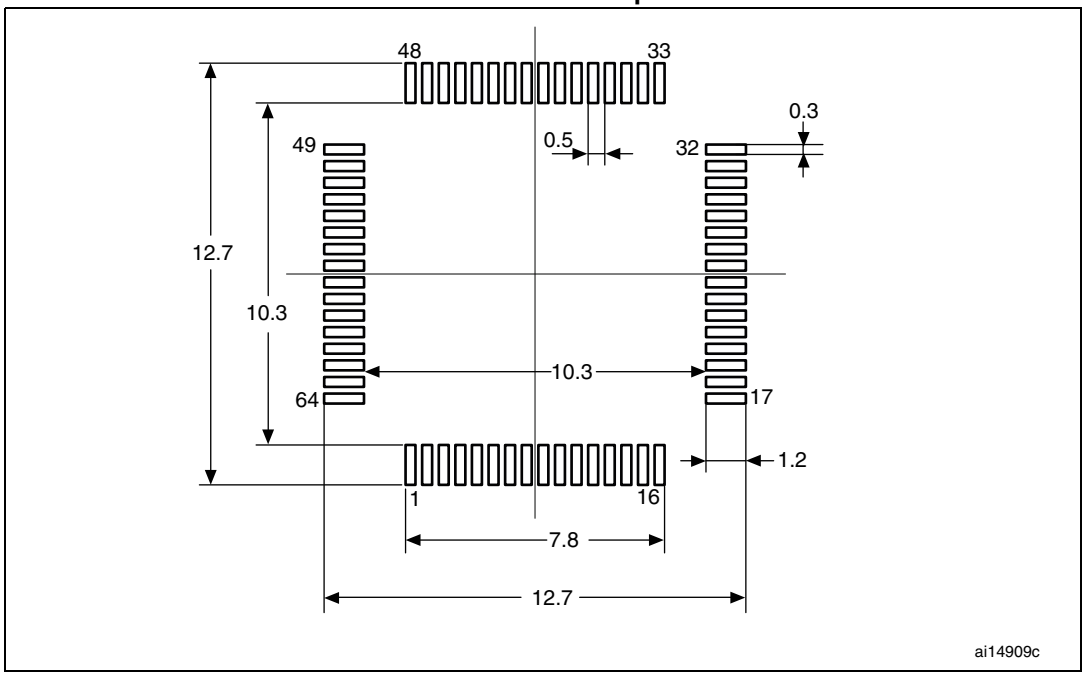

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering

**Table 67. LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

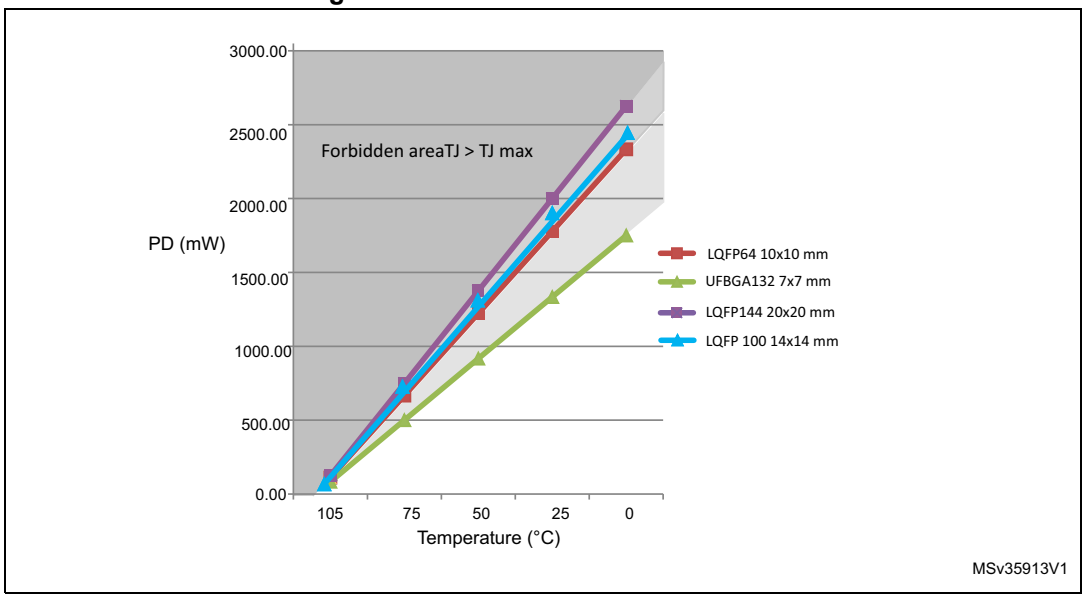
1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 37. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package recommended footprint**




1. Dimensions are in millimeters.

**Figure 43. Thermal resistance suffix 7**




### 7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.