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### What is "[Embedded - Microcontrollers](#)"?

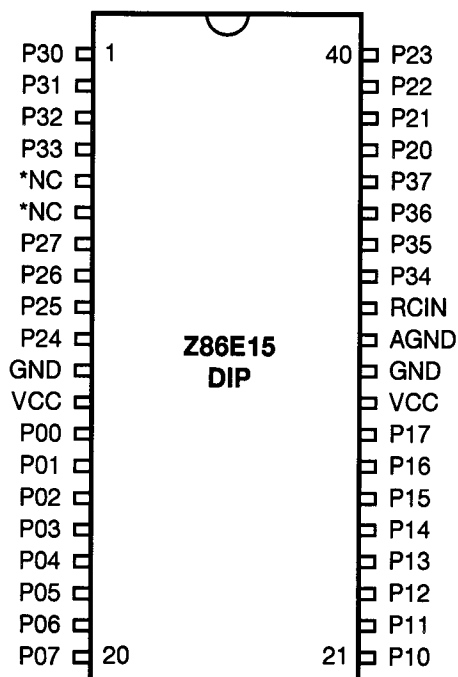
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	5MHz
Connectivity	-
Peripherals	LED, POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	188 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z86e1505psc">https://www.e-xfl.com/product-detail/zilog/z86e1505psc</a>

## PIN DESCRIPTION

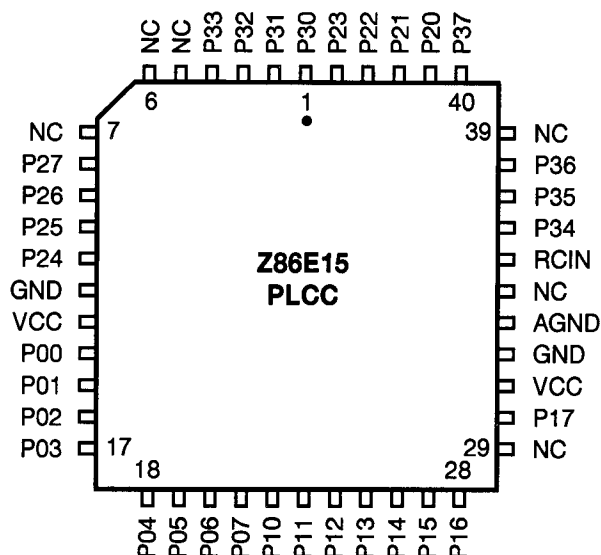
**Notes:**

\*Pin 5 and 6 used for testing Ground during normal operation.  
 When Pin 5 is connected to  $V_{cc}$ , Pin 6 is CLK OUT.  
 When Pin 5 is connected to GND, Pin 6 outputs nothing.  
 These pins must be tied to ground in application.

**Figure 2. 40-Pin DIP Configuration****Table 1. 40-Pin DIP Pin Identification**

Pin #	Symbol	Function	Direction
1-4	P30-P33	Port 3, Pins 0,1,2,3	Input
5-6	NC	Tied to GND	
7-10	P27-P24	Port 2, Pins 7,6,5,4	In/Output
11	GND	Ground	
12	$V_{cc}$	Power Supply	Input
13-20	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7	Output
21-28	P10-P17	Port 1, Pins 0,1,2,3,4,5,6,7	Output
29	$V_{cc}$	Power Supply	
30	GND	Ground	
31	AGND	Analog Ground	
32	RCIN	RCIN	Input
33-36	P34-P37	Port 3, Pins 4,5,6,7	Output
37-40	P20-P23	Port 2, Pins 0,1,2,3	Input

# PIN DESCRIPTION (Continued)



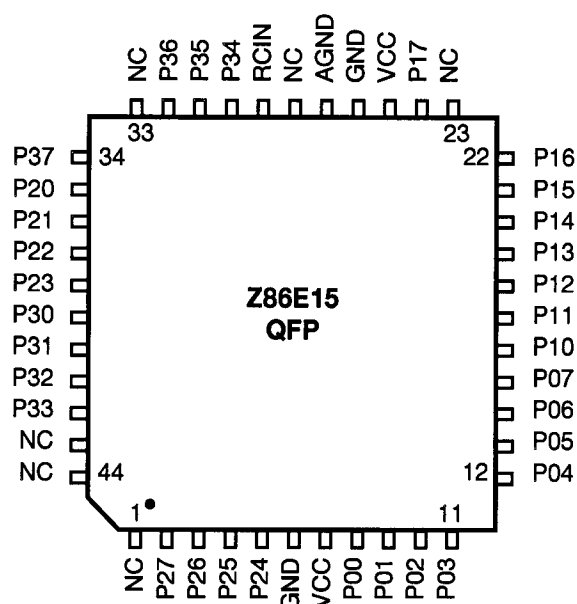
## Notes:

Pins 5 and 6 used for testing. Ground during normal operation  
When Pin 43 is connected to  $V_{cc}$ , Pin 44 is CLKOUT.  
When Pin 43 is connected to GND. Pin 44 outputs nothing.

Figure 3. 44-Pin PLCC Pin Assignments

Table 2. 44-Pin PLCC Pin Assignments

Pin #	Symbol	Function	Direction
1-4	P30-P33	Port 3, Pins 0,1,2,3	Input
5-7	NC	Test Pins (GND)	
8-11	P27-P24	Port 2, Pins 4,5,6,7	In/Output
12	GND	Ground	
13	$V_{cc}$	Power Supply	
14-21	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7	Output
22-28	P10-P16	Port 1, Pins 0,1,2,3,4,5,6	Output
29	NC	Not Connected	
30	P17	Port 1, Pin 7	Output
31	$V_{cc}$	Power Supply	
32	GND	Ground	
33	AGND	Analog Ground	
34	NC	Not Connected	
35	RCIN	RCIN	Input
36-38	P34-P36	Port 3, Pins 4,5,6,7	Output
39	NC	Not Connected	
40	P37	Port 3, Pin 7	Output
41-44	P20-P23	Port 2, Pins 0,1,2,3	In/Output

**Notes:**

Pins 43 and 44 are used for testing ground during normal operation.

When Pin 45 is connected to  $V_{cc}$ , Pin 46 is CLKOUT.

When Pin 45 is connected to GND. Pin 46 outputs nothing.

**Figure 4. 44-Pin QFP Pin Assignments****Table 3. 44-Pin QFP Pin Identification**

Pin #	Symbol	Function	Direction
1	NC	Not Connected	
2-5	P24-P27	Port 2, Pins 4,5,6,7	In/Output
6	GND	Ground	
7	$V_{cc}$	Supply Voltage	
8-15	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7,	Output
16-22	P10-P16	Port 1, Pins 0,1,2,3,4,5,6	Output
23	NC	Not Connected	
24	P17	Port 1, Pin 7	Output
25	$V_{cc}$	Supply Voltage	
26	GND	Ground	
27	AGND	Analog Ground	
28	NC	Not Connected	
29	RCIN	RCIN	Input
30-32	P34-P36	Port 3, Pins 4,5,6	Output
33	NC	Not Connected	
34	P37	Port 3, Pin 7	Output
35-38	P20-P23	Port 2, Pins 0,1,2,3	Input
39-42	P30-P33	Port 3, Pins 0,1,2,3	Input
43-44	NC	Test Pins (GND)	

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V <sub>CC</sub>	Supply Voltage*	−0.3	+7.0	V
T <sub>STG</sub>	Storage Temp	−65	+150	°C
T <sub>A</sub>	Oper Ambient Temp	0	+105	°C

**Note:** \* Voltage on all pins with respect to GND.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed here apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 5).

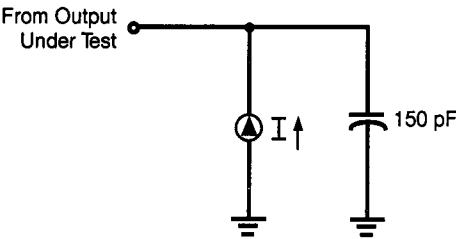


Figure 5. Test Load Diagram

CAPACITANCE

T<sub>A</sub> = 25°C; V<sub>CC</sub> = GND = 0V; f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Max
Input Capacitance	12 pF
Output Capacitance	12 pF
I/O Capacitance	12 pF

Frequency tolerance ±10%

**DC CHARACTERISTICS** $V_{CC} = 5.0V \pm 10\% @ 0^{\circ}C \text{ to } +70^{\circ}C$ 

Sym	Parameter	Min	Max	Typ*	Unit	Condition
$V_{CH}$	Clock Input High Voltage	$0.7 V_{CC}$	$V_{CC} + 0.3V$	2.5	V	Driven by External Clock Generator
$V_{CL}$	Clock Input Low Voltage	$GND - 0.3$	$0.2 V_{CC}$	1.5	V	Driven by External Clock Generator
$V_{IH}$	Input High Voltage	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V	
$V_{IL}$	Input Low Voltage	$GND - 0.3$	$0.2 V_{CC}$	1.5	V	
$V_{OH}$	Output High Voltage	$V_{CC} - 0.4$		4.7	V	$I_{OH} = -2.0 \text{ mA}$ (Port 2 out. in P/P Mode)
$V_{OH}$	Output High Voltage	$V_{CC} - 0.6$			V	$I_{OH} = -2.0 \text{ mA}$ (see note 1 below.)
$V_{OH}$	Output High Voltage	$V_{CC} - 1.0$			V	$I_{OH} = -2.0 \mu A$ (Port 0 and Port 1)
$V_{OL}$	Output Low Voltage		.4		V	$I_{OL} = 4 \text{ mA}$
$V_{OL}$	Output Low Voltage		.8		V	$I_{OL} = 4 \text{ mA}$ (see note 1 below.)
$I_{OL}$	Output Low	10	20		mA	$V_{OL} = V_{CC} - 2.2 \text{ V}$ (see note 1, 2 below.)
$I_{OL}$	Output Leakage	-1	1	<1	$\mu A$	$V_{IN} = 0V, 5.25V$
$I_{CC}$	$V_{CC}$ Supply Current		12	6	mA	@ 5.0 MHz
$I_{CC1}$	HALT Mode Current			2	mA	@ 5.0 MHz
$I_{CC2}$	STOP Mode Current		10		$\mu A$	
$R_p$	Pull Up Resistor	6.76	14.04	10.4	Kohm	Port 20-25 and Port 30-33
$R_p$	Pull Up Resistor (P26-P27) (P0 & P1)	1.8 200	3 500	2.4	Kohm Kohm	

**Notes:**

\* Typical @ 25°C

1. Ports P37-P34. These may be used for LEDs or as general-purpose outputs requiring high sink current.
2.  $V_{CC} = 5.0V \pm 5\% @ 0^{\circ}C \text{ to } +70^{\circ}C$

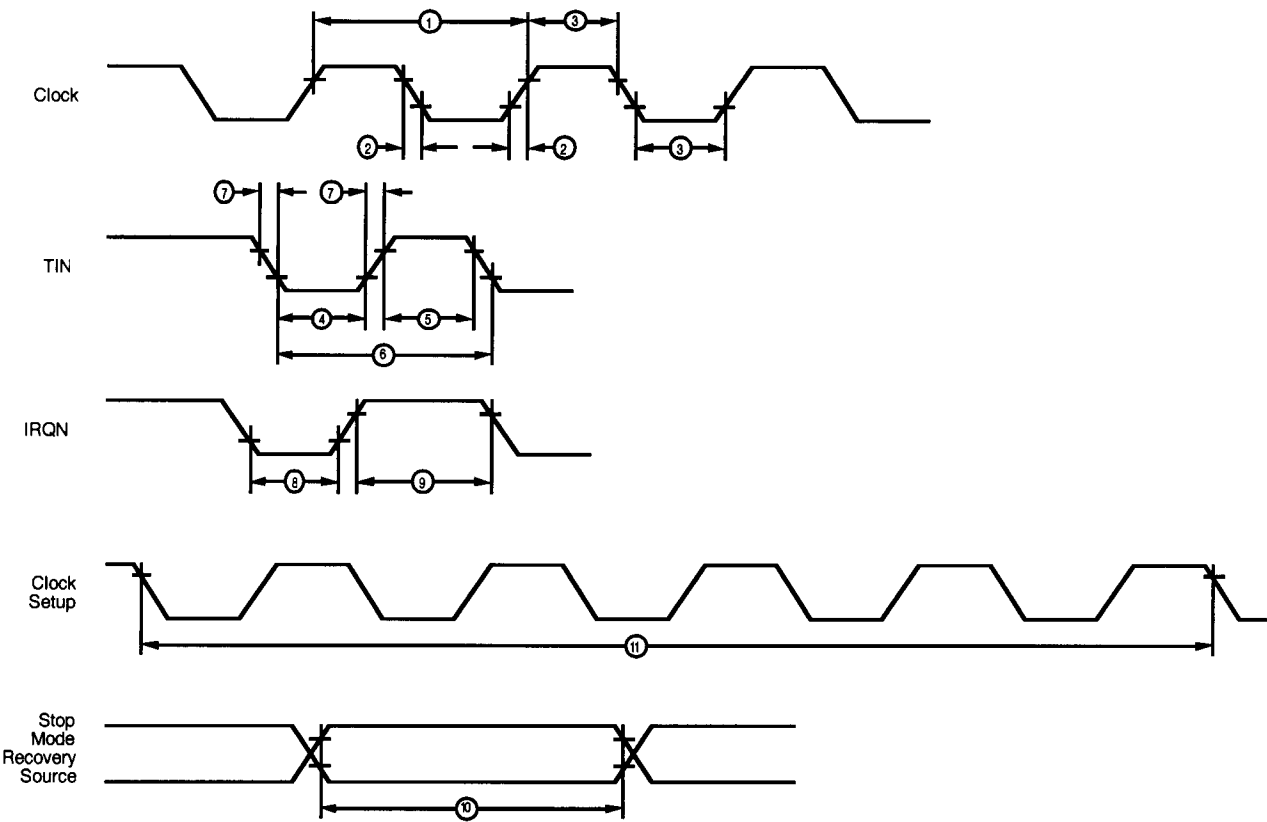


Figure 6. Additional Timing

## PIN FUNCTIONS

**RCIN.** A precision resistor is connected between this pin and the power supply to form the precision RC oscillator.

**CLKOUT.** This pin is the system clock of the Z8® and runs at the frequency of the RC oscillator (Test only).

**Port 0 (P07-P00).** Port 0 is an 8-bit, CMOS-compatible open-drain output (Figure 7).

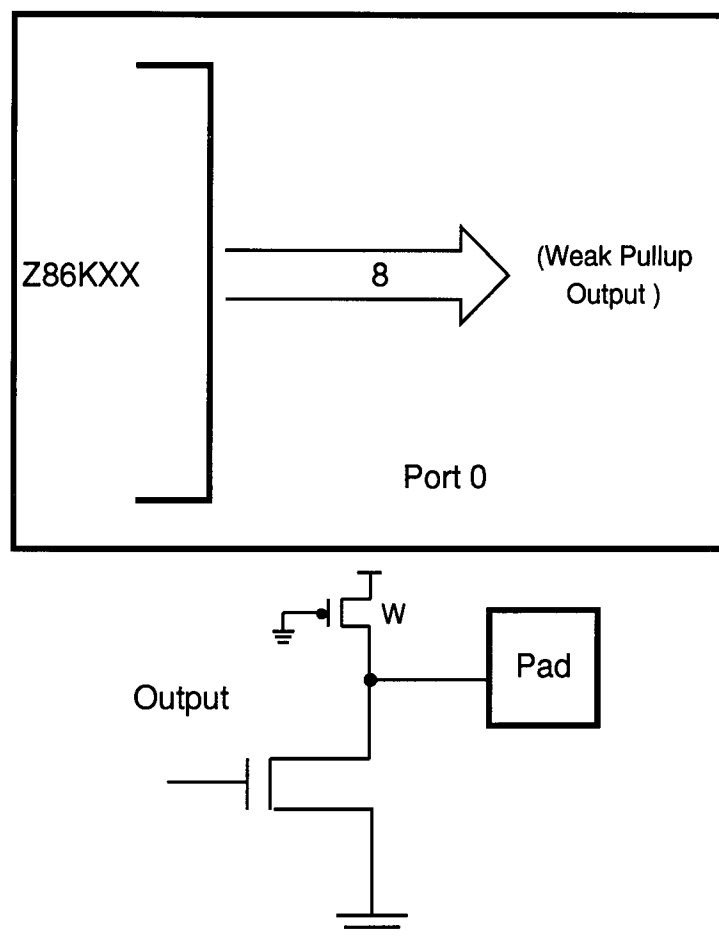


Figure 7. Port 0 Configuration



## PIN FUNCTIONS (Continued)

**Port 2 (P27-P20).** Port 2 is an 8-bit, CMOS-compatible Port with 4-bit input, 4-bit programmable I/O (Figure 9).

P20-P25 have 10.4K ( $\pm 35\%$ ) pull-up resistors. P26-P27 have 2.4K ( $\pm 25\%$ ) pull-up resistors.

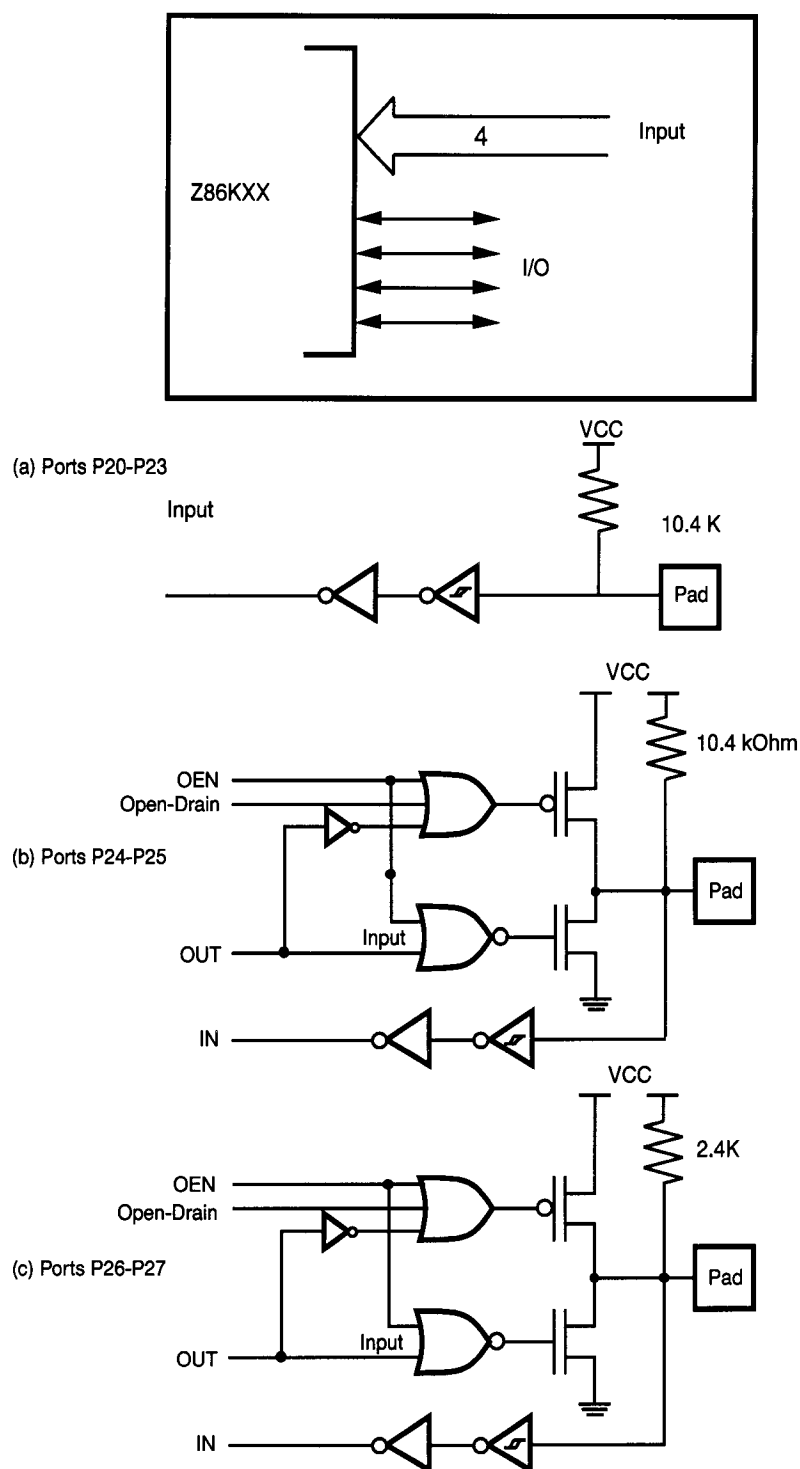
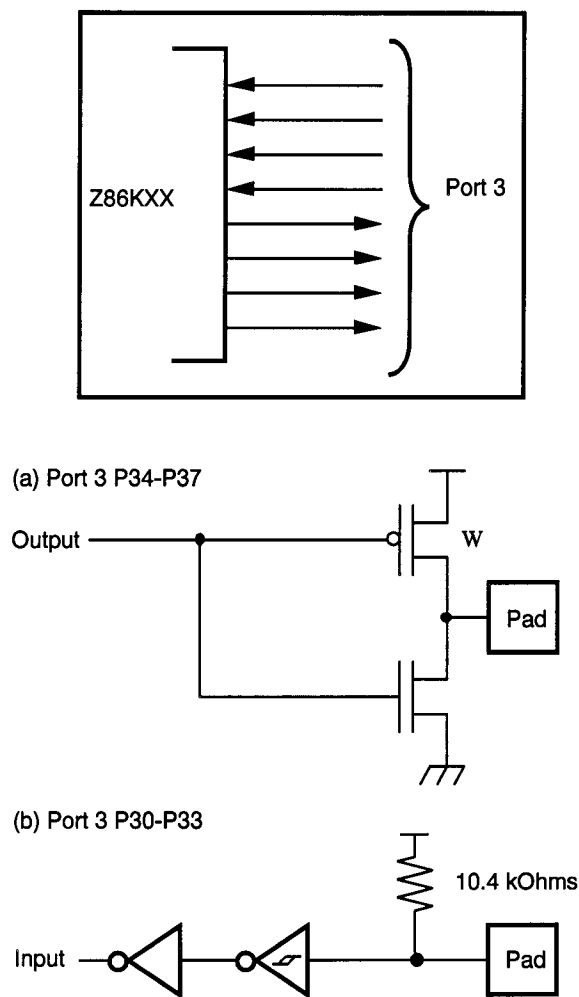


Figure 9. Port 2 Configuration

**Port 3** (P37-P30). Port 3 is an 8-bit, CMOS-compatible four-fixed input (P33-P30) and four-fixed output (P37-P34) I/O port. Port 3 inputs have 10.4 Kohm pull-up resistors. Outputs are capable of directly driving LED.

Port 3 is configured under software control to provide four external interrupt request signals (IRQ0-IRQ3).



**Figure 10. Port 3 Configuration**

## PIN FUNCTIONS (Continued)

**Program Memory.** The 16-bit program counter addresses 4 KB of program memory space at internal locations (Figure 11).

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations have six 16-bit vectors that correspond to the five available interrupts.

Byte 12 to byte 4095 consists of on-chip, mask programmed ROM. Addresses 4096 and greater are reserved.

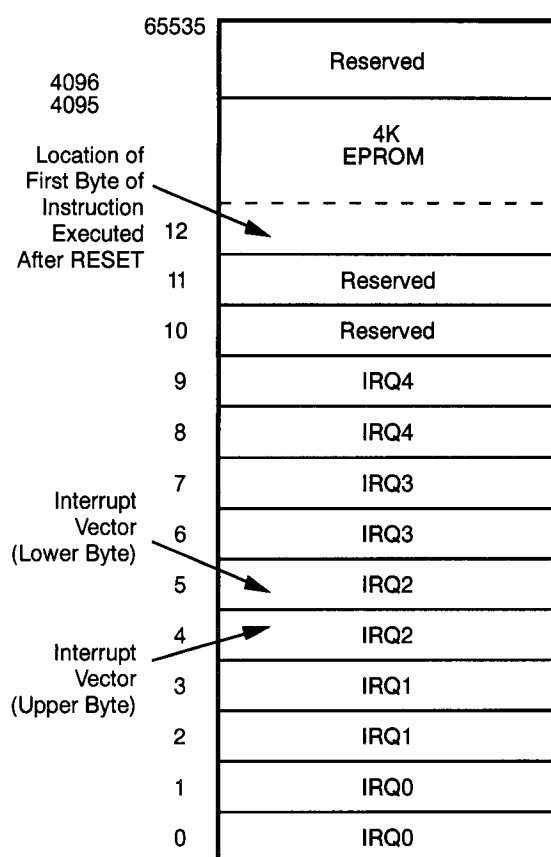


Figure 11. Program Memory Map

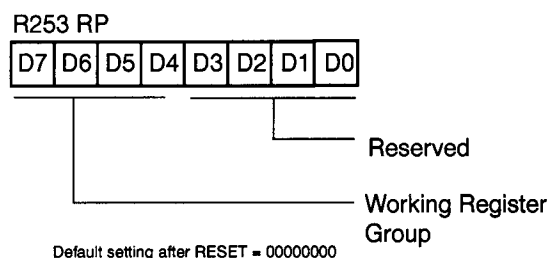


Figure 12. Register Pointer Register

**Register File.** The register file (Figure 13) consists of four I/O port registers, 188 general-purpose registers (excluding P00-P03), and 11 control and status registers (R3-R0, R191-R4, and R255-R240, respectively). The instructions can access registers directly or indirectly through an 8-bit address field. This allows short, 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into nine working-register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

LOCATION		IDENTIFIERS
R255	Stack Pointer (Bits 7-0)	SPL
R254	Reserved	
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Reserved	
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PREQ
R244	Timer/Counter0	T0
R243	Reserved	
R242	Reserved	
R241	Timer Mode	TMR
R240	Reserved	
	Not Implemented	
R 191	General-Purpose Registers	
R4		
R3	Port 3	P3
R2	Port 2	P2
R1	Port 1	P1
R0	Port 0	P0

Note: \* Will not be reset with a STOP Mode Recovery.

Figure 13. Register File Configuration

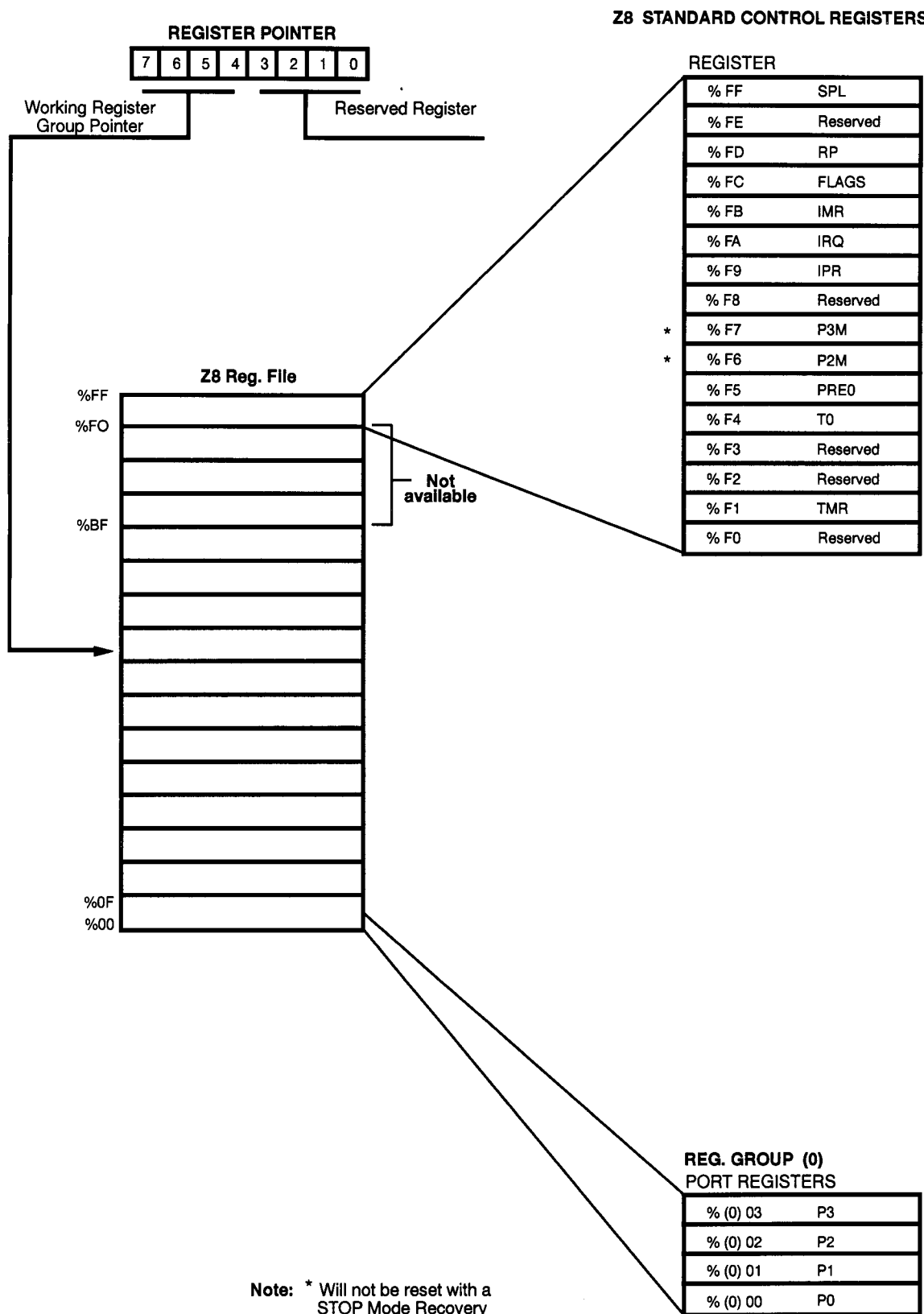


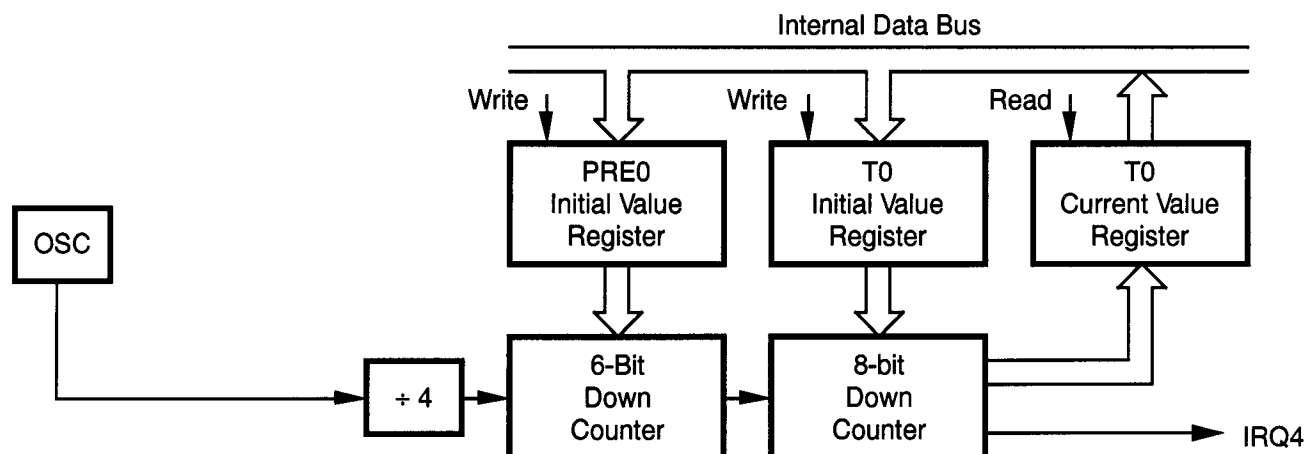
Figure 14. Register File Architecture

**PIN FUNCTIONS** (Continued)

**Counter/Timers.** There is an 8-bit programmable counter/timer (T0) driven by its own 6-bit programmable prescaler (Figure 15).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. The prescaler drives its counter, which decrements the value (1 to 256) on the prescaler overflow. When both the counter and prescaler reach the end of count, a timer interrupt request, IRQ4, is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counter can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode). The counter, but not the prescaler, is read at any time without disturbing its value or count mode.



**Figure 15. Counter/Timers Block Diagram**

**Interrupts.** The Z86E15 has five different interrupts from five different sources. These interrupts are maskable and prioritized (Figure 16). The five sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and the other is claimed by the counter/timer. The Interrupt Masked Register globally or individually enables or disables the five interrupts requests.

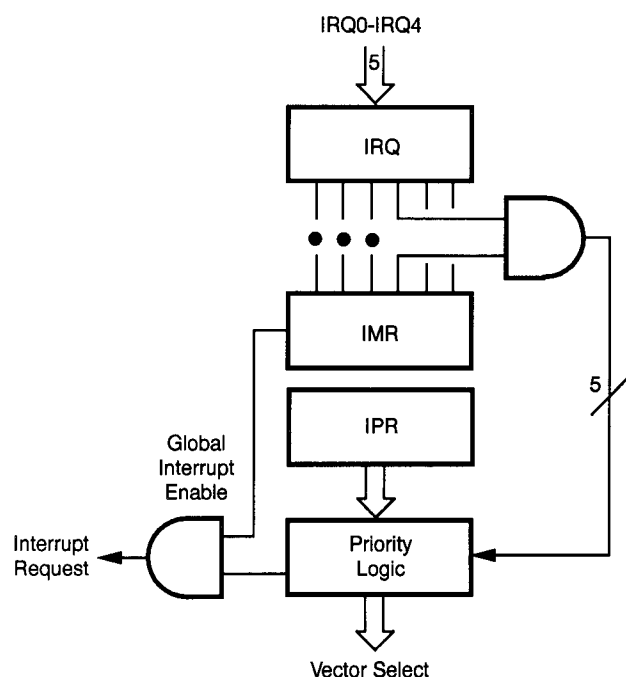


Figure 16. Interrupt Block Diagram

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and status flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt request needs service.

**RC Oscillator.** The Z86E15 provides an internal capacitor to accommodate an RC oscillator configuration. A 1% precision resistor is necessary to achieve  $\pm 10\%$  accurate frequency oscillation.

The Z86E15 also accepts external clock from (RCIN) with (AGND) connected to  $V_{CC}$  (Figure 17).

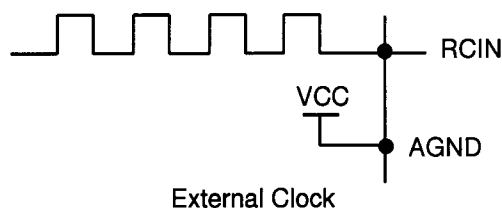
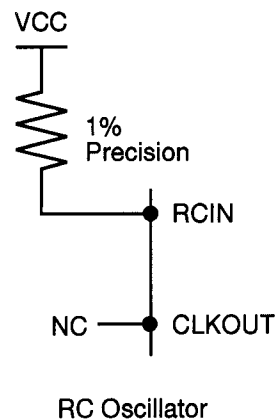


Figure 17. RC Oscillator Configuration

## PIN FUNCTIONS (Continued)

**Watch-Dog Timer.** The Watch-Dog Timer (WDT) is activated automatically by power-on if it is enabled in the Mask Option. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is driven by the system clock. It must be refreshed at least once during each time cycle by executing the WDT instruction. WDT can be enabled by Mask Option. (Figure 18)

**WDT Hot bit.** Bit 7 of the Interrupt Request register (IRQ register FAH) determines whether a hot start or cold start occurred. A cold start is defined as reset occurring from

power-up of the Z86E15 (the default upon power-up is 0). A hot start occurs when a WDT time-out has occurred (bit 7 is set to 1). Bit 7 of the IRQ register is read-only and is automatically reset to 0 when read.

**Watch-Dog Timer .** The WDT time-out is  $\frac{294912 \text{ ms}}{f(\text{Hz})}$ .

**WDT During HALT (D5-R250).** This bit determines whether or not the WDT is active during HALT Mode. The default is 1, and a 1 indicates active during HALT.

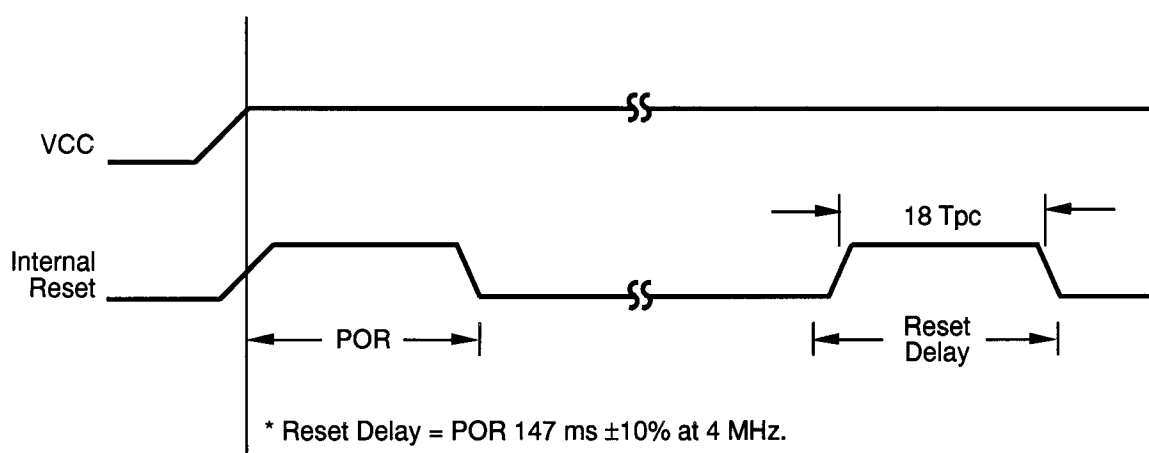
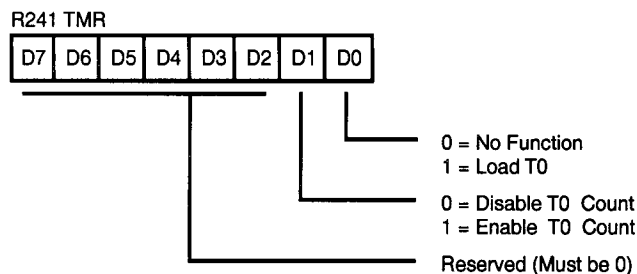
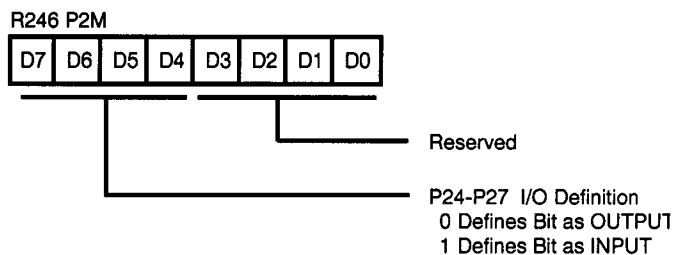


Figure 18. WDT Turn-On Timing After Reset

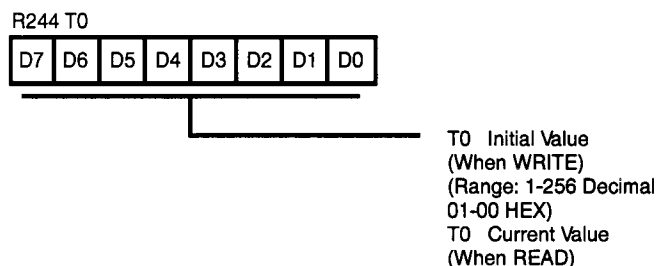
## Z8® CONTROL REGISTER DIAGRAMS



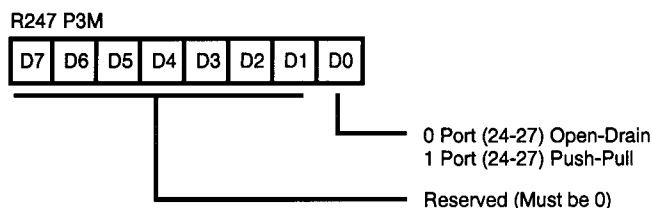
**Figure 21. Timer Mode Register**  
(F1<sub>H</sub>: Read/Write)



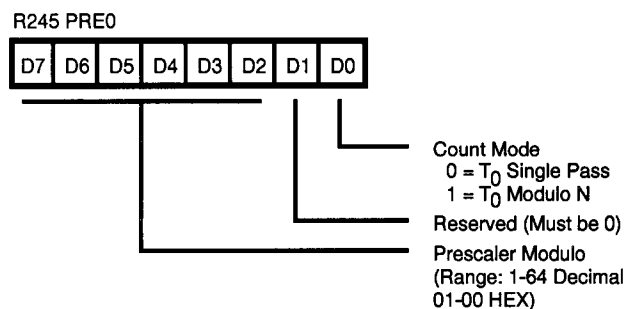
**Port 2 Mode Register**  
**Figure 24. (F6<sub>H</sub>: Write Only)**



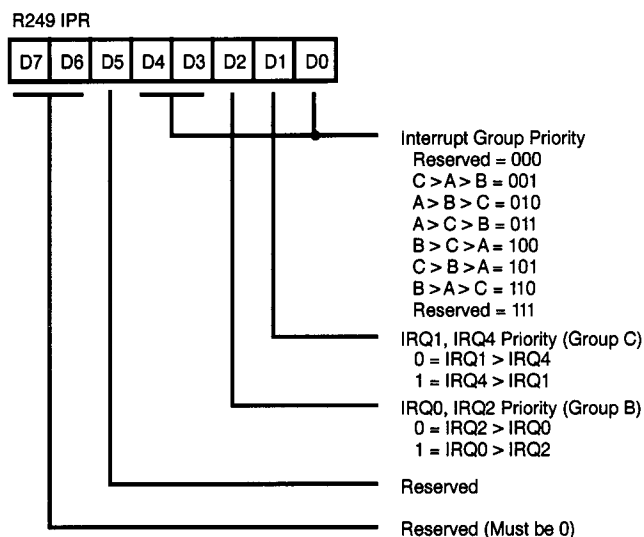
**Counter/Timer 0 Register**  
**Figure 22. (F4<sub>H</sub>: Read/Write)**



**Port 2 Open Drain Mode Register**  
**Figure 25. (F7<sub>H</sub>: Write Only)**



**Prescaler 0 Register**  
**Figure 23. (F5<sub>H</sub>: Write Only)**



**Figure 26. Interrupt Priority Register**  
(F9<sub>H</sub>: Write Only)



## PROGRAMMING

### Signals Required for E15 EPROM

The TEST1 pin will be used as a high voltage pin. The high voltage from this pin will be used to program the EPROM. It will also need to be at high voltage in order for any EPROM operation to be done. When this pin is at high voltage, then an internal signal  $V_{pph}$  is generated from the high voltage detect circuitry and the signal being active will be used to multiplex the remaining pins that are required in all the EPROM operations.

#### TEST1 ( $V_{pp}$ )

This pin is designated a high voltage pin on the Z86E15. All EPROM operations will require a high voltage on this pin. The  $V_{pp}$  supplies the high voltage for the programming of the EPROM.

**Note:** The pins listed below are based on the condition that the  $V_{pp}$  is in high voltage.

#### P33 (Mode Latch)

The Z86E15 utilizes this pin when high will be used to latch the mode. This condition will only happen when the  $V_{pph}$  is active.

#### P32 (Oeb-Output Enable)

This regular pin controls the direction of the data bus. The signal generated goes into the EPROM as the precharge signal.

When this signal is low, the data is output from the EPROM. When the signal is high, data is input to the EPROM.

When the signal is high, the EPROM is precharged. When the signal is low, the EPROM is evaluated.

#### P31 (EPMH)

This regular pin is used to read the option bits when the EPROM is protected.

When the signal is high, during POR, the option bits can be read from the EPROM.

#### P30 (Volt\_Clamp)

This regular pin used the signal to disable the voltage clamp circuit.

When the signal is low, the voltage clamp circuit is enabled. When the signal is high, the voltage clamp circuit is disabled and margin testing can be done.

#### P20 (CEb)

This regular pin on the Z86E15 is the chip enable signal for the EPROM. This signal will be input to the EPROM when  $V_{pph}$  is high. This is an active low signal.

#### P21 (PGMb-Program Mode)

This regular pin on the Z86E15 allows the EPROM to be programmed when the signal is logic low, and when the signal  $V_{pph}$  is high. The data on the databus will be programmed into the location that is addressed by the internal counter that generates the address for the EPROM.

#### P22 (epadr\_clk) and P23 (epadr\_rst)

The address is generated by an internal address counter which is clocked through the signal epadr\_clk. Each clock increments the counter by one. The counter can be reset to zero by the epadr\_rst signal. Both epadr\_clk and epadr\_rst are external signals.

The epadr\_rst signal is an active high signal.

### Data to the EPROM

The data to the EPROM are multiplexed with the pins as shown below in Figure 32: (Data <7.0>)

Data	Pin
D0	P34
D1	P35
D2	P36
D3	P37
D4	P27
D5	P26
D6	P25
D7	P24

Figure 32. Data Pin Assignments

### Option Bit Programming

In order to program the option bits, the Mode 3 should be used. This can be done as follows:

- The  $V_{pp}$  pin is set to high voltage (device pin TEST1 is driven to high voltage).
- The epadr\_rst signal is driven high for one cycle to reset the address counter (device pin P23).
- Three clocks are given on the epadr\_clk pin (P22), which will advance the counter to the count of 3.
- The Mode Latch signal (P33) is driven high for one cycle to latch in the data into the Mode Register.
- The address counter is again reset and the required data is programmed into location 0, which will program the 8 locations of the option bits. In the Z86E15, bits 0, 1 and 2 will be used as there are only 3 option bits for this device.

## PACKAGE INFORMATION

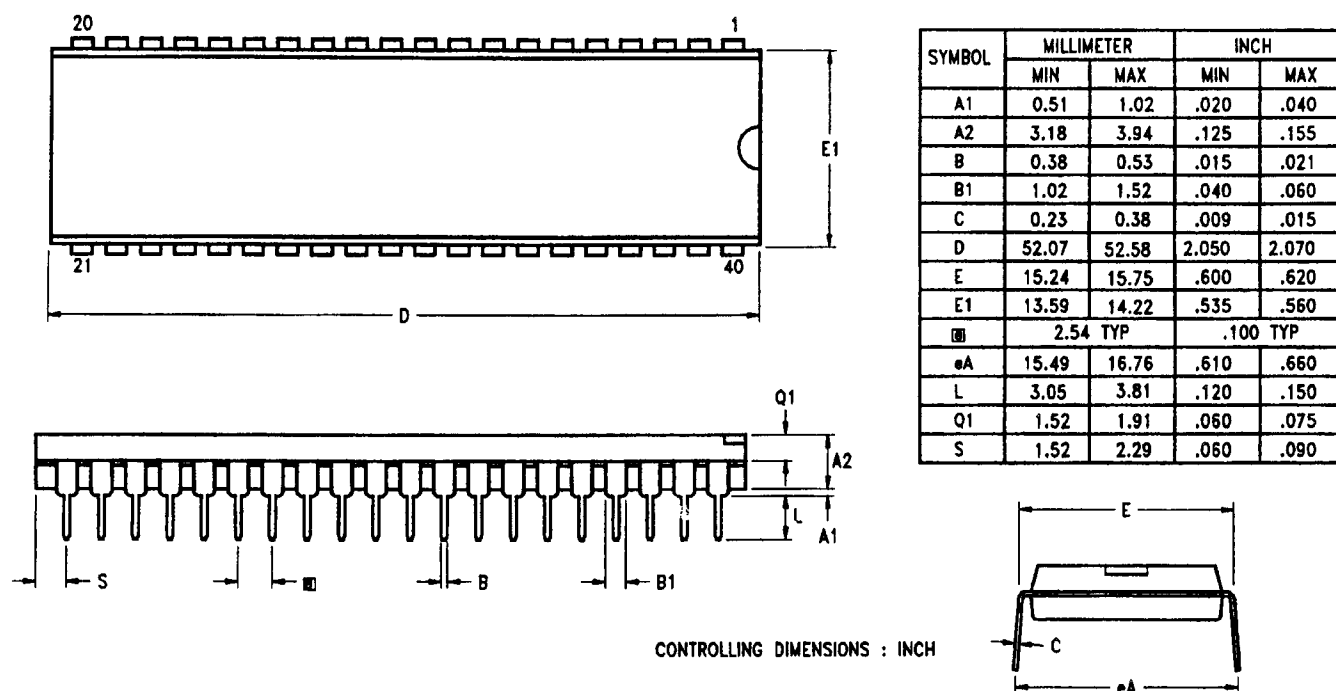


Figure 33. 40-Pin DIP Package Diagram

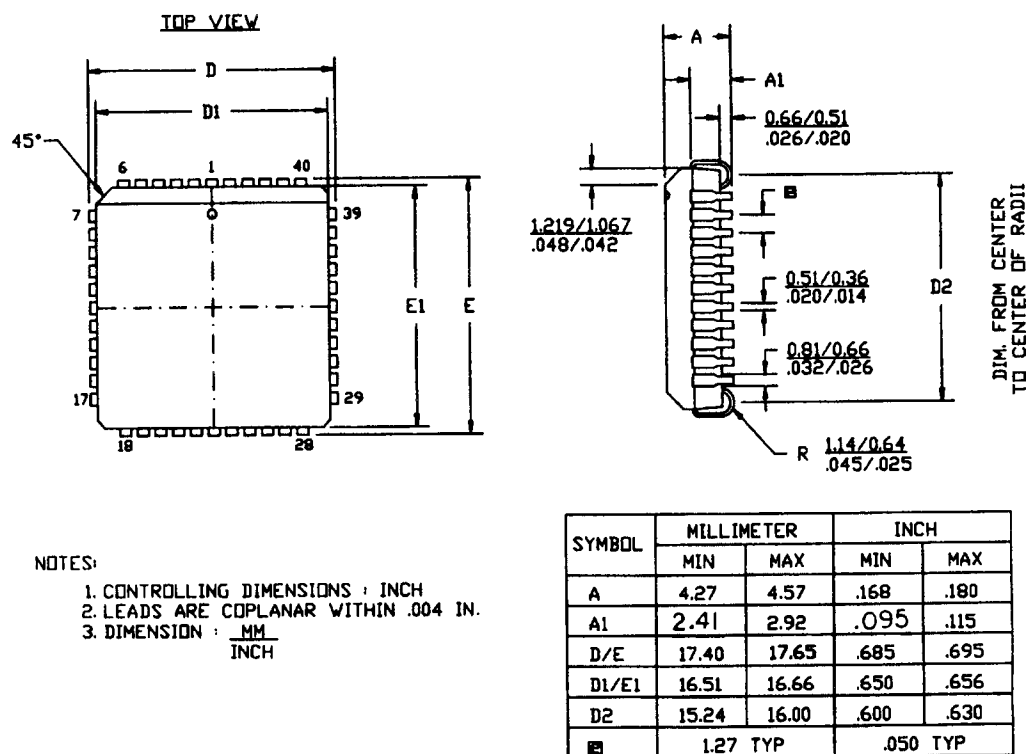


Figure 34. 44-Pin PLCC Package Diagram

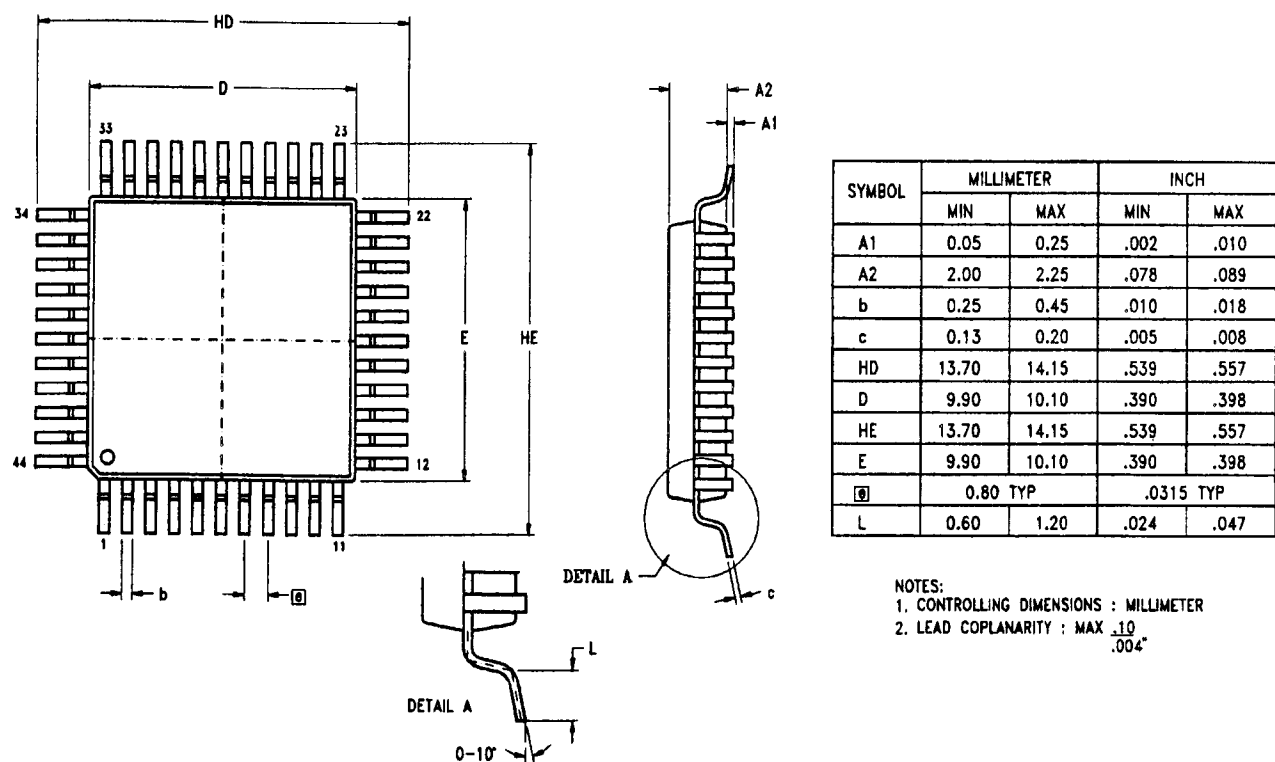


Figure 35. 44-Pin QFP Package Diagram

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**ORDERING INFORMATION**

5 MHz  
40-Pin DIP  
Z86E1505PSC

5 MHz  
44-Pin PLCC  
Z86E1505VSC

5 MHz  
44-Pin QFP  
Z86E1505FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

---

**CODES****Package**

P = Plastic DIP  
V = Plastic Leaded Chip Carrier  
F = Quad Flat Pack

**Speed**

05 = 5 MHz

**Environmental**

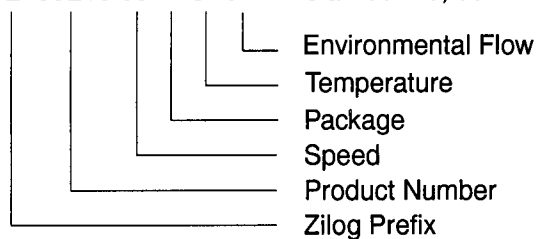
C = Plastic Standard

**Temperature**

S = 0°C to +70°C

**Example:**

Z 86E15 05 P S C is a Z86E15, 05 MHz, DIP, 0° to +70°C, Plastic Standard Flow



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**Development Projects:**

Customer is cautioned that while reasonable efforts will be employed to meet performance objectives and milestone dates, development is subject to unanticipated problems

and delays. No production release is authorized or committed until the Customer and Zilog have agreed upon a Customer Procurement Specification for this project.

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**Pre-Characterization Product:**

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found,

either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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**Low Margin:**

Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on

Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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