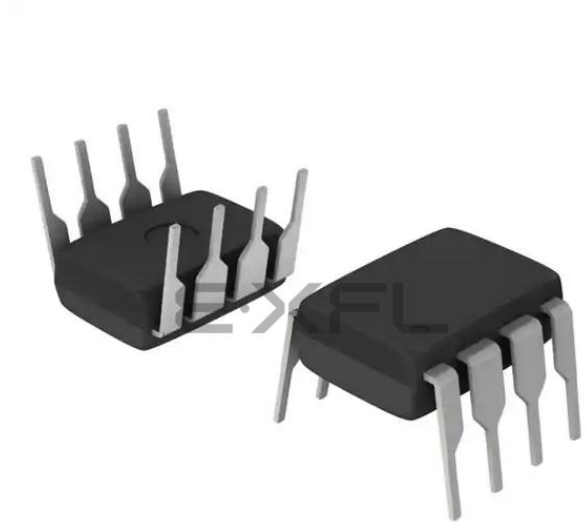


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f635-e-p

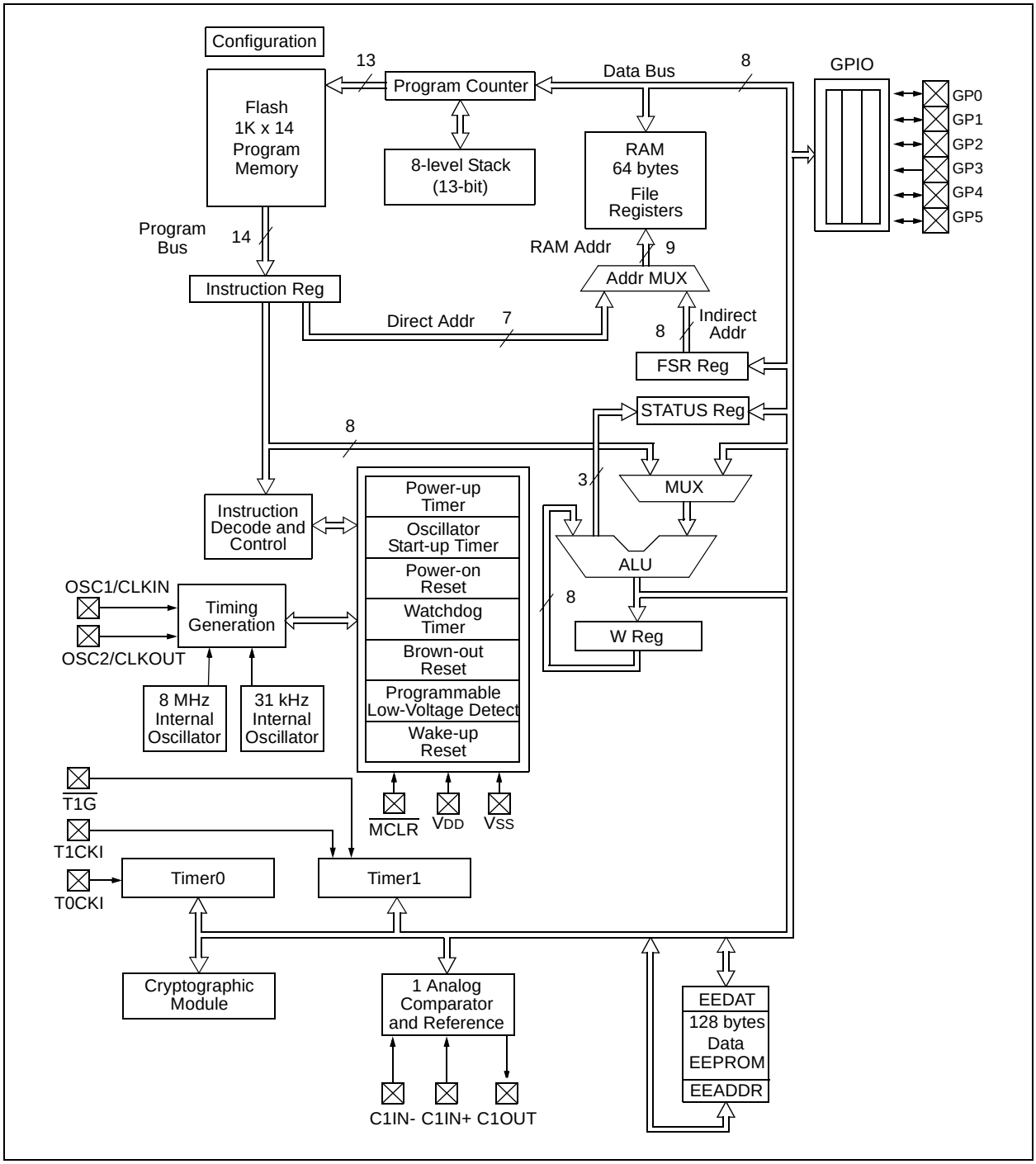
1.0 DEVICE OVERVIEW

This document contains device specific information for the PIC12F635/PIC16F636/639 devices.

Block Diagrams and pinout descriptions of the devices are as follows:

- PIC12F635 (Figure 1-1, Table 1-1)
- PIC16F636 (Figure 1-2, Table 1-2)
- PIC16F639 (Figure 1-3, Table 1-3)

FIGURE 1-1: PIC12F635 BLOCK DIAGRAM



NOTES:

5.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (shared with Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow

Figure 5-1 is a block diagram of the Timer0 module.

5.1 Timer0 Operation

When used as a timer, the Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

5.1.1 8-BIT TIMER MODE

When used as a timer, the Timer0 module will increment every instruction cycle (without prescaler). Timer mode is selected by clearing the T0CS bit of the OPTION register to '0'.

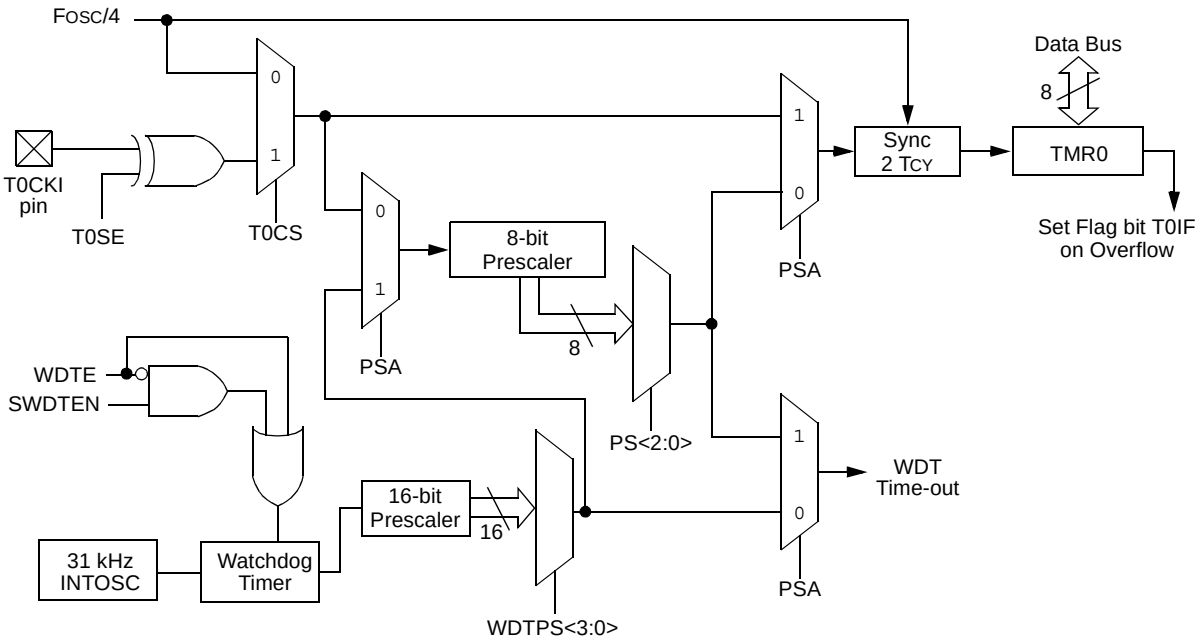
When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note:	The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

5.1.2 8-BIT COUNTER MODE

When used as a counter, the Timer0 module will increment on every rising or falling edge of the T0CKI pin. The incrementing edge is determined by the T0SE bit of the OPTION register. Counter mode is selected by setting the T0CS bit of the OPTION register to '1'.

FIGURE 5-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.
2: SWDTEN and WDTPS<3:0> are bits in the WDTCON register.
3: WDTE bit is in the Configuration Word register.

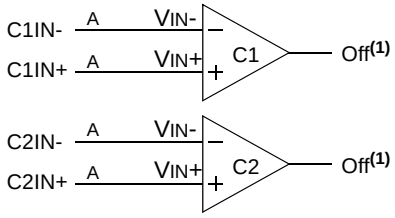
TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	00-- --10
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIE1	EEIE	LVDIE	CRIE	C2IE(1)	C1IE	OSFIE	—	TMR1IE	000- 00-0	000- 00-0
PIR1	EEIF	LVDIF	CRIF	C2IF(1)	C1IF	OSFIF	—	TMR1IF	000- 00-0	000- 00-0
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu

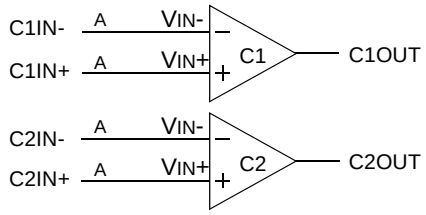
Legend: x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.
Note 1: PIC16F636/639 only.

FIGURE 7-7: COMPARATOR I/O OPERATING MODES (PIC16F636/639)

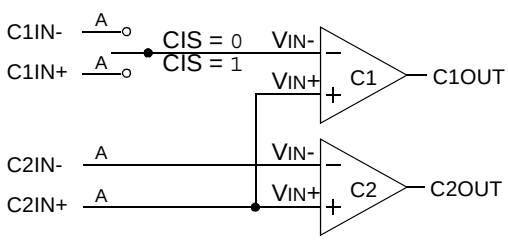
Comparators Reset (POR Default Value)
CM<2:0> = 000



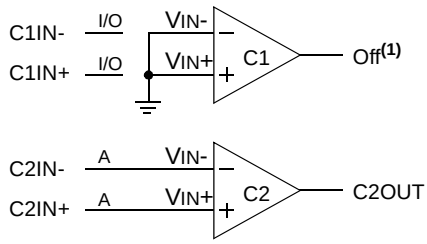
Two Independent Comparators
CM<2:0> = 100



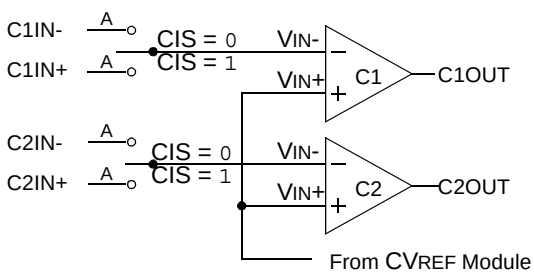
Three Inputs Multiplexed to Two Comparators
CM<2:0> = 001



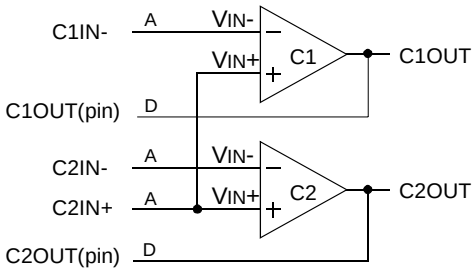
One Independent Comparator
CM<2:0> = 101



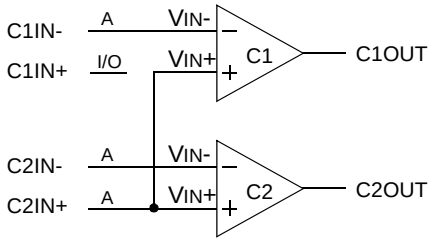
Four Inputs Multiplexed to Two Comparators
CM<2:0> = 010



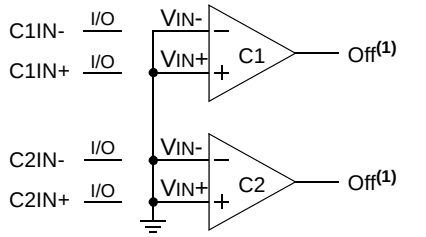
Two Common Reference Comparators with Outputs
CM<2:0> = 110



Two Common Reference Comparators
CM<2:0> = 011



Comparators Off (Lowest Power)
CM<2:0> = 111



Legend: A = Analog Input, ports always reads '0'
CIS = Comparator Input Switch (CMCON0<3>)
I/O = Normal port I/O
D = Comparator Digital Output

Note 1: Reads as '0', unless CxINV = 1.

FIGURE 7-8: COMPARATOR INTERRUPT TIMING W/O CMCON0 READ

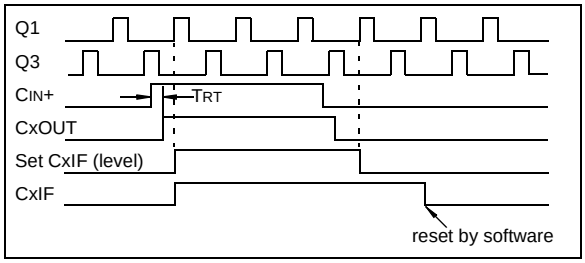
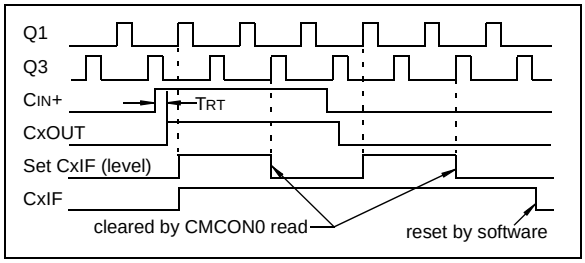


FIGURE 7-9: COMPARATOR INTERRUPT TIMING WITH CMCON0 READ



Note 1: If a change in the CMCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF of the PIR1 register interrupt flag may not get set.

2: When either comparator is first enabled, bias circuitry in the Comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 µs for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

REGISTER 7-2: CMCON0: COMPARATOR CONFIGURATION REGISTER (PIC16F636/639)

R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **C2OUT:** Comparator 2 Output bit

When C2INV = 0:
1 = C2 V_{IN}+ > C2 V_{IN}-
0 = C2 V_{IN}+ < C2 V_{IN}-

When C2INV = 1:
1 = C2 V_{IN}+ < C2 V_{IN}-
0 = C2 V_{IN}+ > C2 V_{IN}-

bit 6 **C1OUT:** Comparator 1 Output bit

When C1INV = 0:
1 = C1 V_{IN}+ > C1 V_{IN}-
0 = C1 V_{IN}+ < C1 V_{IN}-

When C1INV = 1:
1 = C1 V_{IN}+ < C1 V_{IN}-
0 = C1 V_{IN}+ > C1 V_{IN}-

bit 5 **C2INV:** Comparator 2 Output Inversion bit

1 = C2 output inverted
0 = C2 output not inverted

bit 4 **C1INV:** Comparator 1 Output Inversion bit

1 = C1 Output inverted
0 = C1 Output not inverted

bit 3 **CIS:** Comparator Input Switch bit

When CM<2:0> = 010:

1 = C1IN+ connects to C1 V_{IN}-
C2IN+ connects to C2 V_{IN}-
0 = C1IN- connects to C1 V_{IN}-
C2IN- connects to C2 V_{IN}-

When CM<2:0> = 001:
1 = C1IN+ connects to C1 V_{IN}-
0 = C1IN- connects to C1 V_{IN}-

bit 2-0 **CM<2:0>:** Comparator Mode bits (See Figure 7-5)

000 = Comparators off. CxIN pins are configured as analog
001 = Three inputs multiplexed to two comparators
010 = Four inputs multiplexed to two comparators
011 = Two common reference comparators
100 = Two independent comparators
101 = One independent comparator
110 = Two comparators with outputs and common reference
111 = Comparators off. CxIN pins are configured as digital I/O

9.5 Protection Against Spurious Write

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (nominal 64 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:

- Brown-out
- Power Glitch
- Software Malfunction

9.6 Data EEPROM Operation During Code Protection

Data memory can be code-protected by programming the CPD bit in the Configuration Word (Register 12-1) to '0'.

When the data memory is code-protected, the CPU is able to read and write data to the data EEPROM. It is recommended to code-protect the program memory when code-protecting data memory. This prevents anyone from programming zeroes over the existing code (which will execute as NOPs) to reach an added routine, programmed in unused program memory, which outputs the contents of data memory. Programming unused locations in program memory to '0' will also help prevent data memory code protection from becoming breached.

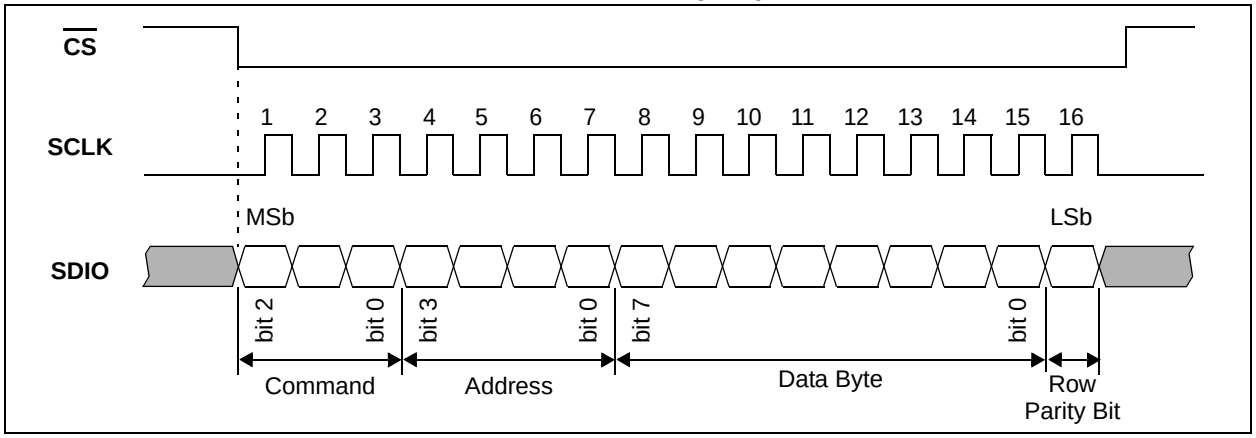
TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH DATA EEPROM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIR1	EEIF	LVDIF	CRIF	C2IF(1)	C1IF	OSFIF	—	TMR1IF	0000 00-0	0000 00-0
PIE1	EEIE	LVDIE	CRIE	C2IE(1)	C1IE	OSFIE	—	TMR1IE	0000 00-0	0000 00-0
EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
EEADR	EEADR7(1)	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition.
Shaded cells are not used by the data EEPROM module.

Note 1: PIC16F636/639 only.

FIGURE 11-19: DETAILED SPI INTERFACE TIMING (AFE)



11.32.2.1 Clamp On Command

This command results in activating (turning on) the modulation transistors of all enabled channels; channels enabled in Configuration Register 0 (Register 11-1).

11.32.2.2 Clamp Off Command

This command results in de-activating (turning off) the modulation transistors of all channels.

11.32.2.3 Sleep Command

This command places the AFE in Sleep mode – minimizing current draw by disabling all but the essential circuitry. Any other command wakes the AFE (example: Clamp Off command).

11.32.2.4 Soft Reset Command

The AFE issues a Soft Reset when it receives an external Soft Reset command. The external Soft Reset command is typically used to end a SPI communication sequence or to initialize the AFE for the next signal detection sequence, etc. See **Section 11.20 "Soft Reset"** for more details on Soft Reset.

If a Soft Reset command is sent during a "Clamp-on" condition, the AFE still keeps the "Clamp-on" condition after the Soft Reset execution. The Soft Reset is executed in Active mode only, not in Standby mode. The SPI Soft Reset command is ignored if the AFE is not in Active mode.

11.32.2.5 AGC Preserve On Command

This command results in preserving the AGC level during each AGC settling time and apply the value to the data slicing circuit for the following data stream. The preserved AGC value is reset by a Soft Reset, and a new AGC value is acquired and preserved when it starts a new AGC settling time. This feature is disabled by an AGC Preserve Off command (see **Section 11.19 "AGC Preserve"**).

11.32.2.6 AGC Preserve Off Command

This command disables the AGC preserve feature and returns the AFE to the normal AGC tracking mode, fast tracking during AGC settling time and slow tracking after that (see **Section 11.19 "AGC Preserve"**).

11.32.3 CONFIGURATION REGISTERS

The AFE includes 8 Configuration registers, including a column parity register and AFE Status Register. All registers are readable and writable via SPI, except STATUS register, which is readable only. Bit 0 of each register is a row parity bit (except for the AFE Status Register 7) that makes the register contents an odd number.

REGISTER 11-8: AFE STATUS REGISTER 7

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CHZACT	CHYACT	CHXACT	AGCACT	WAKEZ	WAKEY	WAKEX	ALARM	PEI
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8 **CHZACT**: Channel Z Active(1) bit (cleared via Soft Reset)
1 = Channel Z is passing data after TAGC
0 = Channel Z is not passing data after TAGC

bit 7 **CHYACT**: Channel Y Active(1) bit (cleared via Soft Reset)
1 = Channel Y is passing data after TAGC
0 = Channel Y is not passing data after TAGC

bit 6 **CHXACT**: Channel X Active(1) bit (cleared via Soft Reset)
1 = Channel X is passing data after TAGC
0 = Channel X is not passing data after TAGC

bit 5 **AGCACT**: AGC Active Status bit (real time, cleared via Soft Reset)
1 = AGC is active (Input signal is strong). AGC is active when input signal level is approximately > 20 mVPP range.
0 = AGC is inactive (Input signal is weak)

bit 4 **WAKEZ**: Wake-up Channel Z Indicator Status bit (cleared via Soft Reset)
1 = Channel Z caused a AFE wake-up (passed ÷64 clock counter)
0 = Channel Z did not cause a AFE wake-up

bit 3 **WAKEY**: Wake-up Channel Y Indicator Status bit (cleared via Soft Reset)
1 = Channel Y caused a AFE wake-up (passed ÷64 clock counter)
0 = Channel Y did not cause a AFE wake-up

bit 2 **WAKEX**: Wake-up Channel X Indicator Status bit (cleared via Soft Reset)
1 = Channel X caused a AFE wake-up (passed ÷64 clock counter)
0 = Channel X did not cause a AFE wake-up

bit 1 **ALARM**: Indicates whether an Alarm timer time-out has occurred (cleared via read "Status Register command")
1 = The Alarm timer time-out has occurred. It may cause the $\overline{\text{ALERT}}$ output to go low depending on the state of bit 4 of the Configuration register 0
0 = The Alarm timer is not timed out

bit 0 **PEI**: Parity Error Indicator bit – indicates whether a Configuration register parity error has occurred (real time)
1 = A parity error has occurred and caused the $\overline{\text{ALERT}}$ output to go low
0 = A parity error has not occurred

Note 1: Bit is high whenever channel is passing data. Bit is low in Standby mode.

See Table 11-7 for the bit conditions of the AFE Status Register after various SPI commands and the AFE Power-on Reset.

TABLE 11-7: AFE STATUS REGISTER BIT CONDITION (AFTER POWER-ON RESET AND VARIOUS SPI COMMANDS)

Condition	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CHZACT	CHYACT	CHXACT	AGCACT	WAKEZ	WAKEY	WAKEX	ALARM	PEI
POR	0	0	0	0	0	0	0	0	1
Read Command (STATUS Register only)	u	u	u	u	u	u	u	0	u
Sleep Command	u	u	u	u	u	u	u	u	u
Soft Reset Executed(1)	0	0	0	0	0	0	0	u	u

Legend: u = unchanged

Note 1: See **Section 11.20 "Soft Reset"** and **Section 11.32.2.4 "Soft Reset Command"** for the condition of Soft Reset execution.

TABLE 12-4: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset Wake-up Reset	$\overline{\text{MCLR}}$ Reset WDT Reset Brown-out Reset(1) Wake-up Reset	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1(3)
STATUS	03h/83h	0001 1xxx	000q quuu(4)	uuuq quuu(4)
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--xx xx00	--00 0000	--uu uu00
PORTC(6)	07h	--xx xx00	--00 0000	--uu uu00
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 000x	0000 000x	uuuu uuuu(2)
PIR1	0Ch	0000 00-0	0000 00-0	uuuu uu-u(2)
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	-uuu uuuu
WDTCON	18h	---0 1000	---0 1000	---u uuuu
CMCON0	19h	0000 0000	0000 0000	uuuu uuuu
CMCON1	1Ah	---- --10	---- --10	---- --uu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu 1uuu
TRISC(6)	87h	--11 1111	--11 1111	--uu 1uuu
PIE1	8Ch	0000 00-0	0000 00-0	uuuu uu-u
PCON	8Eh	--01 q-qq	--0u u-uu(1,5)	--0u u-uu
OSCCON	8Fh	-110 q000	-110 q000	-uuu uuuu
OSCTUNE	90h	---0 0000	---u uuuu	---u uuuu
WPUDA	95h	--11 -111	--11 -111	uuuu uuuu
IOCA	96h	--00 0000	--00 0000	--uu uuuu
WDA	97h	--11 -111	--11 -111	uuuu uuuu
VRCON	99h	0-0- 0000	0-0- 0000	u-u- uuuu
EEDAT	9Ah	0000 0000	0000 0000	uuuu uuuu
EEADR	9Bh	0000 0000	0000 0000	uuuu uuuu
EECON1	9Ch	---- x000	---- q000	---- uuuu
EECON2	9Dh	---- ----	---- ----	---- ----
ADRESL	9Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	9Fh	-000 ----	-000 ----	-uuu ----
LVDCON	94h	--00 -000	--00 -000	--uu -uuu
CRCON	110h	00-- --00	00-- --00	uu-- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 12-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: PIC16F636/639 only.

TABLE 12-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	--01 --0x
$\overline{\text{MCLR}}$ Reset during normal operation	000h	000u uuuu	--0u --uu
$\overline{\text{MCLR}}$ Reset during Sleep	000h	0001 0uuu	--0u --uu
WDT Reset	000h	0000 uuuu	--0u --uu
WDT Wake-up	PC + 1	uuu0 0uuu	--uu --uu
Brown-out Reset	000h	0001 1uuu	--01 --10
Interrupt Wake-up from Sleep	PC + 1(1)	uuu1 0uuu	--uu --uu
Wake-up Reset	000h	0001 1xxx	--01 --0x

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and the Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

12.11 Watchdog Timer (WDT)

The PIC12F635/PIC16F636/639 WDT is code and functionally compatible with other PIC16F WDT modules and adds a 16-bit prescaler to the WDT. This allows the user to have a scaler value for the WDT and TMR0 at the same time. In addition, the WDT time-out value can be extended to 268 seconds. WDT is cleared under certain conditions described in Table 12-7.

12.11.1 WDT OSCILLATOR

The WDT derives its time base from the 31 kHz LFINTOSC. The LTS bit does not reflect that the LFINTOSC is enabled.

The value of WDTCON is '---0 1000' on all Resets. This gives a nominal time base of 16 ms, which is compatible with the time base generated with previous PIC12F635/PIC16F636/639 microcontroller versions.

Note:	When the Oscillator Start-up Timer (OST) is invoked, the WDT is held in Reset, because the WDT Ripple Counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDT will begin counting (if enabled).

A new prescaler has been added to the path between the INTRC and the multiplexers used to select the path for the WDT. This prescaler is 16 bits and can be programmed to divide the INTRC by 32 to 65536, giving the WDT a nominal range of 1 ms to 268s.

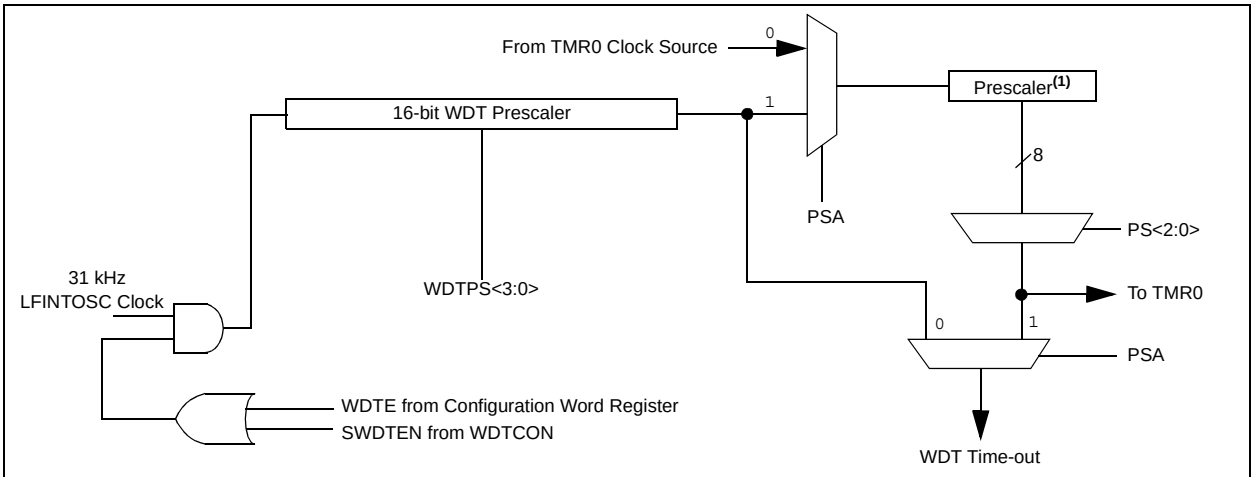
12.11.2 WDT CONTROL

The WDTE bit is located in the Configuration Word register. When set, the WDT runs continuously.

When the WDTE bit in the Configuration Word register is set, the SWDTEN bit of the WDTCON register has no effect. If WDTE is clear, then the SWDTEN bit can be used to enable and disable the WDT. Setting the bit will enable it and clearing the bit will disable it.

The PSA and PS<2:0> bits of the OPTION register have the same function as in previous versions of the PIC16F family of microcontrollers. See **Section 5.0 "Timer0 Module"** for more information.

FIGURE 12-9: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: This is the shared Timer0/WDT prescaler. See **Section 5.1.3 "Software Programmable Prescaler"** for more information.

TABLE 12-7: WDT STATUS

Conditions	WDT
WDTE = 0	Cleared
CLRWDT Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, HFINTOSC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

13.2 Instruction Descriptions

ADDLW	Add literal and W
Syntax:	[*label*] ADDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW	AND literal with W
Syntax:	[*label*] ANDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a two-cycle instruction.

14.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

14.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC® and MCU devices. It debugs and programs PIC® and dsPIC® Flash microcontrollers with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high speed, noise tolerant, low-voltage differential signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

14.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

14.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

15.4 DC Characteristics: PIC12F635/PIC16F636-I (Industrial) PIC12F635/PIC16F636-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports:					
D030		with TTL buffer	VSS	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D030A			VSS	—	0.15 VDD	V	Otherwise
D031		with Schmitt Trigger buffer	VSS	—	0.2 VDD	V	Entire range
D032		$\overline{MCLR}$, OSC1 (RC mode)	VSS	—	0.2 VDD	V	
D033		OSC1 (XT and LP modes)(1)	VSS	—	0.3	V	
D033A		OSC1 (HS mode)(1)	VSS	—	0.3 VDD	V	
	VIH	**Input High Voltage**					
		I/O ports:					
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			(0.25 VDD + 0.8)	—	VDD	V	Otherwise
D041		with Schmitt Trigger buffer	0.8 VDD	—	VDD	V	Entire range
D042		$\overline{MCLR}$	0.8 VDD	—	VDD	V	
D043		OSC1 (XT and LP modes)	1.6	—	VDD	V	**(Note 1)**
D043A		OSC1 (HS mode)	0.7 VDD	—	VDD	V	**(Note 1)**
D043B		OSC1 (RC mode)	0.9 VDD	—	VDD	V	
	IIL	**Input Leakage Current(2)**					
D060		I/O ports	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D060A		Analog inputs	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD
D060B		VREF	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD
D061		$\overline{MCLR}$(3)	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration
D070	IPUR	**PORTA Weak Pull-up Current**	50	250	400	µA	VDD = 5.0V, VPIN = VSS
D071	IPDR	**PORTA Weak Pull-down Current**	50	250	400	µA	VDD = 5.0V, VPIN = VDD
	VOL	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V (Ind.)
D083		OSC2/CLKOUT (RC mode)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V (Ind.) IOL = 1.2 mA, VDD = 4.5V (Ext.)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 9.4.1 "Using the Data EEPROM"** for additional information.

15.6 DC Characteristics: PIC16F639-I (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial Supply Voltage 2.0V ≤ VDD ≤ 3.6V					
Param No.	Sym	Device Characteristics	Min	Typ†	Max	Units	Conditions	
							VDD	Note
D010	IDD	**Supply Current(1,2,3)**	—	11	16	µA	2.0	FOSC = 32.768 kHz LP Oscillator mode
			—	18	28	µA	3.0	
D011			—	140	240	µA	2.0	FOSC = 1 MHz XT Oscillator mode
			—	220	380	µA	3.0	
D012			—	260	360	µA	2.0	FOSC = 4 MHz XT Oscillator mode
			—	420	650	µA	3.0	
D013			—	130	220	µA	2.0	FOSC = 1 MHz EC Oscillator mode
			—	215	360	µA	3.0	
D014			—	220	340	µA	2.0	FOSC = 4 MHz EC Oscillator mode
			—	375	550	µA	3.0	
D015			—	8	20	µA	2.0	FOSC = 31 kHz LFINTOSC mode
			—	16	40	µA	3.0	
D016			—	340	450	µA	2.0	FOSC = 4 MHz HFINTOSC mode
			—	500	700	µA	3.0	
D017			—	230	400	µA	2.0	FOSC = 4 MHz EXTRC mode
			—	400	680	µA	3.0	
D020	IPD	**Power-down Base Current(4)**	—	0.15	1.2	µA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled (excludes AFE)
			—	0.20	1.5	µA	3.0	
D021	IWDT		—	1.2	2.2	µA	2.0	WDT Current(1)
			—	2.0	4.0	µA	3.0	
D022A	IBOR		—	42	60	µA	3.0	BOR Current(1)
D022B	ILVD		—	22	28	µA	2.0	PLVD Current
			—	25	35	µA	3.0	
D023	ICMP		—	32	45	µA	2.0	Comparator Current(1)
			—	60	78	µA	3.0	
D024A	IVREFHS		—	30	36	µA	2.0	CVREF Current(1) (high-range)
			—	45	55	µA	3.0	
D024B	IVREFLS		—	39	47	µA	2.0	CVREF Current(1) (low-range)
			—	59	72	µA	3.0	
D025	IT1OSC		—	4.5	7.0	µA	2.0	T1OSC Current(1)
			—	5.0	8.0	µA	3.0	
D026	IACT	**Active Current** of AFE only (receiving signal) 1 LC Input Channel Signal 3 LC Input Channel Signals	 — —	 10 13	 — 18	 µA µA	 3.6 3.6	$\overline{CS}$ = VDD; Input = Continuous Wave (CW); Amplitude = 300 mVPP. All channels enabled.
D027	ISTDBY	**Standby Current** of AFE only (not receiving signal) 1 LC Input Channel Enabled 2 LC Input Channels Enabled 3 LC Input Channels Enabled	 — — —	 3 4 5	 5 6 7	 µA µA µA	 3.6 3.6 3.6	$\overline{CS}$ = VDD; $\overline{ALERT}$ = VDD
D028	ISLEEP	**Sleep Current** of AFE only	—	0.2	1	µA	3.6	$\overline{CS}$ = VDD; $\overline{ALERT}$ = VDD

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled. MCU only, Analog Front-End not included.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. MCU only, Analog Front-End not included.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

15.10 AC Characteristics: PIC12F635/PIC16F636/639 (Industrial, Extended)

FIGURE 15-5: CLOCK TIMING

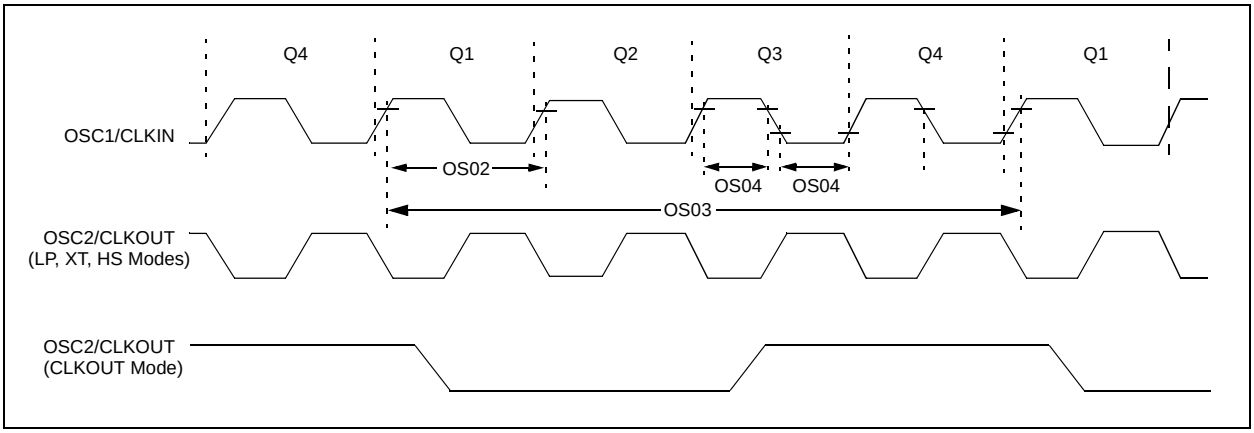


TABLE 15-1: CLOCK OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
OS01	FOSC	External CLKIN Frequency(1)	DC	—	37	kHz	LP Oscillator mode
			DC	—	4	MHz	XT Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	—	20	MHz	EC Oscillator mode
		Oscillator Frequency(1)	—	32.768	—	kHz	LP Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
			1	—	20	MHz	HS Oscillator mode
			DC	—	4	MHz	RC Oscillator mode
OS02	TOSC	External CLKIN Period(1)	27	—	∞	µs	LP Oscillator mode
			250	—	∞	ns	XT Oscillator mode
			50	—	∞	ns	HS Oscillator mode
			50	—	∞	ns	EC Oscillator mode
		Oscillator Period(1)	—	30.5	—	µs	LP Oscillator mode
			250	—	10,000	ns	XT Oscillator mode
			50	—	1,000	ns	HS Oscillator mode
			250	—	—	ns	RC Oscillator mode
OS03	TCY	Instruction Cycle Time(1)	200	TCY	DC	ns	TCY = 4/FOSC
OS04*	TosH, TosL	External CLKIN High, External CLKIN Low	2	—	—	µs	LP oscillator
			100	—	—	ns	XT oscillator
			20	—	—	ns	HS oscillator
OS05*	TosR, TosF	External CLKIN Rise, External CLKIN Fall	0	—	50	ns	LP oscillator
			0	—	25	ns	XT oscillator
			0	—	15	ns	HS oscillator

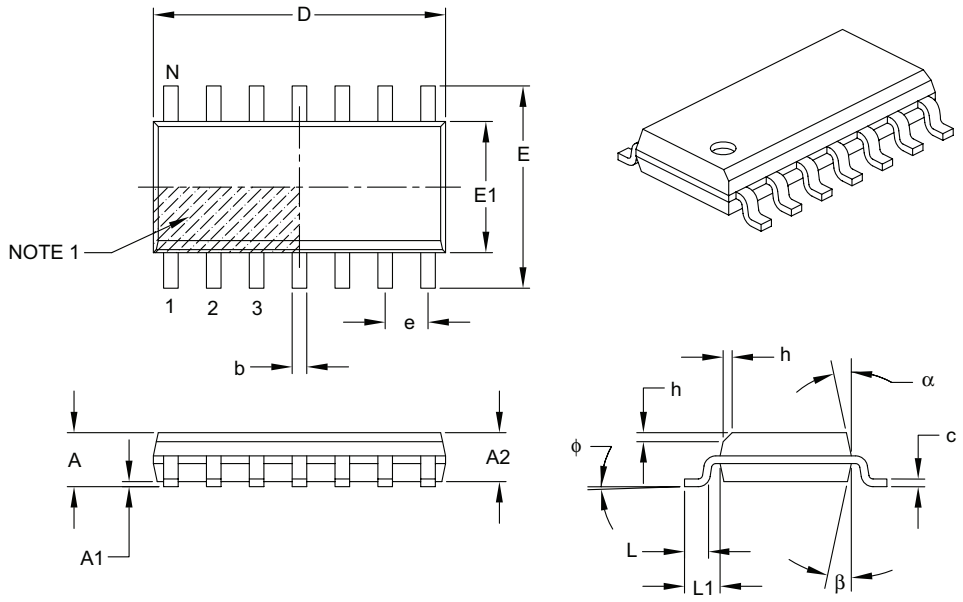
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

14-Lead Plastic Small Outline (SL or OD) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

Column Parity Register 6 126
Configuration Register 0 123
Configuration Register 1 124
Configuration Register 2 124
Configuration Register 3 125
Configuration Register 4 125
Configuration Register 5 126
CMCON0 (Comparator Control 0) 80
CMCON0 (Comparator Control) Register 79
CMCON1 (Comparator Control 1) 82
CMCON1 (Comparator Control) Register 82
CONFIG (Configuration Word) 130
EEADR (EEPROM Address) 91
EECON1 (EEPROM Control 1) 92
EEDAT (EEPROM Data) 91
INTCON (Interrupt Control) 28
IOCA (Interrupt-on-change PORTA) 50
LVDCON (Low-Voltage Detect Control) 89
OPTION_REG (OPTION) 27
OPTION_REG (Option) 63
OSCCON (Oscillator Control) 36
OSCTUNE (Oscillator Tuning) 40
PCON (Power Control Register) 31
PIE1 (Peripheral Interrupt Enable 1) 29
PIR1 (Peripheral Interrupt Request 1) 30
PORTA 48
PORTC 57
Reset Values 137
Reset Values (Special Registers) 138
STATUS 26
T1CON 68
TRISA (Tri-State PORTA) 48
TRISC (Tri-State PORTC) 57
VRCON (Voltage Reference Control) 84
WDA (Weak Pull-up/Pull-down Direction PORTA) 49
WDTCON (Watchdog Timer Control) 144
WPUDA (Weak Pull-up/Pull-down Enable PORTA) 49
Reset 131
Revision History 225

S

Software Simulator (MPLAB SIM) 160
Special Function Registers (SFR) 18
Maps
PIC12F635 19
PIC16F636/639 20
Summary
PIC12F635, Bank 0 21
PIC12F635, Bank 1 22
PIC12F635/PIC16F636/639, Bank 2 25
PIC16F636/639, Bank 0 23
PIC16F636/639, Bank 1 24
SPI Timing
Analog Front-End (AFE) for PIC16F639 190
STATUS Register 26

T

T1CON Register 68
Thermal Considerations 177
Time-out Sequence 135
Timer0 61
Associated Registers 63
External Clock 62
Interrupt 63
Operation 61, 64
Specifications 184
T0CKI 62
Timer1 64
Associated registers 69
Asynchronous Counter Mode 66
Reading and Writing 66
Interrupt 67
Modes of Operation 64
Operation During Sleep 67
Oscillator 66
Prescaler 66
Specifications 184
Timer1 Gate
Inverting Gate 66
Selecting Source 66, 81
Synchronizing CxOUT w/Timer1 81
TMR1H Register 64
TMR1L Register 64
Timers
Timer1
T1CON 68
Timing Diagrams
Brown-out Reset (BOR) 87, 182
Brown-out Reset Situations 134
CLKOUT and I/O 181
Clock Timing 179
Comparator Output 71
Fail-Safe Clock Monitor (FSCM) 46
INT Pin Interrupt 141
Internal Oscillator Switch Timing 42
Reset, WDT, OST and Power-up Timer 182
Time-out Sequence on Power-up (Delayed $\overline{\text{MCLR}}$) 136
Time-out Sequence on Power-up ($\overline{\text{MCLR}}$ with V_{DD}) 136
Timer0 and Timer1 External Clock 184
Timer1 Incrementing Edge 67
Two Speed Start-up 44
Wake-up from Sleep through Interrupt 146
Timing Parameter Symbology 178
TRISA 47
TRISA Register 48
TRISC Register 57
Two-Speed Clock Start-up Mode 43

U

Ultra Low-Power Wake-up 13, 14, 47, 51

V

Voltage Reference. *See* Comparator Voltage Reference (CV_{REF})
Voltage References
Associated registers 85

W

Wake-up from Sleep 145
Wake-up Reset (WUR) 132
Wake-up using Interrupts 145
Watchdog Timer (WDT) 143
Associated Registers 144
Control 143
Oscillator 143
Specifications 183
WDA Register 49
WDTCON Register 144
WPUDA Register 49
WWW Address 223
WWW, On-Line Support 7