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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f635-e-sn

PIC12F635/PIC16F636/639

8/14-Pin Flash-Based, 8-Bit CMOS Microcontrollers With nanoWatt Technology

High-Performance RISC CPU:

- Only 35 instructions to learn:
  - All single-cycle instructions except branches
- Operating speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range of 8 MHz to 125 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - Crystal fail detect for critical applications
  - Clock mode switching during operation for power savings
- Clock mode switching for low-power operation
- Power-Saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and Extended Temperature range
- Power-on Reset (POR)
- Wake-up Reset (WUR)
- Independent weak pull-up/pull-down resistors
- Programmable Low-Voltage Detect (PLVD)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection (program and data independent)
- High-Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM Retention: > 40 years

Low-Power Features:

- Standby Current:
  - 1 nA @ 2.0V, typical
- Operating Current:
  - 8.5 μA @ 32 kHz, 2.0V, typical
  - 100 μA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical

Peripheral Features:

- 6/12 I/O pins with individual direction control:
  - High-current source/sink for direct LED drive
  - Interrupt-on-change pin
  - Individually programmable weak pull-ups/ pull-downs
  - Ultra Low-Power Wake-up
- Analog Comparator module with:
  - Up to two analog comparators
  - Programmable On-chip Voltage Reference (CV_{REF}) module (% of V_{DD})
  - Comparator inputs and outputs externally accessible
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Timer1 Gate (count enable)
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
- KEELOQ® compatible hardware Cryptographic module
- In-Circuit Serial Programming™ (ICSP™) via two pins

Low-Frequency Analog Front-End Features (PIC16F639 only):

- Three input pins for 125 kHz LF input signals
- High input detection sensitivity (3 mV_{PP}, typical)
- Demodulated data, Carrier clock or RSSI output selection
- Input carrier frequency: 125 kHz, typical
- Input modulation frequency: 4 kHz, maximum
- 8 internal Configuration registers
- Bidirectional transponder communication (LF talk back)
- Programmable antenna tuning capacitance (up to 63 pF, 1 pF/step)
- Low standby current: 5 μA (with 3 channels enabled), typical
- Low operating current: 15 μA (with 3 channels enabled), typical
- Serial Peripheral Interface (SPI) with internal MCU and external devices
- Supports Battery Back-up mode and batteryless operation with external circuits

Device	Program Memory	Data Memory		I/O	Comparators	Low Frequency Analog Front-End
	Flash (words)	SRAM (bytes)	EEPROM (bytes)			
PIC12F635	1024	64	128	6	1	N
PIC16F636	2048	128	256	12	2	N
PIC16F639	2048	128	256	12	2	Y

Note 1: Any references to PORTA, RAn, TRISA and TRISAn refer to GPIO, GPn, TRISIO and TRISIOn, respectively.

2: V_{DDT} is the supply voltage of the Analog Front-End section (PIC16F639 only). V_{DDT} is treated as V_{DD} in this document unless otherwise stated.

3: V_{SST} is the ground reference voltage of the Analog Front-End section (PIC16F639 only). V_{SST} is treated as V_{SS} in this document unless otherwise stated.

14-Pin Diagram (PDIP, SOIC, TSSOP)

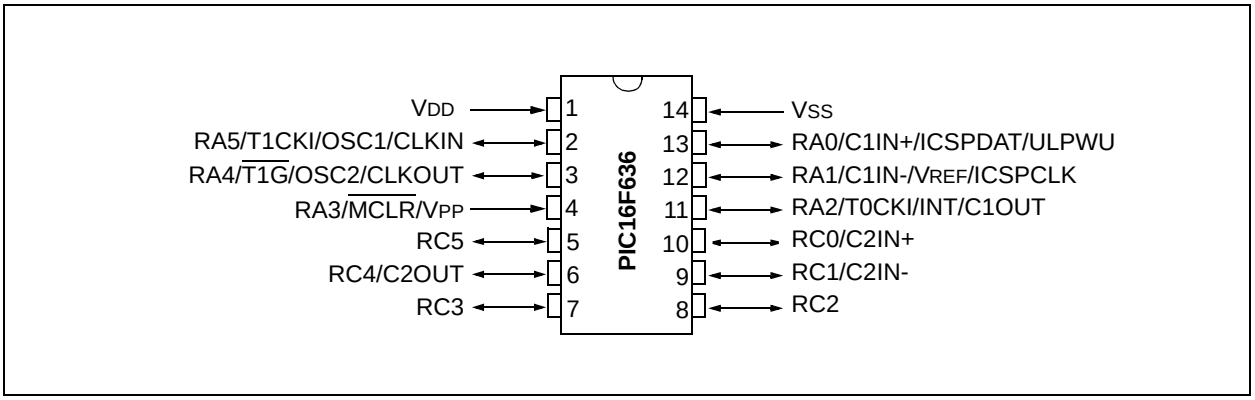


TABLE 2: 14-PIN SUMMARY (PDIP, SOIC, TSSOP)

I/O	Pin	Comparators	Timer	Interrupts	Pull-ups	Basic
RA0	13	C1IN+	—	IOC	Y	ICSPDAT/ULPWU
RA1	12	C1IN-	—	IOC	Y	VREF/ICSPCLK
RA2	11	C1OUT	T0CKI	INT/IOC	Y	—
RA3(1)	4	—	—	IOC	Y(2)	MCLR/VPP
RA4	3	—	T1G	IOC	Y	OSC2/CLKOUT
RA5	2	—	T1CKI	IOC	Y	OSC1/CLKIN
RC0	10	C2IN+	—	—	—	—
RC1	9	C2IN-	—	—	—	—
RC2	8	—	—	—	—	—
RC3	7	—	—	—	—	—
RC4	6	C2OUT	—	—	—	—
RC5	5	—	—	—	—	—
—	1	—	—	—	—	VDD
—	14	—	—	—	—	VSS

Note 1: Input only.

2: Only when pin is configured for external MCLR.

2.2.2.2 OPTION Register

The OPTION register is a readable and writable register which contains various control bits to configure:

- TMR0/WDT prescaler
- External RA2/INT interrupt
- TMR0
- Weak pull-up/pull-downs on PORTA

Note: To achieve a 1:1 prescaler assignment for Timer0, assign the prescaler to the WDT by setting the PSA bit of the OPTION register to '1'. See **Section 5.1.3 "Software Programmable Prescaler"**.

REGISTER 2-2: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{RAPU}}$:** PORTA Pull-up Enable bit
1 = PORTA pull-ups are disabled
0 = PORTA pull-ups are enabled by individual PORT latch values

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RA2/INT pin
0 = Interrupt on falling edge of RA2/INT pin

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on RA2/T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on RA2/T0CKI pin
0 = Increment on low-to-high transition on RA2/T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

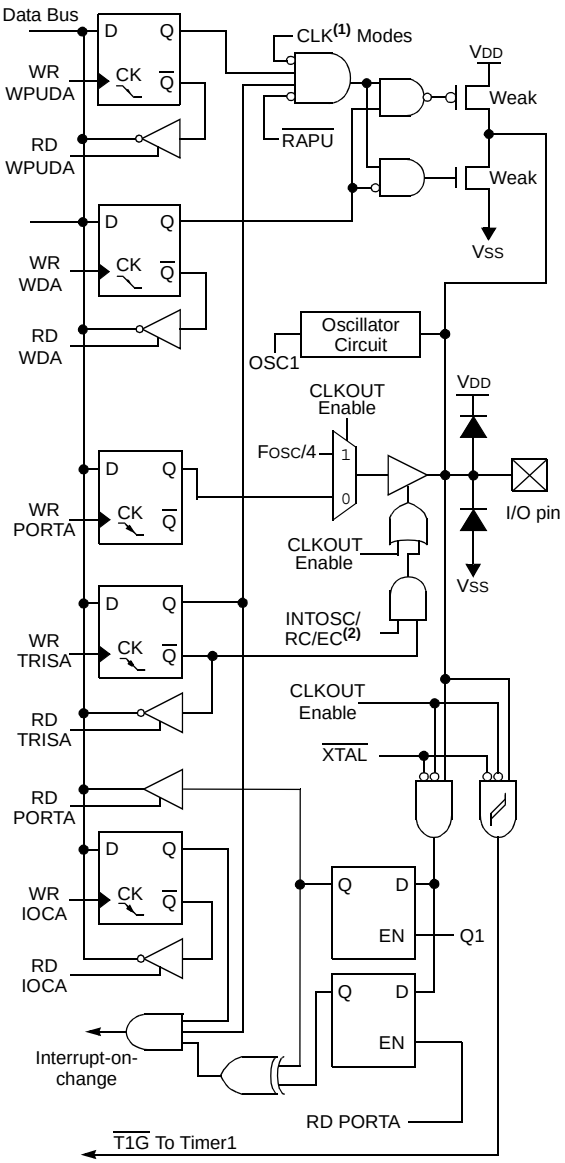
Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

4.2.4.5 RA4/$\overline{T1G}$/OSC2/CLKOUT

Figure 4-5 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 gate input
- a crystal/resonator connection
- a clock output

FIGURE 4-5: BLOCK DIAGRAM OF RA4



Note 1: Oscillator modes are XT, HS, LP, LPTMR1 and CLKOUT Enable.

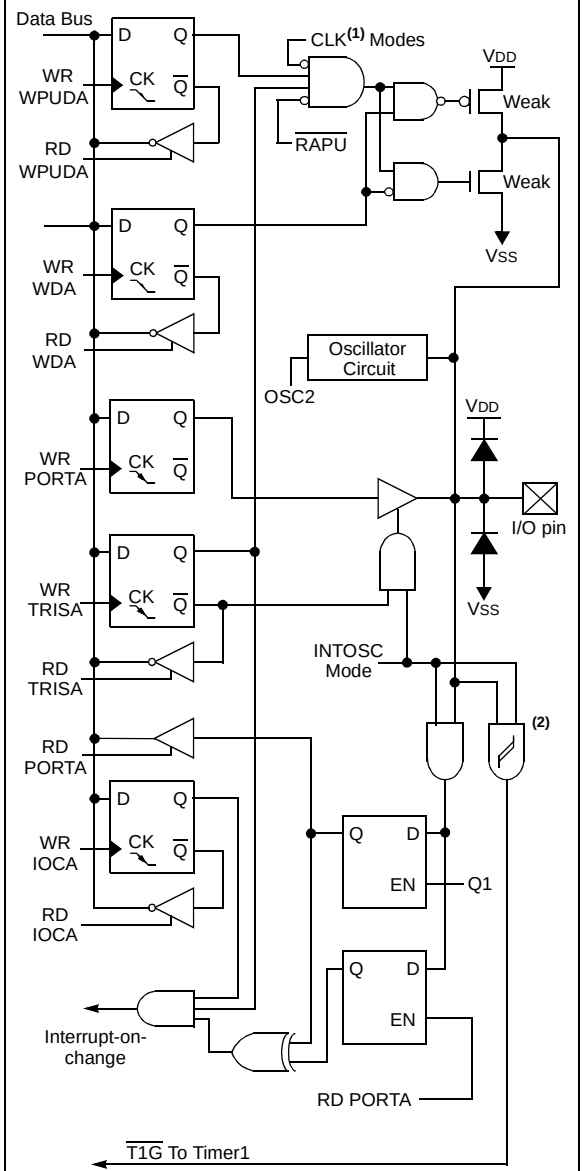
2: With CLKOUT option.

4.2.4.6 RA5/T1CKI/OSC1/CLKIN

Figure 4-6 shows the diagram for this pin. The RA5 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 clock input
- a crystal/resonator connection
- a clock input

FIGURE 4-6: BLOCK DIAGRAM OF RA5



Note 1: Oscillator modes are XT, HS, LP and LPTMR1.

2: When using Timer1 with LP oscillator, the Schmitt Trigger is bypassed.

7.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The comparators are very useful mixed signal building blocks because they provide analog functionality independent of the program execution. The Analog Comparator module includes the following features:

- Dual comparators (PIC16F636/639 only)
- Multiple comparator configurations
- Comparator(s) output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Timer1 gate (count enable)
- Output synchronization to Timer1 clock input
- Programmable voltage reference

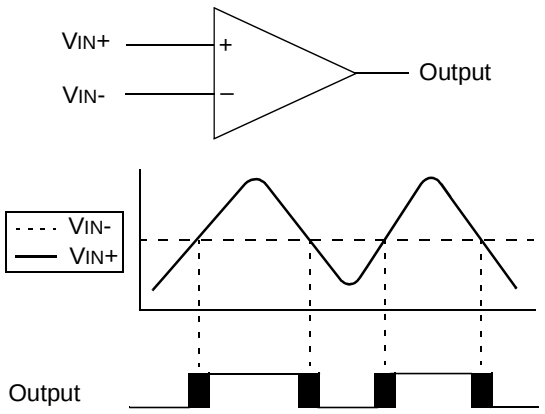
7.1 Comparator Overview

A comparator is shown in Figure 7-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The PIC12F635 contains a single comparator as shown in Figure 7-2.

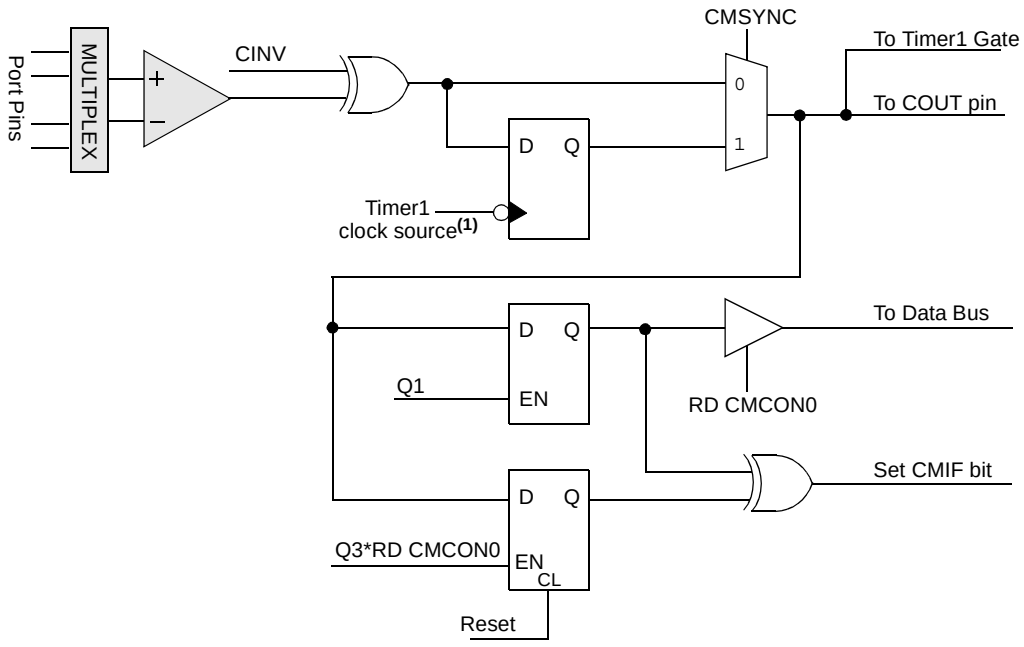
The PIC16F636/639 devices contains two comparators as shown in Figure 7-3 and Figure 7-4. The comparators are not independently configurable.

FIGURE 7-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

FIGURE 7-2: COMPARATOR OUTPUT BLOCK DIAGRAM (PIC12F635)



Note 1: Comparator output is latched on falling edge of Timer1 clock source.

2: Q1 and Q3 are phases of the four-phase system clock (FOSC).

3: Q1 is held high during Sleep mode.

7.4 Comparator Control

The CMCON0 register (Register 7-1) provides access to the following comparator features:

- Mode selection
- Output state
- Output polarity
- Input switch

7.4.1 COMPARATOR OUTPUT STATE

Each comparator state can always be read internally via the CxOUT bit of the CMCON0 register. The comparator state may also be directed to the CxOUT pin in the following modes:

PIC12F635

- CM<2:0> = 001
- CM<2:0> = 011
- CM<2:0> = 101

PIC16F636/639

- CM<2:0> = 110

When one of the above modes is selected, the associated TRIS bit of the CxOUT pin must be cleared.

7.4.2 COMPARATOR OUTPUT POLARITY

Inverting the output of a comparator is functionally equivalent to swapping the comparator inputs. The polarity of a comparator output can be inverted by setting the CXINV bit of the CMCON0 register. Clearing CXINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 7-1.

TABLE 7-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	CxINV	CxOUT
VIN- > VIN+	0	0
VIN- < VIN+	0	1
VIN- > VIN+	1	1
VIN- < VIN+	1	0

Note: CxOUT refers to both the register bit and output pin.

7.4.3 COMPARATOR INPUT SWITCH

The inverting input of the comparators may be switched between two analog pins in the following modes:

PIC12F635

- CM<2:0> = 101
- CM<2:0> = 110

PIC16F636/639

- CM<2:0> = 001 (Comparator C1 only)
- CM<2:0> = 010 (Comparators C1 and C2)

In the above modes, both pins remain in Analog mode regardless of which pin is selected as the input. The CIS bit of the CMCON0 register controls the comparator input switch.

REGISTER 8-1: LVDCON: LOW-VOLTAGE DETECT CONTROL REGISTER

U-0	U-0	R-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	—	IRVST(1)	LVDEN	—	LVDL2	LVDL1	LVDL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **IRVST:** Internal Reference Voltage Stable Status Flag bit(1)
1 = Indicates that the PLVD is stable and PLVD interrupt is reliable
0 = Indicates that the PLVD is not stable and PLVD interrupt must not be enabled

bit 4 **LVDEN:** Low-Voltage Detect Module Enable bit
1 = Enables PLVD Module, powers up PLVD circuit and supporting reference circuitry
0 = Disables PLVD Module, powers down PLVD circuit and supporting reference circuitry

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **LVDL<2:0>:** Low-Voltage Detection Level bits (nominal values)
111 = 4.5V
110 = 4.2V
101 = 4.0V
100 = 2.3V (default)
011 = 2.2V
010 = 2.1V
001 = 2.0V(2)
000 = Reserved

Note 1: The IRVST bit is usable only when the HFINTOSC is running.
2: Not tested and below minimum operating conditions.

TABLE 8-1: REGISTERS ASSOCIATED WITH PROGRAMMABLE LOW-VOLTAGE DETECT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIE1	OSFIE	C2IE	C1IE	LCDIE	—	LVDIE	—	CCP2IE	0000 -0-0	0000 -0-0
PIR1	OSFIF	C2IF	C1IF	LCDIF	—	LVDIF	—	CCP2IF	0000 -0-0	0000 -0-0
LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -100	--00 -100

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used by the PLVD module.

FIGURE 11-3: BIDIRECTIONAL PASSIVE KEYLESS ENTRY (PKE) SYSTEM APPLICATION EXAMPLE

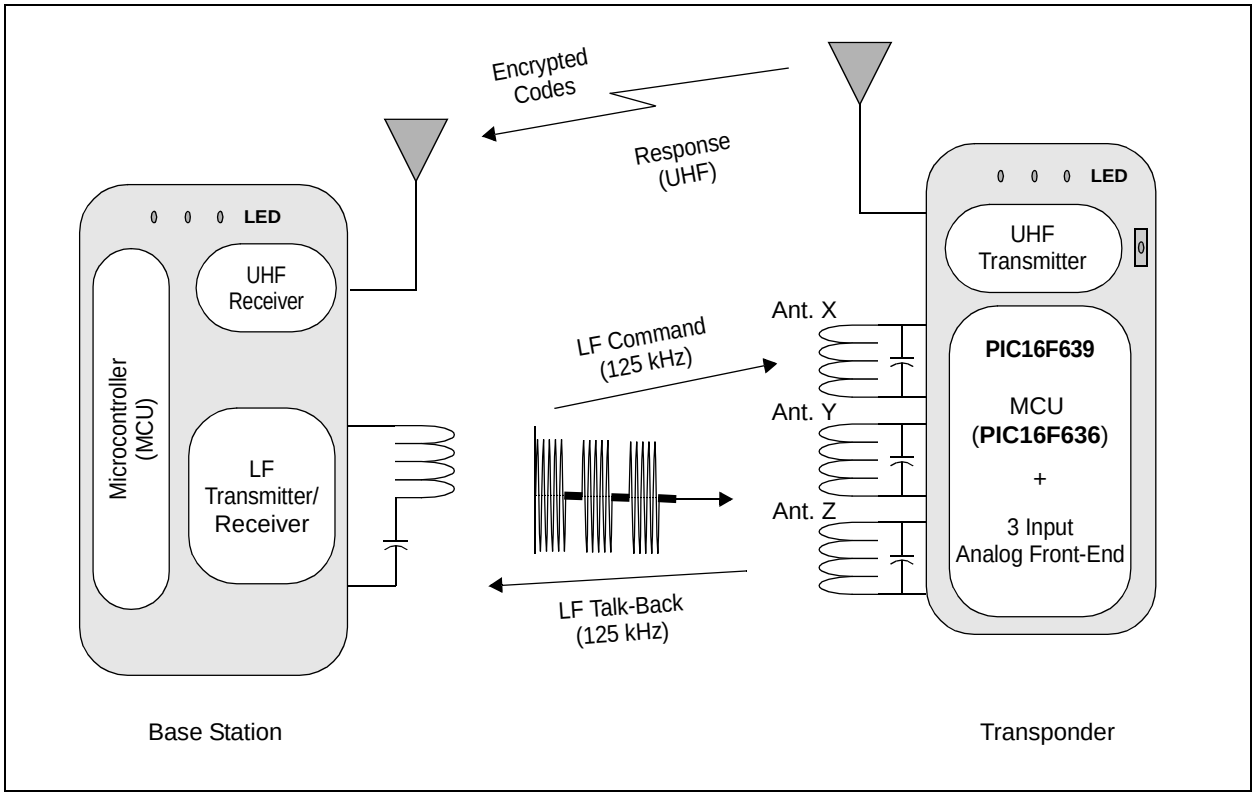


FIGURE 11-4: PASSIVE KEYLESS ENTRY (PKE) TRANSPONDER CONFIGURATION EXAMPLE

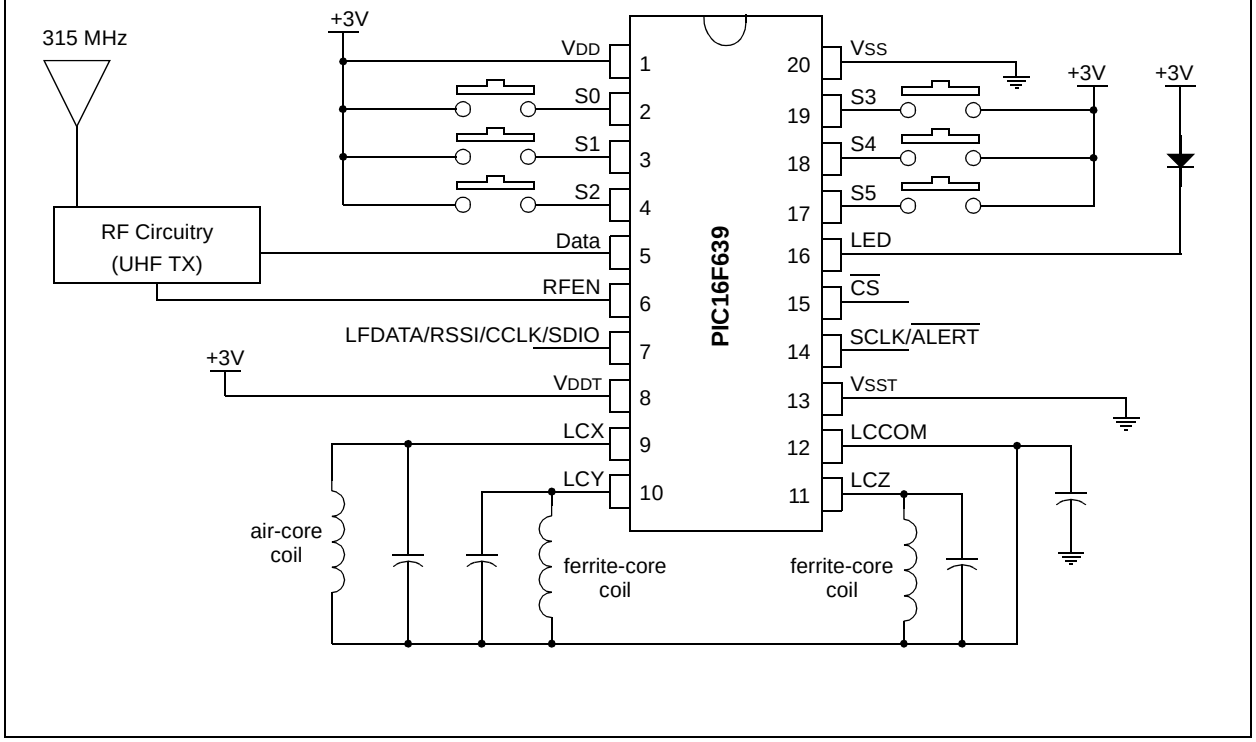
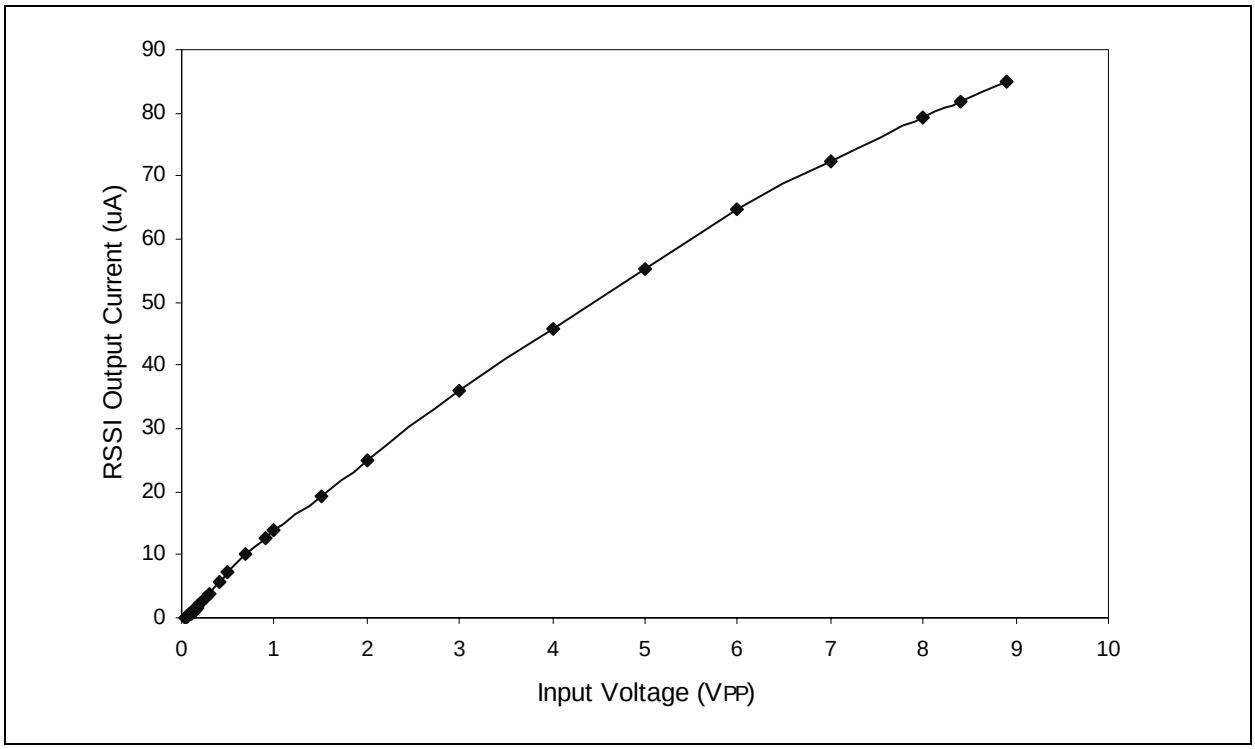


FIGURE 11-15: RSSI OUTPUT CURRENT VS. INPUT SIGNAL LEVEL EXAMPLE



REGISTER 11-2: CONFIGURATION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATOUT1	DATOUT0	LCXTUN5	LCXTUN4	LCXTUN3	LCXTUN2	LCXTUN1	LCXTUN0	R1PAR
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8-7 **DATOUT<1:0>:** LFDATA Output type bit
00 = Demodulated output
01 = Carrier Clock output
10 = RSSI output
11 = RSSI output

bit 6-1 **LCXTUN<5:0>:** LCX Tuning Capacitance bit
000000 = +0 pF (Default)
:
111111 = +63 pF

bit 0 **R1PAR**: Register Parity Bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

REGISTER 11-3: CONFIGURATION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSSIFET	CLKDIV	LCYTUN5	LCYTUN4	LCYTUN3	LCYTUN2	LCYTUN1	LCYTUN0	R2PAR
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8 **RSSIFET**: Pull-down MOSFET on LFDATA pad bit (controllable by user in the RSSI mode only)
1 = Pull-down RSSI MOSFET on
0 = Pull-down RSSI MOSFET off

bit 7 **CLKDIV:** Carrier Clock Divide-by bit
1 = Carrier Clock/4
0 = Carrier Clock/1

bit 6-1 **LCYTUN<5:0>:** LCY Tuning Capacitance bit
000000 = +0 pF (Default)
:
111111 = +63 pF

bit 0 **R2PAR**: Register Parity Bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

REGISTER 11-6: CONFIGURATION REGISTER 5

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AUTOCHSEL	AGCSIG	MODMIN1	MODMIN0	LCZSEN3	LCZSEN2	LCZSEN1	LCZSEN0	R5PAR
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8 **AUTOCHSEL**: Auto Channel Select bit
1 = Enabled – AFE selects channel(s) that has demodulator output "high" at the end of TSTAB; or otherwise, blocks the channel(s).
0 = Disabled – AFE follows channel enable/disable bits defined in Register 0

bit 7 **AGCSIG**: Demodulator Output Enable bit, after the AGC loop is active
1 = Enabled – No output until AGC is regulating at around 20 mVPP at input pins. The AGC Active Status bit is set when the AGC begins regulating.
0 = Disabled – the AFE passes signal of any level it is capable of detecting

bit 6-5 **MODMIN<1:0>**: Minimum Modulation Depth bit
00 = 50%
01 = 75%
10 = 25%
11 = 12%

bit 4-1 **LCZSEN<3:0>(1)**: LCZ Sensitivity Reduction bit
0000 = -0dB (Default)
:
1111 = -30dB

bit 0 **R5PAR**: Register Parity Bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

Note 1: Assured monotonic increment (or decrement) by design.

REGISTER 11-7: COLUMN PARITY REGISTER 6

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
COLPAR7	COLPAR6	COLPAR5	COLPAR4	COLPAR3	COLPAR2	COLPAR1	COLPAR0	R6PAR
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8 **COLPAR7**: Set/Cleared so that this 8th parity bit + the sum of the Configuration register row parity bits contain an odd number of set bits.

bit 7 **COLPAR6**: Set/Cleared such that this 7th parity bit + the sum of the 7th bits in Configuration Registers 0 through 5 contain an odd number of set bits.

bit 6 **COLPAR5**: Set/Cleared such that this 6th parity bit + the sum of the 6th bits in Configuration Registers 0 through 5 contain an odd number of set bits.

bit 5 **COLPAR4**: Set/Cleared such that this 5th parity bit + the sum of the 5th bits in Configuration Registers 0 through 5 contain an odd number of set bits.

bit 4 **COLPAR3**: Set/Cleared such that this 4th parity bit + the sum of the 4th bits in Configuration Registers 0 through 5 contain an odd number of set bits.

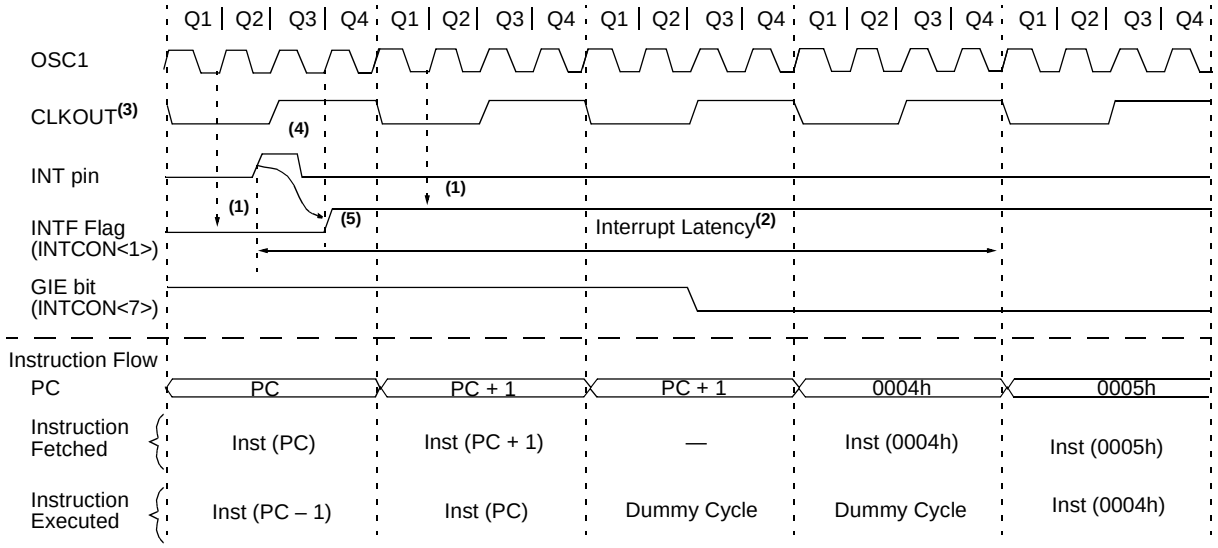
bit 3 **COLPAR2**: Set/Cleared such that this 3rd parity bit + the sum of the 3rd bits in Configuration Registers 0 through 5 contain an odd number of set bits.

bit 2 **COLPAR1**: Set/Cleared such that this 2nd parity bit + the sum of the 2nd bits in Configuration Registers 0 through 5 contain an odd number of set bits.

bit 1 **COLPAR0**: Set/Cleared such that this 1st parity bit + the sum of the 1st bits in Configuration Registers 0 through 5 contain an odd number of set bits.

bit 0 **R6PAR**: Register Parity bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

FIGURE 12-8: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-4 TCY. Synchronous latency = 3 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT is available only in INTOSC and RC Oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in **Section 15.0 "Electrical Specifications"**.

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

TABLE 12-6: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
PIR1	EEIF	LVDIF	CRIF	C2IF(1)	C1IF	OSFIF	—	TMR1IF	0000 00-0	0000 00-0
PIE1	EEIE	LVDIE	CRIE	C2IE(1)	C1IE	OSFIE	—	TMR1IE	0000 00-0	0000 00-0

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0', q = value depends upon condition. Shaded cells are not used by the Interrupt module.

Note 1: PIC16F636/639 only.

15.1 DC Characteristics: PIC12F635/PIC16F636-I (Industrial) PIC12F635/PIC16F636-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001			2.0	—	5.5	V	FOSC < = 4 MHz
D001A			2.0	—	5.5	V	FOSC < = 8 MHz, HFINTOSC, EC
D001B			3.0	—	5.5	V	FOSC < = 10 MHz
D001C			4.5	—	5.5	V	FOSC < = 20 MHz
D002	VDR	**RAM Data Retention Voltage(1)**	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See **Section 12.3 "Power-on Reset"** for details.
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See **Section 12.3 "Power-on Reset"** for details.
D005	VBOD	**Brown-out Reset**	2.0	2.1	2.2	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

15.6 DC Characteristics: PIC16F639-I (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial Supply Voltage 2.0V ≤ VDD ≤ 3.6V					
Param No.	Sym	Device Characteristics	Min	Typ†	Max	Units	Conditions	
							VDD	Note
D010	IDD	**Supply Current(1,2,3)**	—	11	16	µA	2.0	FOSC = 32.768 kHz LP Oscillator mode
			—	18	28	µA	3.0	
D011			—	140	240	µA	2.0	FOSC = 1 MHz XT Oscillator mode
			—	220	380	µA	3.0	
D012			—	260	360	µA	2.0	FOSC = 4 MHz XT Oscillator mode
			—	420	650	µA	3.0	
D013			—	130	220	µA	2.0	FOSC = 1 MHz EC Oscillator mode
			—	215	360	µA	3.0	
D014			—	220	340	µA	2.0	FOSC = 4 MHz EC Oscillator mode
			—	375	550	µA	3.0	
D015			—	8	20	µA	2.0	FOSC = 31 kHz LFINTOSC mode
			—	16	40	µA	3.0	
D016			—	340	450	µA	2.0	FOSC = 4 MHz HFINTOSC mode
			—	500	700	µA	3.0	
D017			—	230	400	µA	2.0	FOSC = 4 MHz EXTRC mode
			—	400	680	µA	3.0	
D020	IPD	**Power-down Base Current(4)**	—	0.15	1.2	µA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled (excludes AFE)
			—	0.20	1.5	µA	3.0	
D021	IWDT		—	1.2	2.2	µA	2.0	WDT Current(1)
			—	2.0	4.0	µA	3.0	
D022A	IBOR		—	42	60	µA	3.0	BOR Current(1)
D022B	ILVD		—	22	28	µA	2.0	PLVD Current
			—	25	35	µA	3.0	
D023	ICMP		—	32	45	µA	2.0	Comparator Current(1)
			—	60	78	µA	3.0	
D024A	IVREFHS		—	30	36	µA	2.0	CVREF Current(1) (high-range)
			—	45	55	µA	3.0	
D024B	IVREFLS		—	39	47	µA	2.0	CVREF Current(1) (low-range)
			—	59	72	µA	3.0	
D025	IT1OSC		—	4.5	7.0	µA	2.0	T1OSC Current(1)
			—	5.0	8.0	µA	3.0	
D026	IACT	**Active Current** of AFE only (receiving signal) 1 LC Input Channel Signal 3 LC Input Channel Signals	 — —	 10 13	 — 18	 µA µA	 3.6 3.6	$\overline{CS}$ = VDD; Input = Continuous Wave (CW); Amplitude = 300 mVPP. All channels enabled.
D027	ISTDBY	**Standby Current** of AFE only (not receiving signal) 1 LC Input Channel Enabled 2 LC Input Channels Enabled 3 LC Input Channels Enabled	 — — —	 3 4 5	 5 6 7	 µA µA µA	 3.6 3.6 3.6	$\overline{CS}$ = VDD; $\overline{ALERT}$ = VDD
D028	ISLEEP	**Sleep Current** of AFE only	—	0.2	1	µA	3.6	$\overline{CS}$ = VDD; $\overline{ALERT}$ = VDD

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled. MCU only, Analog Front-End not included.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. MCU only, Analog Front-End not included.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

15.12 SPI Timing: Analog Front-End (AFE) for PIC16F639

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Supply Voltage 2.0V ≤ VDD ≤ 3.6V Operating temperature -40°C ≤ TAMB ≤ +85°C for industrial LC Signal Input Sinusoidal 300 mVPP Carrier Frequency 125 kHz LCCOM connected to VSS				
Param	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
AF33	FSCLK	SCLK Frequency	—	—	3	MHz	
AF34	Tcssc	$\overline{CS}$ fall to first SCLK edge setup time	100	—	—	ns	
AF35	TSU	SDI setup time	30	—	—	ns	
AF36	THD	SDI hold time	50	—	—	ns	
AF37	THI	SCLK high time	150	—	—	ns	
AF38	TLO	SCLK low time	150	—	—	ns	
AF39	TDO	SDO setup time	—	—	150	ns	
AF40	TSCCS	SCLK last edge to $\overline{CS}$ rise setup time	100	—	—	ns	
AF41	TCSH	$\overline{CS}$ high time	500	—	—	ns	
AF42	TCS1	$\overline{CS}$ rise to SCLK edge setup time	50	—	—	ns	
AF43	TCS0	SCLK edge to $\overline{CS}$ fall setup time	50	—	—	ns	SCLK edge when $\overline{CS}$ is high
AF44	TSPIR	Rise time of SPI data (SPI Read command)	—	10	—	ns	VDD = 3.0V. Time is measured from 10% to 90% of amplitude
AF45	TSPIF	Fall time of SPI data (SPI Read command)	—	10	—	ns	VDD = 3.0V. Time is measured from 90% to 10% of amplitude

***** Parameter is characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-24: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)

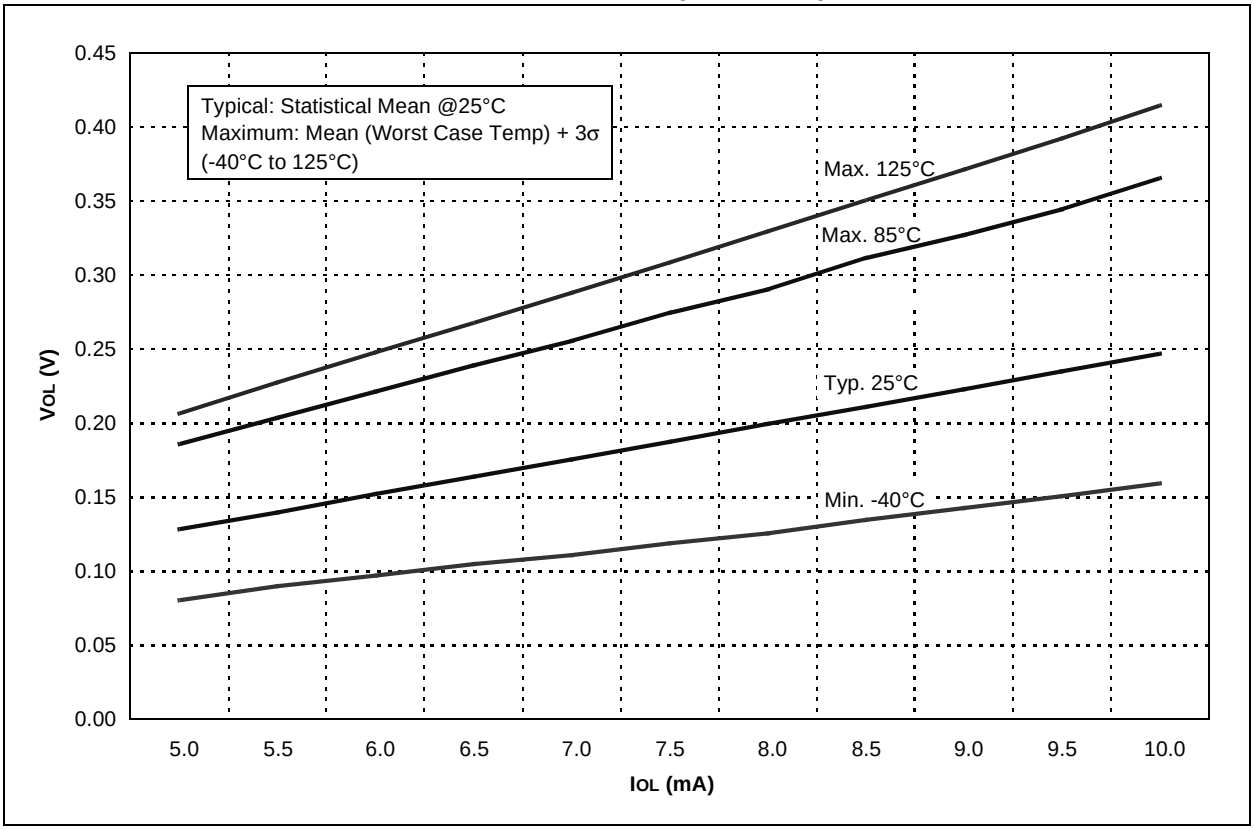


FIGURE 16-25: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)

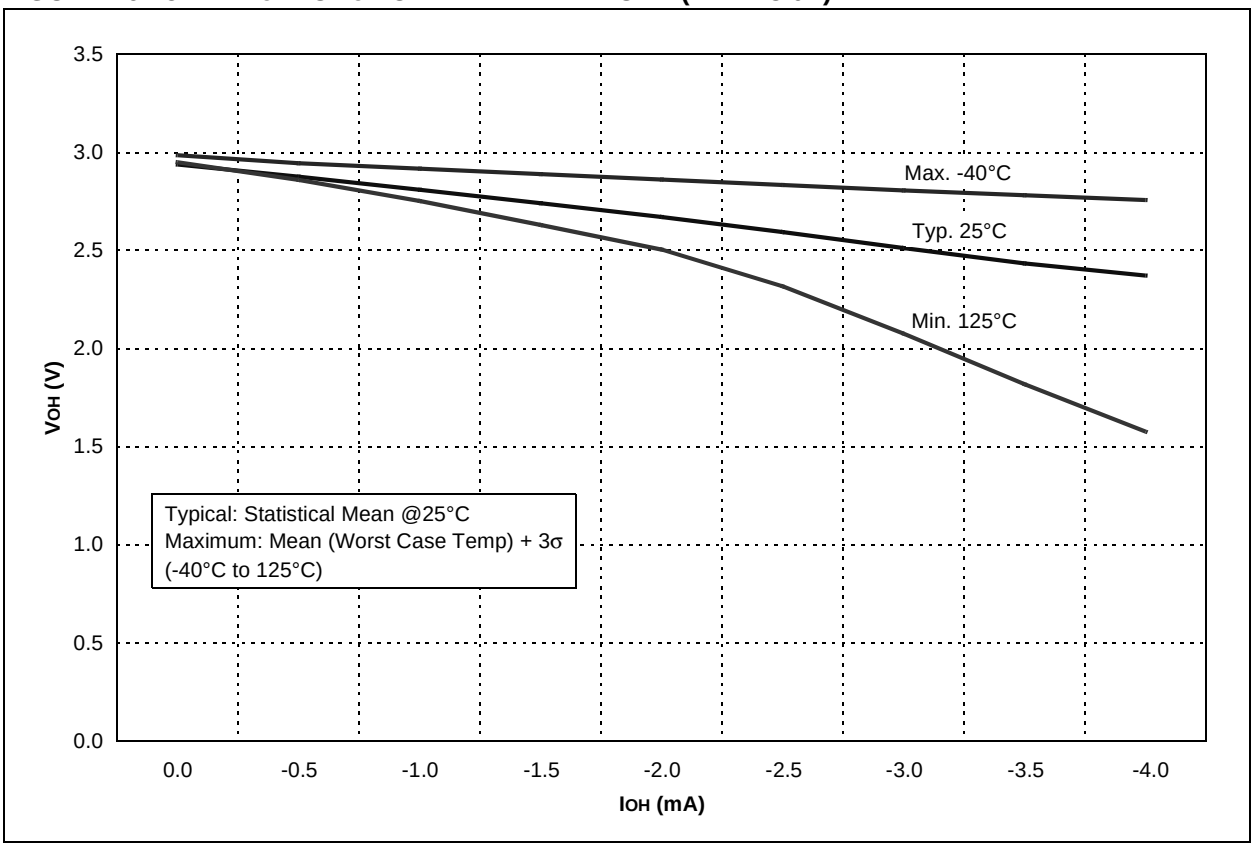


FIGURE 16-28: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

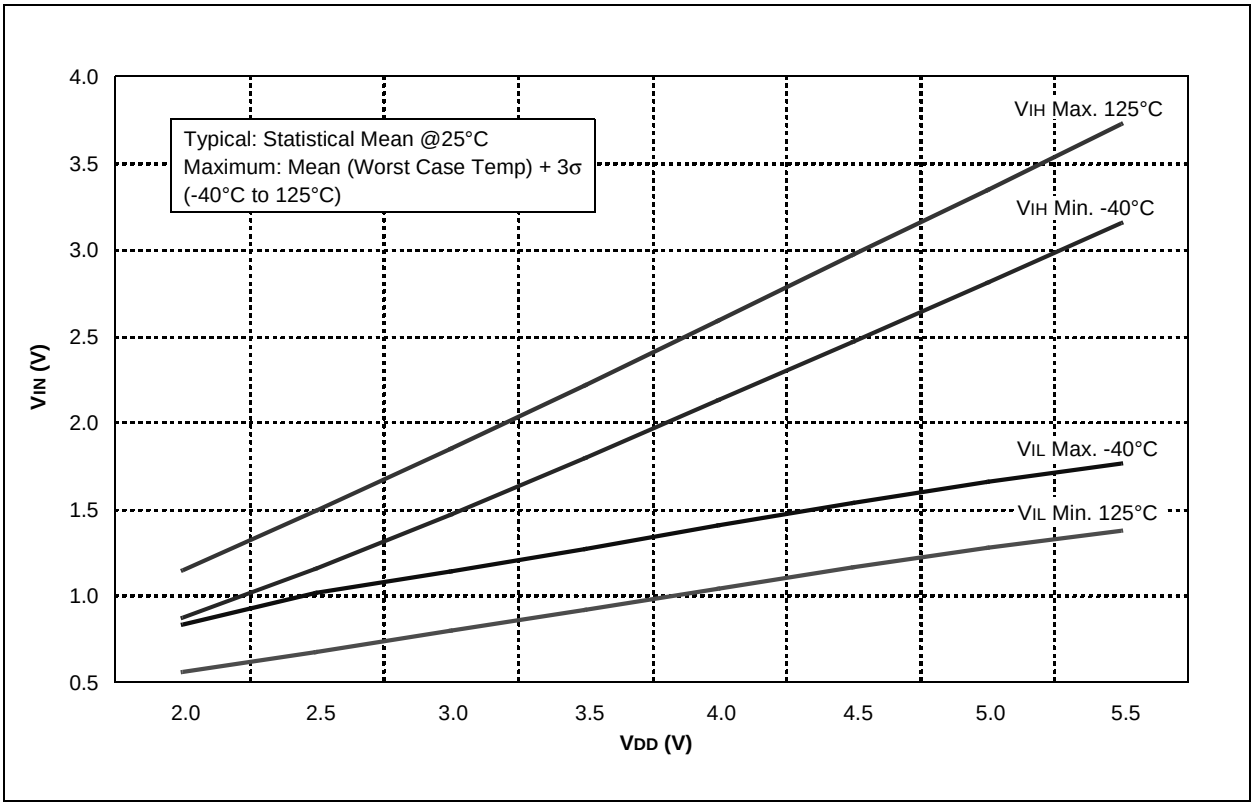
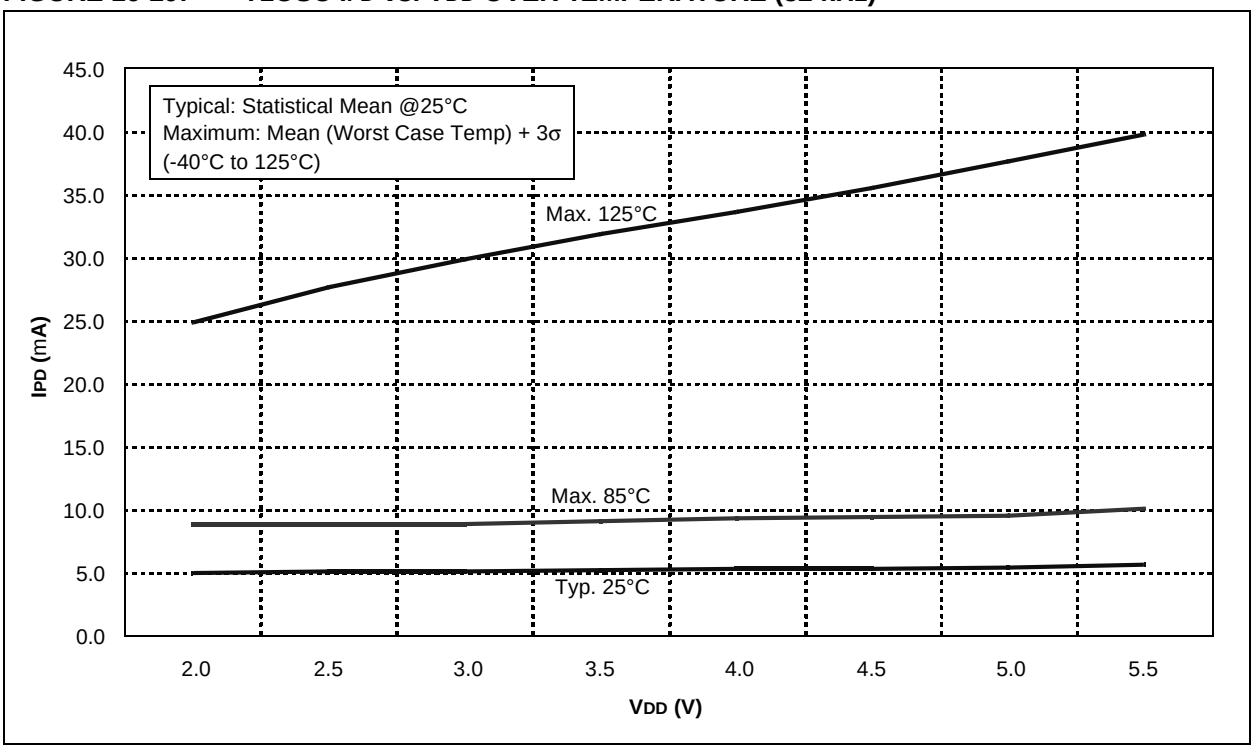
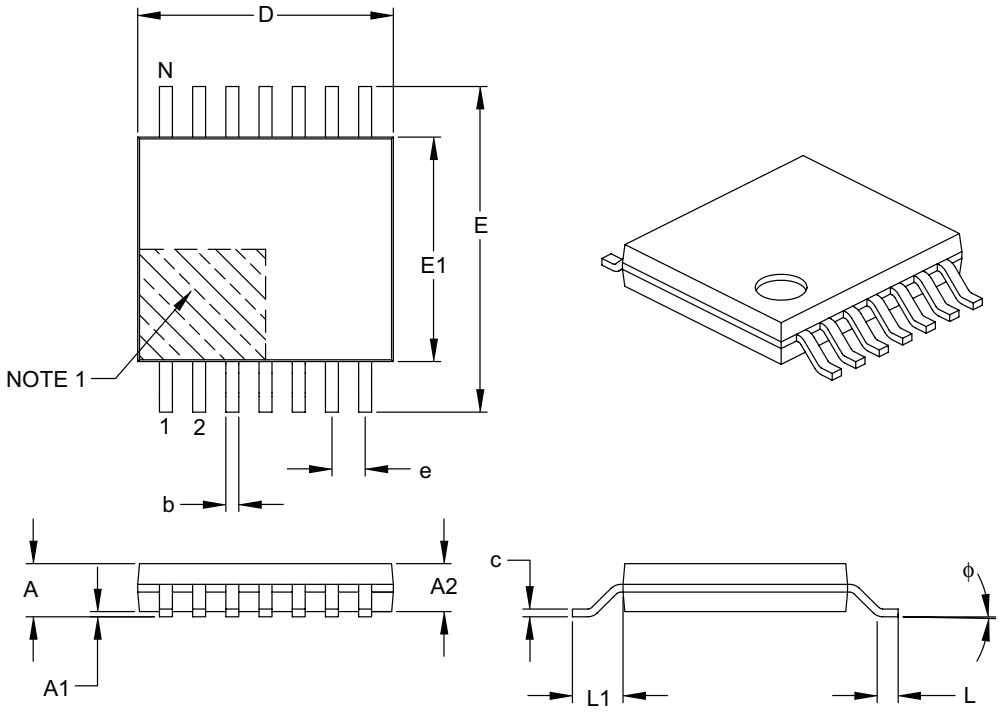


FIGURE 16-29: T1OSC IPD vs. VDD OVER TEMPERATURE (32 kHz)



14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

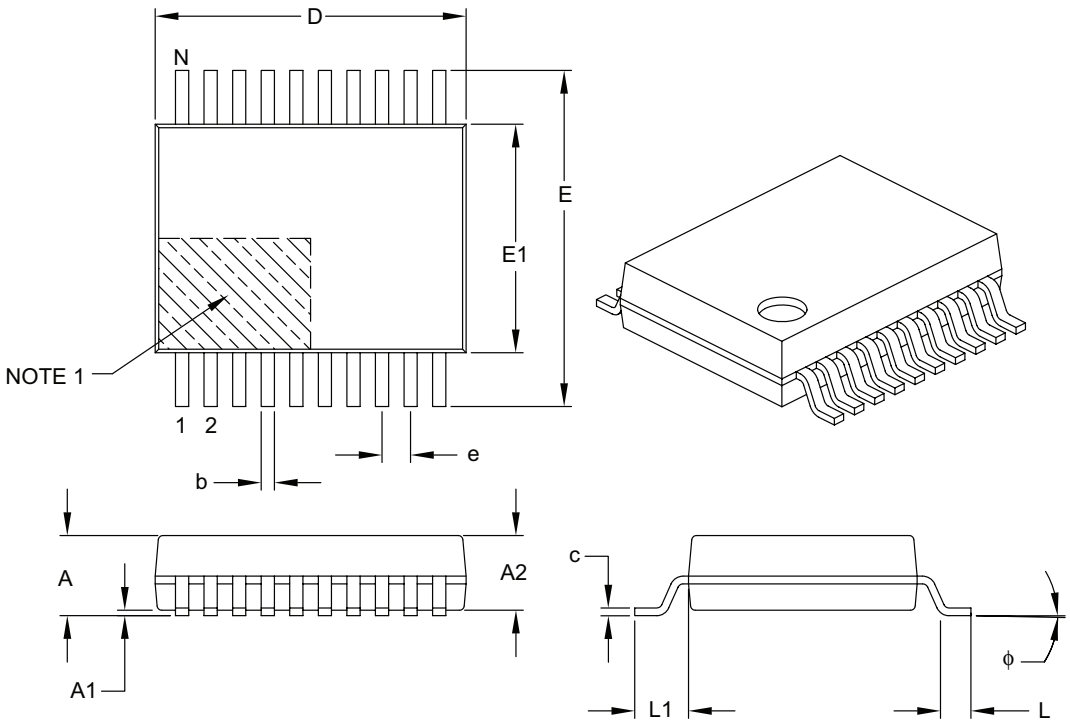
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B