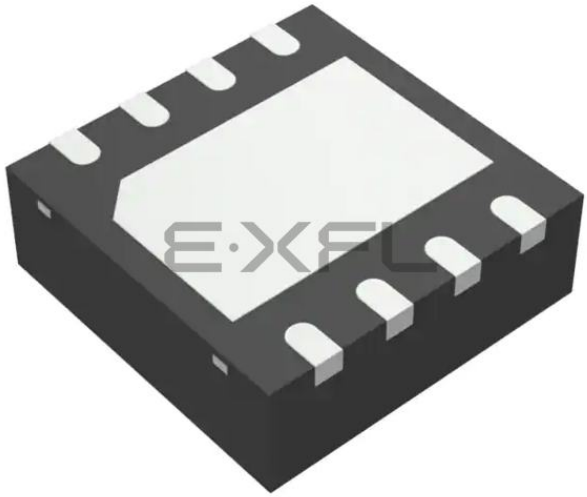

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f635-i-md

TABLE 1-3: PIC16F639 PINOUT DESCRIPTIONS

Name	Function	Input Type	Output Type	Description
LCCOM	LCCOM	AN	—	Common reference for analog inputs.
LCX	LCX	AN	—	125 kHz analog X channel input.
LCY	LCY	AN	—	125 kHz analog Y channel input.
LCZ	LCZ	AN	—	125 kHz analog Z channel input.
RA0/C1IN+/ICSPDAT/ULPWU	RA0	TTL	—	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down. Selectable Ultra Low-Power Wake-up pin.
	C1IN+	AN	—	Comparator1 input – positive.
	ICSPDAT	TTL	CMOS	Serial Programming Data IO.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
RA1/C1IN-/VREF/ICSPCLK	RA1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	C1IN-	AN	—	Comparator1 input – negative.
	VREF	AN	—	External voltage reference
	ICSPCLK	ST	—	Serial Programming Clock.
RA2/T0CKI/INT/C1OUT	RA2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T0CKI	ST	—	External clock for Timer0.
	INT	ST	—	External Interrupt.
	C1OUT	—	CMOS	Comparator1 output.
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear Reset. Pull-up enabled when configured as $\overline{\text{MCLR}}$.
	VPP	HV	—	Programming voltage.
RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT	RA4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate.
	OSC2	—	XTAL	XTAL connection.
	CLKOUT	—	CMOS	TOSC reference clock.
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T1CKI	ST	—	Timer1 clock.
	OSC1	XTAL	—	XTAL connection.
	CLKIN	ST	—	TOSC/4 reference clock.
RC0/C2IN+	RC0	TTL	CMOS	General purpose I/O.
	C2IN+	AN	—	Comparator1 input – positive.
RC1/C2IN-/$\overline{\text{CS}}$	RC1	TTL	CMOS	General purpose I/O.
	C2IN-	AN	—	Comparator1 input – negative.
	$\overline{\text{CS}}$	TTL	—	Chip select input for SPI communication with internal pull-up resistor.
RC2/SCLK/$\overline{\text{ALERT}}$	RC2	TTL	CMOS	General purpose I/O.
	SCLK	TTL	—	Digital clock input for SPI communication.
	$\overline{\text{ALERT}}$	—	OD	Output with internal pull-up resistor for AFE error signal.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; D = Direct
HV = High Voltage; ST = Schmitt Trigger input with CMOS levels; OD = Open Drain
TTL = TTL compatible input; XTAL = Crystal

2.2.1 GENERAL PURPOSE REGISTER

The register file is organized as 64 x 8 for the PIC12F635 and 128 x 8 for the PIC16F636/639. Each register is accessed, either directly or indirectly, through the File Select Register, FSR (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Figure 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 2-5: PIC12F635/PIC16F636/639 SPECIAL FUNCTION REGISTERS SUMMARY BANK 2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR/ WUR	Page
Bank 2											
10Ch	—	Unimplemented								—	—
10Dh	—	Unimplemented								—	—
10Eh	—	Unimplemented								—	—
10Fh	—	Unimplemented								—	—
110h	CRCON	GO/$\overline{\text{DONE}}$	ENC/$\overline{\text{DEC}}$	—	—	—	—	CRREG1	CRREG0	00-- --00	00-- --00
111h	CRDAT0(2)	Cryptographic Data Register 0								0000 0000	0000 0000
112h	CRDAT1(2)	Cryptographic Data Register 1								0000 0000	0000 0000
113h	CRDAT2(2)	Cryptographic Data Register 2								0000 0000	0000 0000
114h	CRDAT3(2)	Cryptographic Data Register 3								0000 0000	0000 0000
115h	—	Unimplemented								—	—
116h	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

2: CRDAT<3:0> registers are KEELOQ® hardware peripheral related registers and require the execution of the "KEELOQ Encoder License Agreement" regarding implementation of the module and access to related registers. The "KEELOQ Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ or by contacting your local Microchip Sales Representative.

2.2.2.6 PCON Register

The Power Control (PCON) register (see Table 12-3) contains flag bits to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Wake-up Reset ($\overline{WUR}$)
- Brown-out Reset ($\overline{BOR}$)
- Watchdog Timer Reset (WDT)
- External $\overline{MCLR}$ Reset

The PCON register also controls the Ultra Low-Power Wake-up and software enable of the $\overline{BOR}$.

The PCON register bits are shown in Register 2-6.

REGISTER 2-6: PCON: POWER CONTROL REGISTER

U-0	U-0	R/W-0	R/W-1	R/W-x	U-0	R/W-0	R/W-x
—	—	ULPWUE	SBOREN(1)	$\overline{WUR}$	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **ULPWUE:** Ultra Low-Power Wake-up Enable bit
1 = Ultra low-power wake-up enabled
0 = Ultra low-power wake-up disabled

bit 4 **SBOREN:** Software BOR Enable bit(1)
1 = BOR enabled
0 = BOR disabled

bit 3 **$\overline{WUR}$**: Wake-up Reset Status bit
1 = No Wake-up Reset occurred
0 = A Wake-up Reset occurred (must be set in software after a Power-on Reset occurs)

bit 2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: BOREN<1:0> = 01 in the Configuration Word register for this bit to control the $\overline{BOR}$.

6.10 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 6-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 6-1: T1CON: TIMER 1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV(1)	TMR1GE(2)	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **T1GINV:** Timer1 Gate Invert bit(1)
1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 6 **TMR1GE:** Timer1 Gate Enable bit(2)
If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 is on if Timer1 gate is active
0 = Timer1 is on

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
If INTOSC without CLKOUT oscillator is active:
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
Else:
This bit is ignored. LP oscillator is disabled.

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from T1CKI pin (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Note 1: T1GINV bit inverts the Timer1 gate logic, regardless of source.
2: TMR1GE bit must be set to use either $\overline{\text{T1G}}$ pin or C2OUT, as selected by the T1GSS bit of the CMCON1 register, as a Timer1 gate source.

7.5 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Specifications in **Section 15.0 "Electrical Specifications"** for more details.

7.6 Comparator Interrupt Operation

The comparator interrupt flag is set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figures 7-8 and 7-9). One latch is updated with the comparator output level when the CMCON0 register is read. This latch retains the value until the next read of the CMCON0 register or the occurrence of a Reset. The other latch of the mismatch circuit is updated on every Q1 system clock. A mismatch condition will occur when a comparator output change is clocked through the second latch on the Q1 clock cycle. The mismatch condition will persist, holding the CxIF bit of the PIR1 register true, until either the CMCON0 register is read or the comparator output returns to the previous state.

Note:	A write operation to the CMCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.

Software will need to maintain information about the status of the comparator output to determine the actual change that has occurred.

The CxIF bit of the PIR1 register, is the comparator interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CxIE bit of the PIE1 register and the PEIE and GIE bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CxIF bit of the PIR1 register will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of CMCON0. This will end the mismatch condition. See Figures 7-8 and 7-9.
b) Clear the CxIF interrupt flag.

A persistent mismatch condition will preclude clearing the CxIF interrupt flag. Reading CMCON0 will end the mismatch condition and allow the CxIF bit to be cleared.

Note:	If a change in the CMCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF interrupt flag may not get set.

8.0 PROGRAMMABLE LOW-VOLTAGE DETECT (PLVD) MODULE

The Programmable Low-Voltage Detect (PLVD) module is a power supply detector which monitors the internal power supply. This module is typically used in key fobs and other devices, where certain actions need to be taken as a result of a falling battery voltage.

The PLVD module includes the following capabilities:

- Eight programmable trip points
- Interrupt on falling VDD
- Stable reference indication
- Operation during Sleep

A Block diagram of the PLVD module is shown in Figure 8-1.

FIGURE 8-1: PLVD BLOCK DIAGRAM

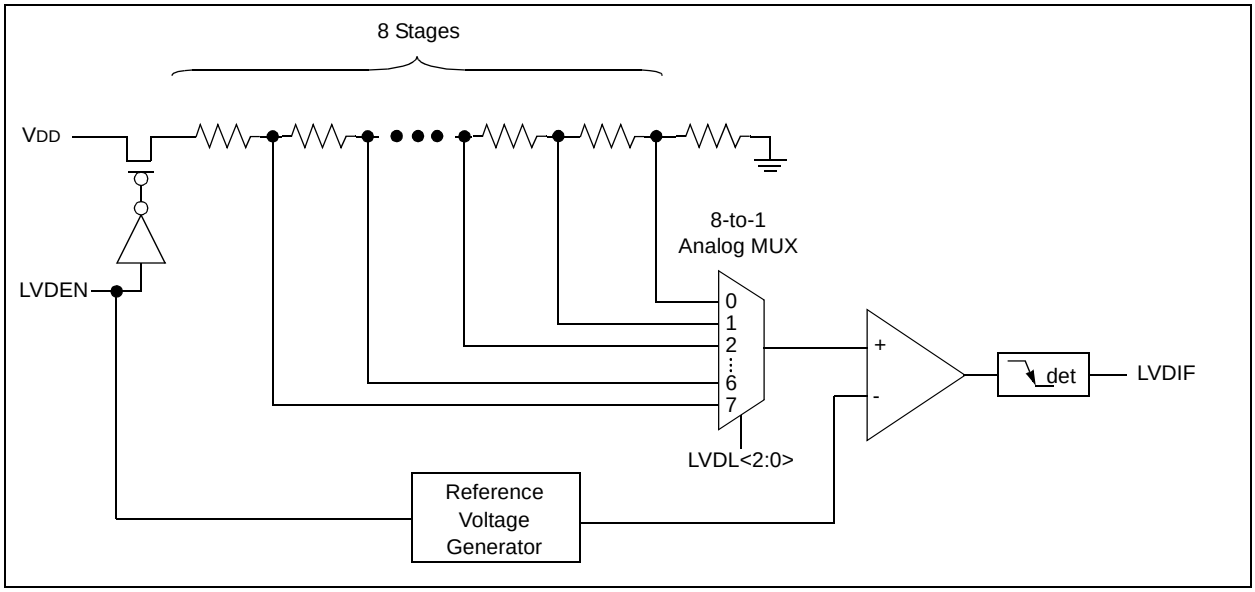
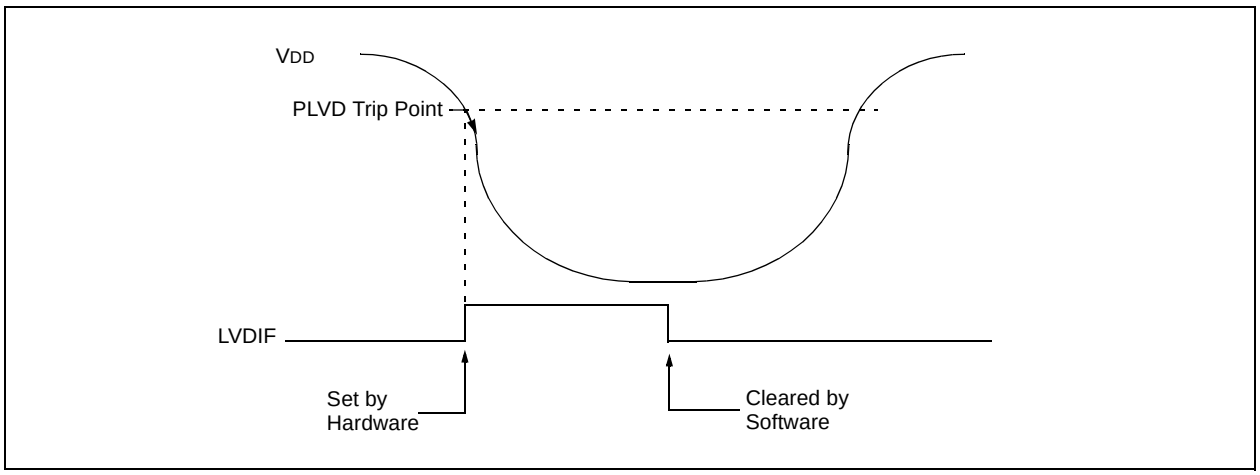


FIGURE 8-2: PLVD OPERATION



10.0 KEELOQ® COMPATIBLE CRYPTOGRAPHIC MODULE

To obtain information regarding the implementation of the KEELOQ module, Microchip Technology requires the execution of the "KEELOQ® Encoder License Agreement".

The "KEELOQ® Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ. Further information may be obtained by contacting your local Microchip Sales Representative.

NOTES:

REGISTER 11-2: CONFIGURATION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATOUT1	DATOUT0	LCXTUN5	LCXTUN4	LCXTUN3	LCXTUN2	LCXTUN1	LCXTUN0	R1PAR
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8-7 **DATOUT<1:0>:** LFDATA Output type bit
00 = Demodulated output
01 = Carrier Clock output
10 = RSSI output
11 = RSSI output

bit 6-1 **LCXTUN<5:0>:** LCX Tuning Capacitance bit
000000 = +0 pF (Default)
:
111111 = +63 pF

bit 0 **R1PAR**: Register Parity Bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

REGISTER 11-3: CONFIGURATION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSSIFET	CLKDIV	LCYTUN5	LCYTUN4	LCYTUN3	LCYTUN2	LCYTUN1	LCYTUN0	R2PAR
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8 **RSSIFET**: Pull-down MOSFET on LFDATA pad bit (controllable by user in the RSSI mode only)
1 = Pull-down RSSI MOSFET on
0 = Pull-down RSSI MOSFET off

bit 7 **CLKDIV:** Carrier Clock Divide-by bit
1 = Carrier Clock/4
0 = Carrier Clock/1

bit 6-1 **LCYTUN<5:0>:** LCY Tuning Capacitance bit
000000 = +0 pF (Default)
:
111111 = +63 pF

bit 0 **R2PAR**: Register Parity Bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

15.7 DC Characteristics: PIC16F639-I (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial Supply Voltage 2.0V ≤ VDD ≤ 3.6V				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VOH	**Output High Voltage**					
D090		I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 3.6V (Ind.)
D092		OSC2/CLKOUT (RC mode)	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 3.6V (Ind.) IOH = -1.0 mA, VDD = 3.6V (Ext.)
		Digital Output High Voltage					Analog Front-End (AFE) section
D093		LFDATA/SDIO for Analog Front-End (AFE)	VDD – 0.5	—	—	V	IOH = -400 µA, VDD = 2.0V
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	—	50*	pF	
D102	IULP	**Ultra Low-power Wake-up Current**	—	200	—	nA	
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh(1)	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 9.4.1 "Using the Data EEPROM"** for additional information

15.8 Thermal Considerations

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C						
Param No.	**Sym**	**Characteristic**		**Typ**	**Units**	**Conditions**
TH01	θJA	Thermal Resistance Junction to Ambient	PIC12F635	84.6	°C/W	8-pin PDIP package
				163.0	°C/W	8-pin SOIC package
				52.4	°C/W	8-pin DFN 4x4x0.9 mm package
				52.4	°C/W	8-pin DFN-S 6x5 mm package
			PIC16F636	69.8	°C/W	14-pin PDIP package
				85.0	°C/W	14-pin SOIC package
				100.4	°C/W	14-pin TSSOP package
				46.3	°C/W	16-pin QFN 4x0.9mm package
			PIC16F639	108.1	°C/W	20-pin SSOP package
TH02	θJC	Thermal Resistance Junction to Case	PIC12F635	41.2	°C/W	8-pin PDIP package
				38.8	°C/W	8-pin SOIC package
				3.0	°C/W	8-pin DFN 4x4x0.9 mm package
				3.0	°C/W	8-pin DFN-S 6x5 mm package
			PIC16F636	32.5	°C/W	14-pin PDIP package
				31.0	°C/W	14-pin SOIC package
				31.7	°C/W	14-pin TSSOP package
				2.6	°C/W	16-pin QFN 4x0.9mm package
			PIC16F639	32.2	°C/W	20-pin SSOP package
TH03	TJ	Junction Temperature		150	°C	For derated power calculations
TH04	PD	Power Dissipation		—	W	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation		—	W	PINTERNAL = IDD x VDD **(NOTE 1)**
TH06	PI/O	I/O Power Dissipation		—	W	PI/O = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH))
TH07	PDER	Derated Power		—	W	PDER = (TJ - TA)/θJA **(NOTE 2, 3)**

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature.

3: Maximum allowable power dissipation is the lower value of either the absolute maximum total power dissipation or derated power (PDER).

FIGURE 16-32: LFINTOSC FREQUENCY vs. VDD OVER TEMPERATURE (31 kHz)

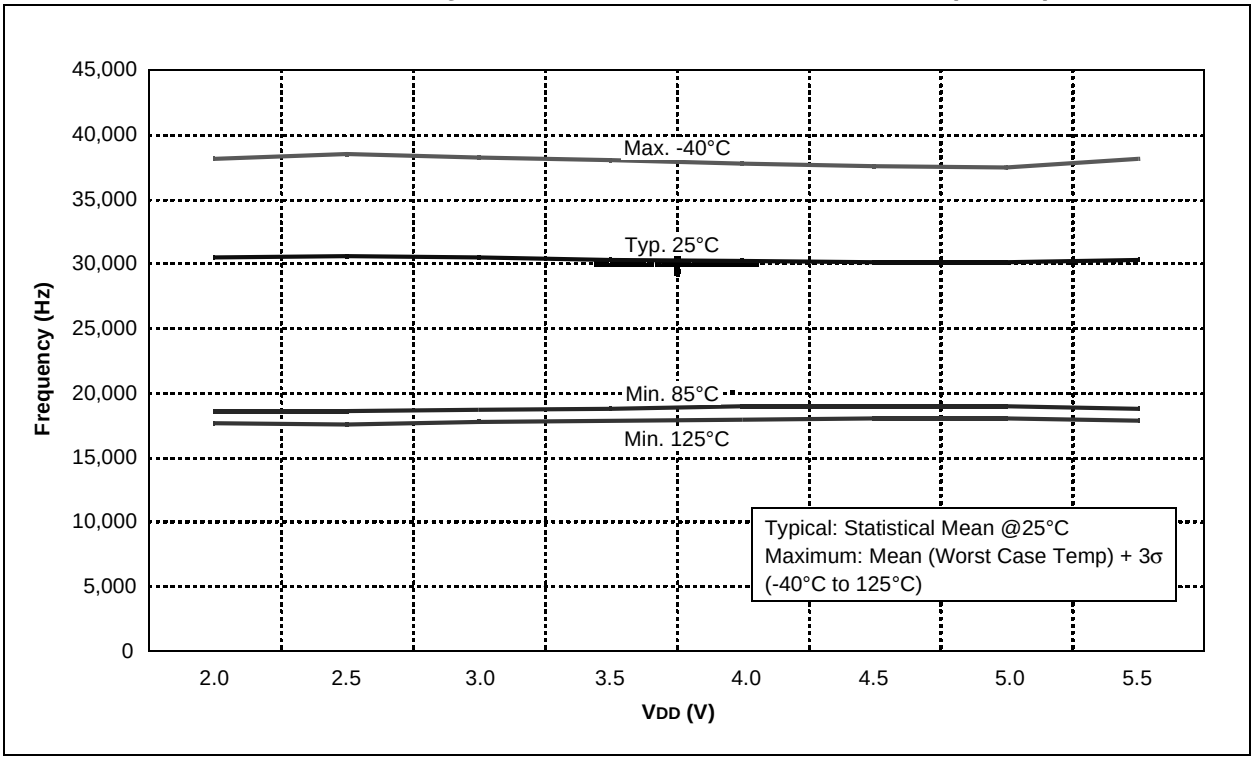
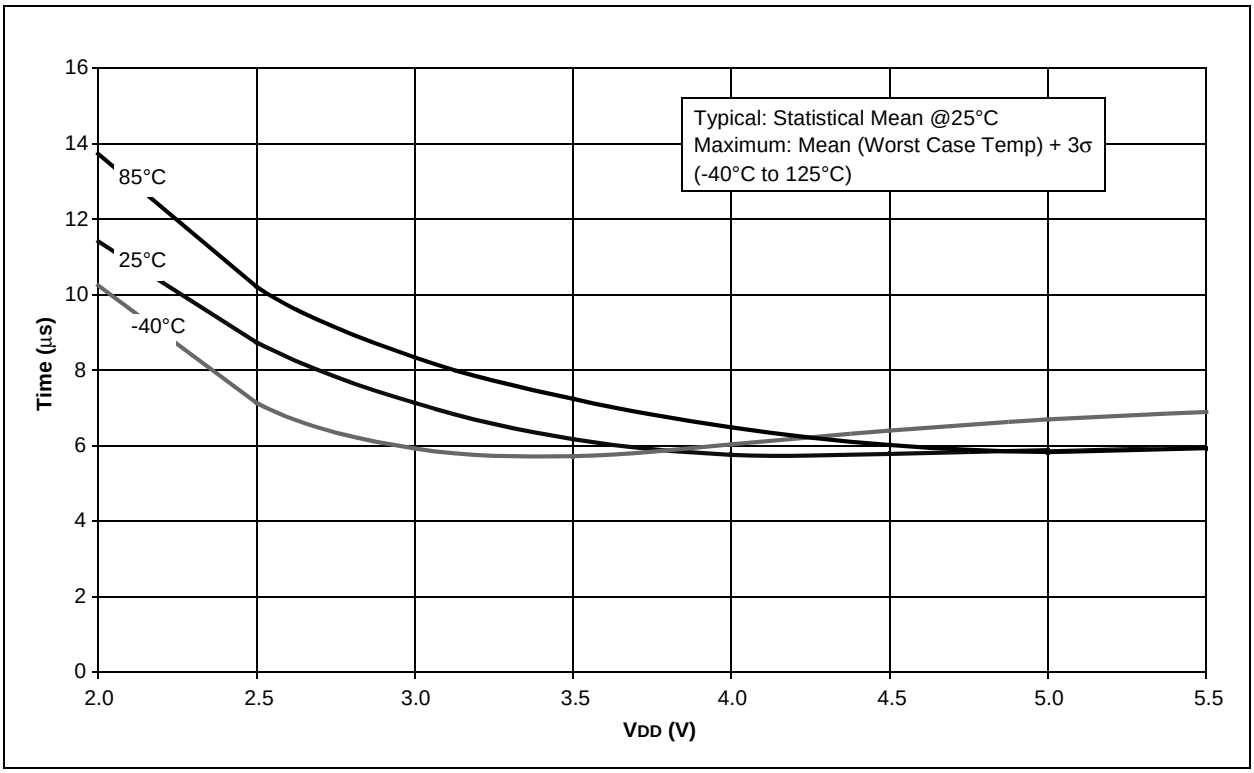
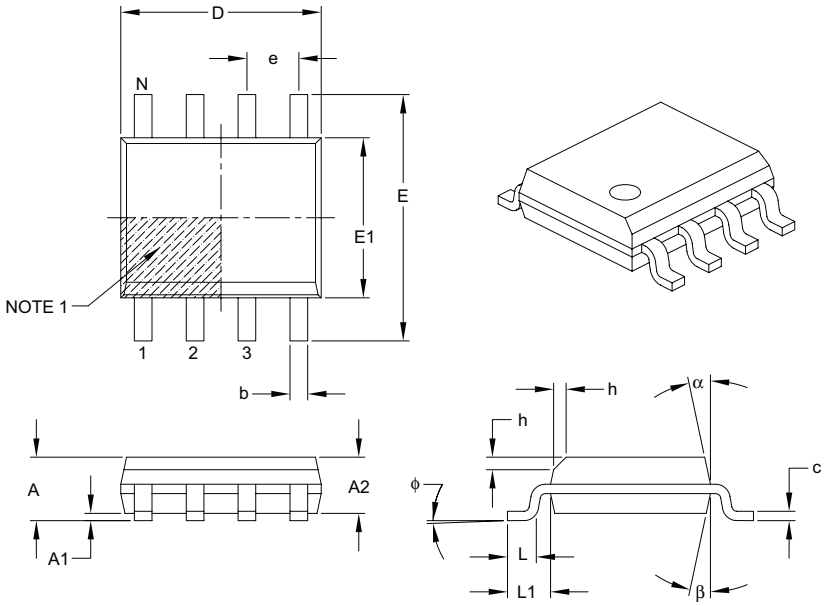


FIGURE 16-33: TYPICAL HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE



8-Lead Plastic Small Outline (SN or OA) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

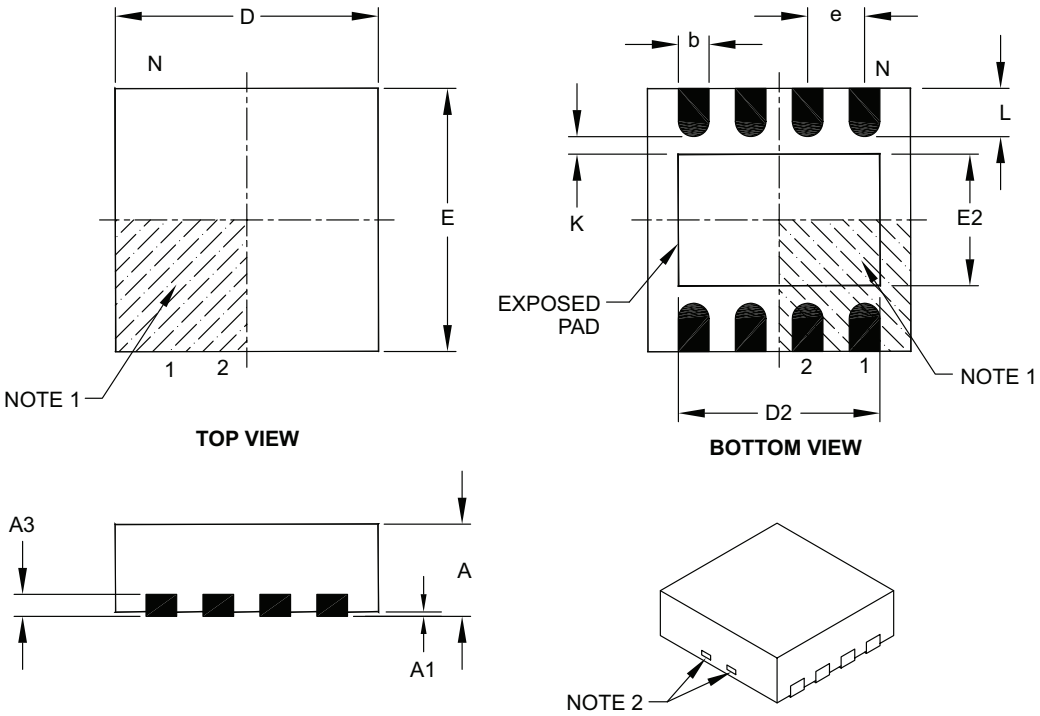
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.80 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Width	E2	0.00	2.20	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Length	D2	0.00	3.00	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.55	0.65
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

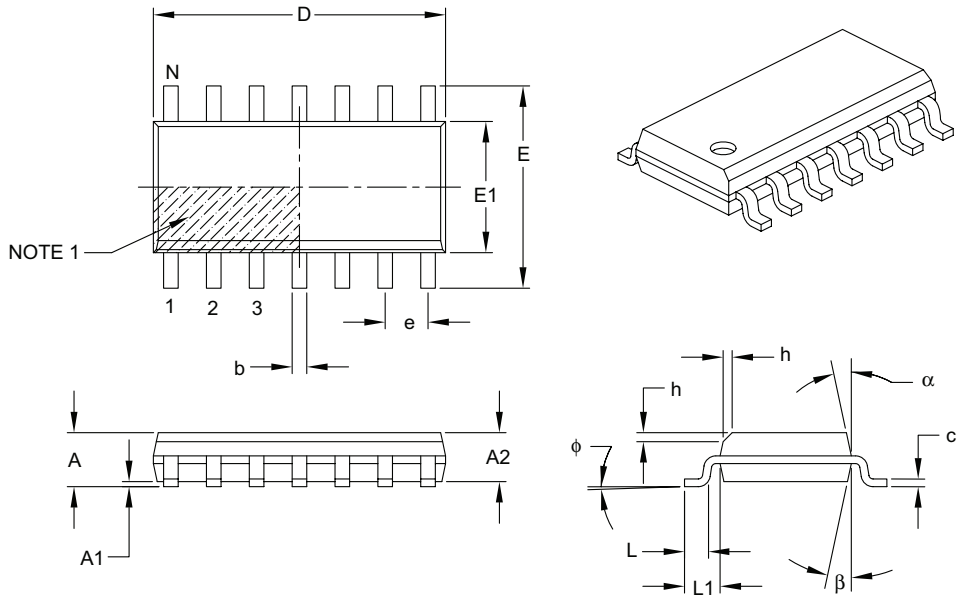
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131C

14-Lead Plastic Small Outline (SL or OD) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

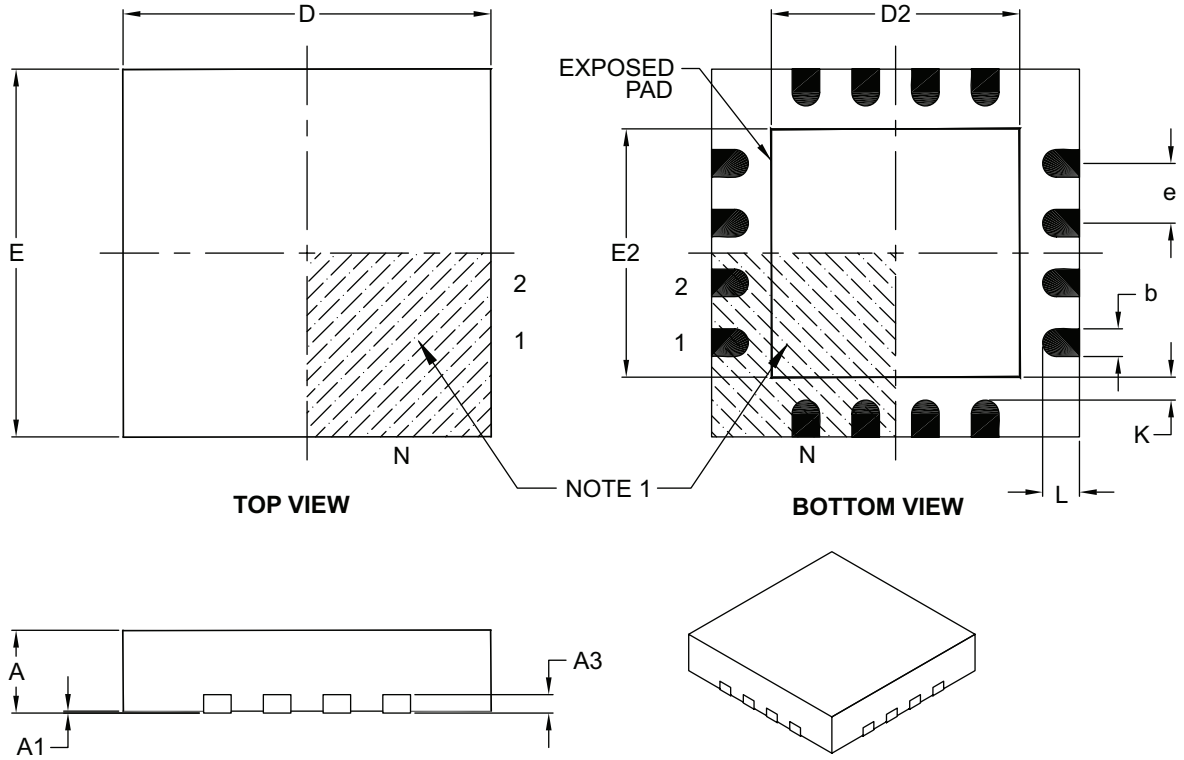
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

This is a new data sheet.

Revision B

Added PIC16F639 to the data sheet.

Revision C (12/2006)

Added Characterization data; Updated Package Drawings; Added Comparator Voltage Reference section.

Revision D (03/2007)

Replaced Package Drawings (Rev. AM); Replaced Development Support Section. Updated Product ID System.

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A

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C