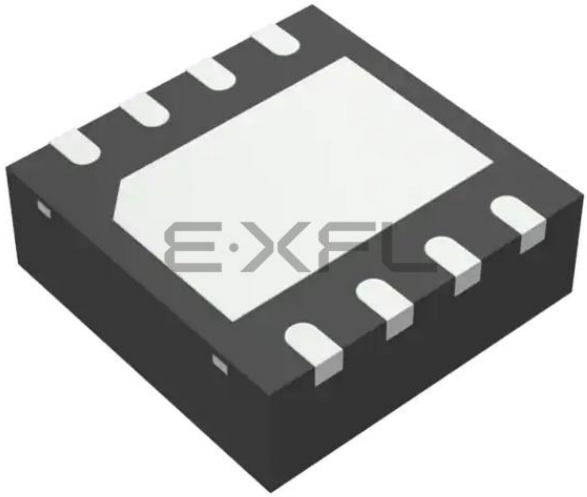

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN-S (6x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f635-i-mf

FIGURE 2-3: PIC12F635 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr.(1)	00h	Indirect addr.(1)	80h	Accesses 00h-0Bh	100h	Accesses 80h-8Bh	180h
TMR0	01h	OPTION_REG	81h		101h		181h
PCL	02h	PCL	82h		102h		182h
STATUS	03h	STATUS	83h		103h		183h
FSR	04h	FSR	84h		104h		184h
GPIO	05h	TRISIO	85h		105h		185h
	06h		86h		106h		186h
	07h		87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah		10Ah		18Ah
INTCON	0Bh	INTCON	8Bh		10Bh		18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
	0Dh		8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh		10Fh		18Fh
T1CON	10h	OSCTUNE	90h	CRCON	110h		190h
	11h		91h	CRDAT0(2)	111h		191h
	12h		92h	CRDAT1(2)	112h		192h
	13h		93h	CRDAT2(2)	113h		193h
	14h	LVDCON	94h	CRDAT3(2)	114h		194h
	15h	WPUDA	95h		115h		195h
	16h	IOCA	96h		116h		196h
	17h	WDA	97h		117h		197h
WDTCON	18h		98h		118h		198h
CMCON0	19h	VRCON	99h		119h		199h
CMCON1	1Ah	EEDAT	9Ah		11Ah		19Ah
	1Bh	EEADR	9Bh		11Bh		19Bh
	1Ch	EECON1	9Ch		11Ch		19Ch
	1Dh	EECON2(1)	9Dh		11Dh		19Dh
	1Eh		9Eh		11Eh		19Eh
	1Fh		9Fh		11Fh		19Fh
	20h – 3Fh		A0h – EFh		120h – 16Fh		1A0h – 1EFh
General Purpose Register 64 Bytes	40h – 7Fh	Accesses 70h-7Fh	F0h – FFh	Accesses 70h-7Fh	170h – 17Fh	Accesses Bank 0	1F0h – 1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: CRDAT<3:0> registers are KEELOQ® hardware peripheral related registers and require the execution of the "KEELOQ® Encoder License Agreement" regarding implementation of the module and access to related registers. The "KEELOQ® Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ or by contacting your local Microchip Sales Representative.

FIGURE 2-4: PIC16F636/639 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr.(1)	00h	Indirect addr. (1)	80h	Accesses 00h-0Bh	100h	Accesses 80h-8Bh	180h
TMR0	01h	OPTION_REG	81h		101h		181h
PCL	02h	PCL	82h		102h		182h
STATUS	03h	STATUS	83h		103h		183h
FSR	04h	FSR	84h		104h		184h
PORTA	05h	TRISA	85h		105h		185h
	06h		86h		106h		186h
PORTC	07h	TRISC	87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah		10Ah		18Ah
INTCON	0Bh	INTCON	8Bh		10Bh		18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
	0Dh		8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh		10Fh		18Fh
T1CON	10h	OSCTUNE	90h	CRCON	110h		190h
	11h		91h	CRDAT0(2)	111h		191h
	12h		92h	CRDAT1(2)	112h		192h
	13h		93h	CRDAT2(2)	113h		193h
	14h	LVDCON	94h	CRDAT3(2)	114h		194h
	15h	WPUDA	95h		115h		195h
	16h	IOCA	96h		116h		196h
	17h	WDA	97h		117h		197h
WDTCON	18h		98h		118h		198h
CMCON0	19h	VRCON	99h		119h		199h
CMCON1	1Ah	EEDAT	9Ah		11Ah		19Ah
	1Bh	EEADR	9Bh		11Bh		19Bh
	1Ch	EECON1	9Ch		11Ch		19Ch
	1Dh	EECON2(1)	9Dh		11Dh		19Dh
	1Eh		9Eh		11Eh		19Eh
	1Fh		9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 32 Bytes	A0h		120h		1A0h
			BFh				
			C0h				
			EFh		16Fh		1EFh
		Accesses 70h-7Fh	F0h	Accesses 70h-7Fh	170h	Accesses Bank 0	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: CRDAT<3:0> registers are KEELOQ hardware peripheral related registers and require the execution of the "KEELOQ® Encoder License Agreement" regarding implementation of the module and access to related registers. The "KEELOQ® Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ or by contacting your local Microchip Sales Representative.

TABLE 2-3: PIC16F636/639 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR/ WUR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32,137
01h	TMR0	Timer0 Module Register								xxxx xxxx	61,137
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	32,137
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	26,137
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	32,137
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xx00	48,137
06h	—	Unimplemented								—	—
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xx00	57,137
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	32,137
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(2)	0000 000x	28,137
0Ch	PIR1	EEIF	LVDIF	CRIF	C2IF	C1IF	OSFIF	—	TMR1IF	0000 00-0	30,137
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	64,137
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	64,137
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	68,137
11h	—	Unimplemented								—	—
12h	—	Unimplemented								—	—
13h	—	Unimplemented								—	—
14h	—	Unimplemented								—	—
15h	—	Unimplemented								—	—
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	144,137
19h	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	79,137
1Ah	CMCON1	—	—	—	—	—	—	T1GSS	C2SYNC	---- --10	82,137
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	—	Unimplemented								—	—
1Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset but will set again if the mismatch exists.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (GPR and SFR)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS,` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF, BSF, SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see **Section 13.0 "Instruction Set Summary"**

Note 1: The C and DC bits operate as a $\overline{Borrow}$ and Digit $\overline{Borrow}$ out bit, respectively, in subtraction.

REGISTER 2-1: STATUS: STATUS REGISTER

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
`1` = Bank 2, 3 (100h-1FFh)
`0` = Bank 0, 1 (00h-FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
`00` = Bank 0 (00h-7Fh)
`01` = Bank 1 (80h-FFh)
`10` = Bank 2 (100h-17Fh)
`11` = Bank 3 (180h-1FFh)

bit 4 **$\overline{TO}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Borrow}$ bit (`ADDWF, ADDLW, SUBLW, SUBWF` instructions)(1)
`1` = A carry-out from the 4th low-order bit of the result occurred
`0` = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF, ADDLW, SUBLW, SUBWF` instructions)(1)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF, RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

3.4.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 3-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

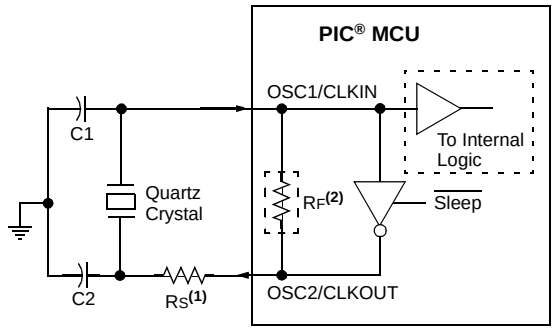
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 3-3 and Figure 3-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 3-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: A series resistor (RS) may be required for quartz crystals with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

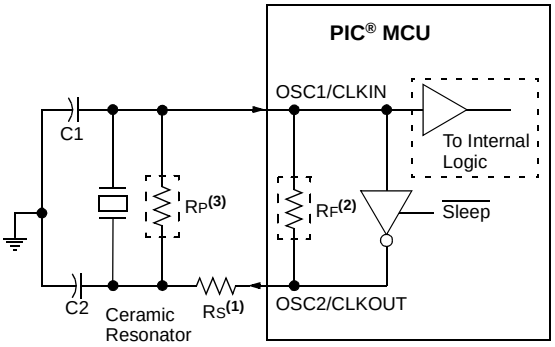
Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Applications Notes:

- AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826)
- AN849, "*Basic PIC® Oscillator Design*" (DS00849)
- AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)
- AN949, "*Making Your Oscillator Work*" (DS00949)

FIGURE 3-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (RS) may be required for ceramic resonators with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

4.0 I/O PORTS

There are as many as twelve general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

4.1 PORTA and the TRISA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 4-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). The exception is RA3, which is input only and its TRIS bit will always read as '1'. Example 4-1 shows how to initialize PORTA.

Note:	PORTA = GPIO TRISA = TRISIO

Reading the PORTA register (Register 4-1) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. RA3 reads '0' when MCLRE = 1.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

Note:	The CMCON0 register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 4-1: INITIALIZING PORTA

```
BANKSEL PORTA          ;
CLRF    PORTA          ;Init PORTA
MOVLW   07h            ;Set RA<2:0> to
MOVWF   CMCON0         ;digital I/O
BSF     STATUS,RP0     ;Bank 1
BCF     STATUS,RP1     ;
MOVLW   0Ch            ;Set RA<3:2> as inputs
MOVWF   TRISA          ;and set RA<5:4,1:0>
                       ;as outputs
```

4.2 Additional Pin Functions

Every PORTA pin on the PIC12F635/PIC16F636/639 has an interrupt-on-change option and a weak pull-up/pull-down option. RA0 has an Ultra Low-Power Wake-up option. The next three sections describe these functions.

4.2.1 WEAK PULL-UP/PULL-DOWN

Each of the PORTA pins, except RA3, has an internal weak pull-up and pull-down. The WDA bits select either a pull-up or pull-down for an individual port bit. Individual control bits can turn on the pull-up or pull-down. These pull-ups/pull-downs are automatically turned off when the port pin is configured as an output, as an alternate function or on a Power-on Reset, setting the $\overline{\text{RAPU}}$ bit of the OPTION register. A weak pull-up on RA3 is enabled when configured as $\overline{\text{MCLR}}$ in the Configuration Word register and disabled when high voltage is detected, to reduce current consumption through RA3, while in Programming mode.

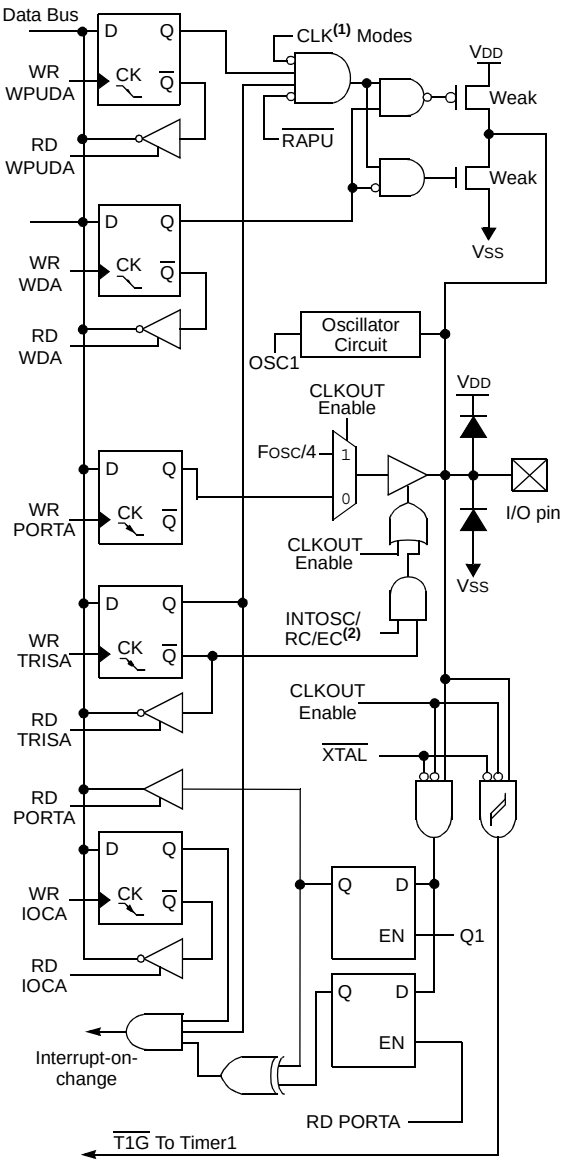
Note:	PORTA = GPIO TRISA = TRISIO

4.2.4.5 RA4/$\overline{T1G}$/OSC2/CLKOUT

Figure 4-5 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 gate input
- a crystal/resonator connection
- a clock output

FIGURE 4-5: BLOCK DIAGRAM OF RA4



Note 1: Oscillator modes are XT, HS, LP, LPTMR1 and CLKOUT Enable.

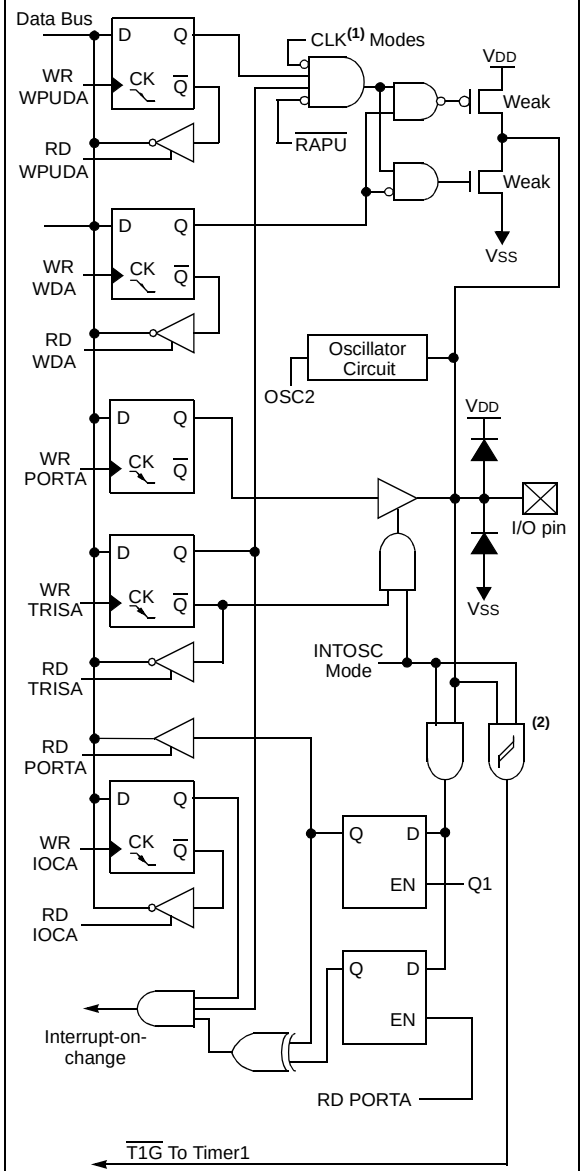
2: With CLKOUT option.

4.2.4.6 RA5/T1CKI/OSC1/CLKIN

Figure 4-6 shows the diagram for this pin. The RA5 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 clock input
- a crystal/resonator connection
- a clock input

FIGURE 4-6: BLOCK DIAGRAM OF RA5

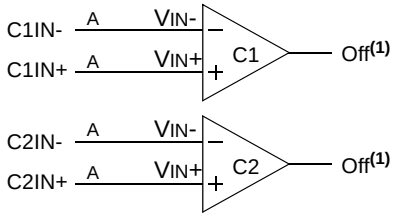


Note 1: Oscillator modes are XT, HS, LP and LPTMR1.

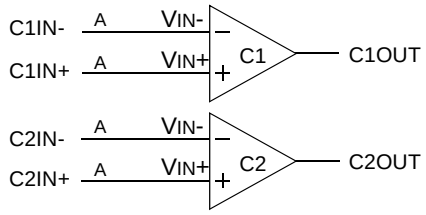
2: When using Timer1 with LP oscillator, the Schmitt Trigger is bypassed.

FIGURE 7-7: COMPARATOR I/O OPERATING MODES (PIC16F636/639)

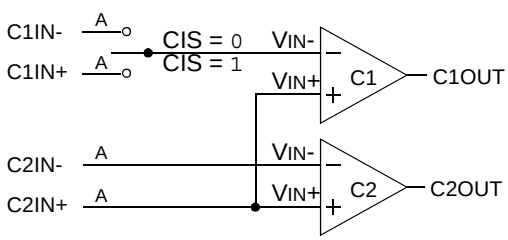
Comparators Reset (POR Default Value)
CM<2:0> = 000



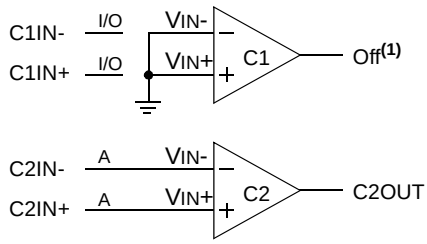
Two Independent Comparators
CM<2:0> = 100



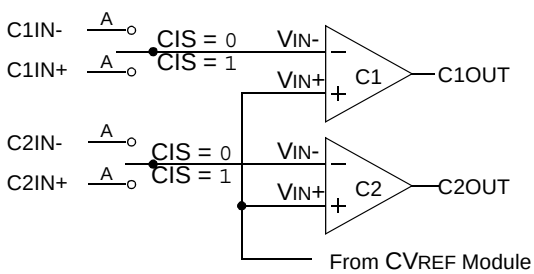
Three Inputs Multiplexed to Two Comparators
CM<2:0> = 001



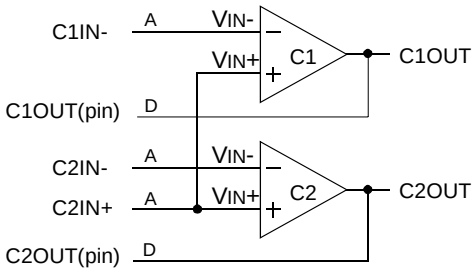
One Independent Comparator
CM<2:0> = 101



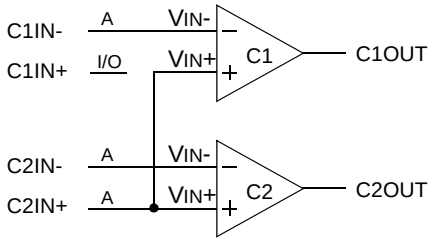
Four Inputs Multiplexed to Two Comparators
CM<2:0> = 010



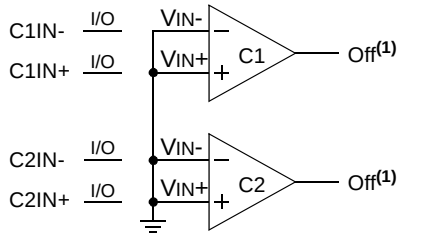
Two Common Reference Comparators with Outputs
CM<2:0> = 110



Two Common Reference Comparators
CM<2:0> = 011



Comparators Off (Lowest Power)
CM<2:0> = 111



Legend: A = Analog Input, ports always reads '0'
CIS = Comparator Input Switch (CMCON0<3>)
I/O = Normal port I/O
D = Comparator Digital Output

Note 1: Reads as '0', unless CxINV = 1.

8.0 PROGRAMMABLE LOW-VOLTAGE DETECT (PLVD) MODULE

The Programmable Low-Voltage Detect (PLVD) module is a power supply detector which monitors the internal power supply. This module is typically used in key fobs and other devices, where certain actions need to be taken as a result of a falling battery voltage.

The PLVD module includes the following capabilities:

- Eight programmable trip points
- Interrupt on falling VDD
- Stable reference indication
- Operation during Sleep

A Block diagram of the PLVD module is shown in Figure 8-1.

FIGURE 8-1: PLVD BLOCK DIAGRAM

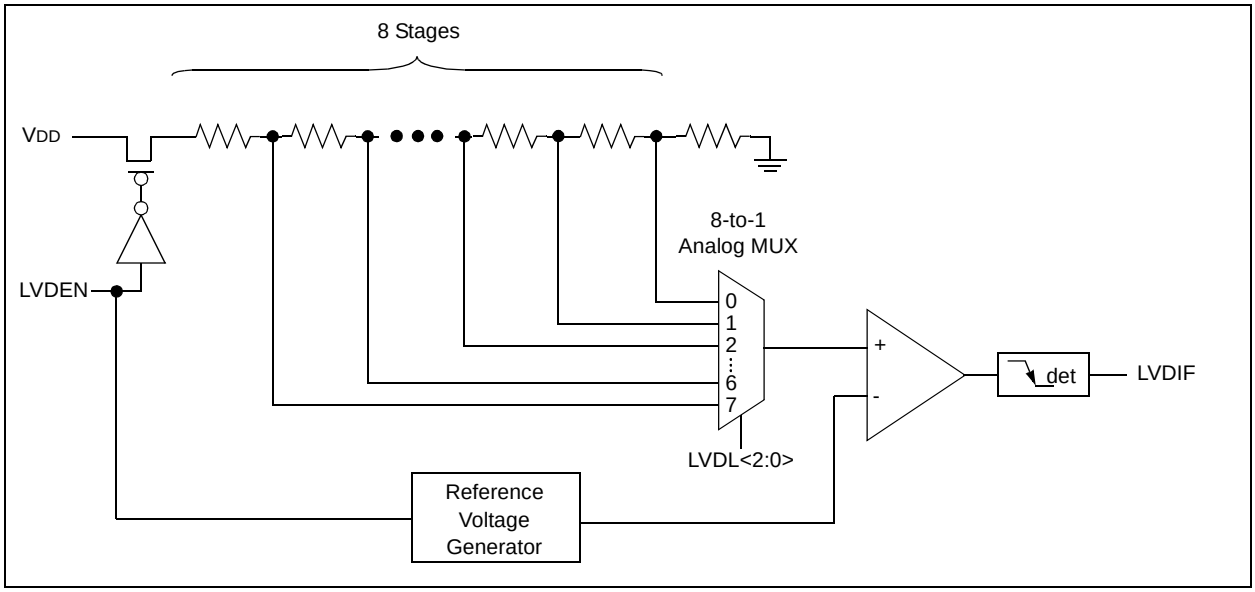
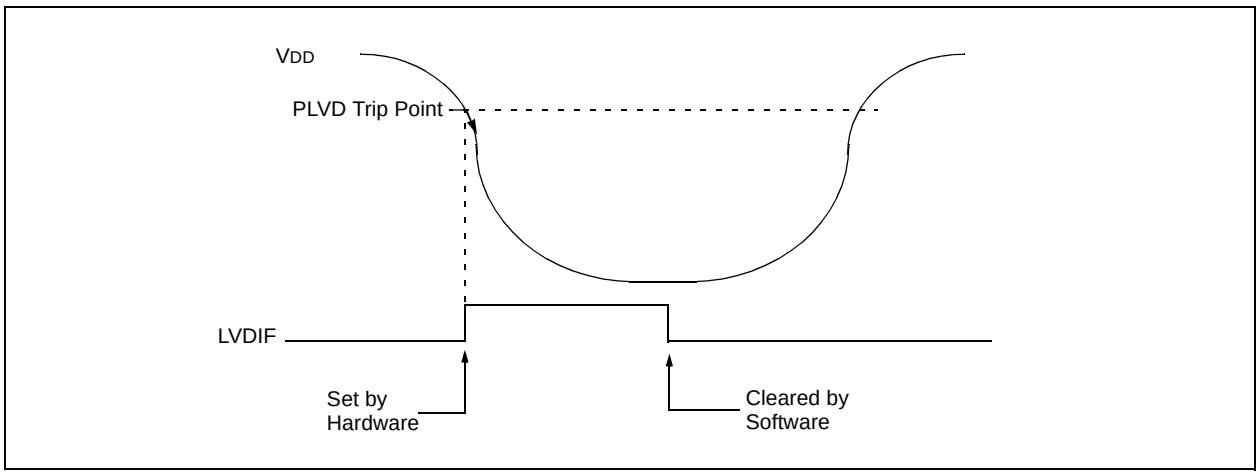


FIGURE 8-2: PLVD OPERATION



11.0 ANALOG FRONT-END (AFE) FUNCTIONAL DESCRIPTION (PIC16F639 ONLY)

The PIC16F639 device consists of the PIC16F636 device and low frequency (LF) Analog Front-End (AFE), with the AFE section containing three analog-input channels for signal detection and LF talk-back. This section describes the Analog Front-End (AFE) in detail.

The PIC16F639 device can detect a 125 kHz input signal as low as 1 mVpp and transmit data by using internal LF talk-back modulation or via an external transmitter. The PIC16F639 can also be used for various bidirectional communication applications. Figure 11-3 and Figure 11-4 show application examples of the device.

Each analog input channel has internal tuning capacitance, sensitivity control circuits, an input signal strength limiter and an LF talk-back modulation transistor. An Automatic Gain Control (AGC) loop is used for all three input channel gains. The output of each channel is OR'd and fed into a demodulator. The digital output is passed to the LFDATA pin. Figure 11-1 shows the block diagram of the AFE and Figure 11-2 shows the LC input path.

There are a total of eight Configuration registers. Six of them are used for AFE operation options, one for column parity bits and one for status indication of AFE operation. Each register has 9 bits including one row parity bit. These registers are readable and writable by SPI (Serial Protocol Interface) commands except for the STATUS register, which is read-only.

11.1 RF Limiter

The RF Limiter limits LC pin input voltage by de-Q'ing the attached LC resonant circuit. The absolute voltage limit is defined by the silicon process's maximum allowed input voltage (see **Section 15.0 "Electrical Specifications"**). The limiter begins de-Q'ing the external LC antenna when the input voltage exceeds V_{DE_Q}, progressively de-Q'ing harder to reduce the antenna input voltage.

The signal levels from all 3 channels are combined such that the limiter attenuates all 3 channels uniformly, in respect to the channel with the strongest signal.

11.2 Modulation Circuit

The modulation circuit consists of a modulation transistor (FET), internal tuning capacitors and external LC antenna components. The modulation transistor and the internal tuning capacitors are connected between the LC input pin and LCCOM pin. Each LC input has its own modulation transistor.

When the modulation transistor turns on, its low Turn-on Resistance (R_M) clamps the induced LC antenna voltage. The coil voltage is minimized when the modulation transistor turns-on and maximized when the modulation transistor turns-off. The modulation transistor's low Turn-on Resistance (R_M) results in a high modulation depth.

The LF talk-back is achieved by turning on and off the modulation transistor.

The modulation data comes from the microcontroller section via the digital SPI interface as "Clamp On", "Clamp Off" commands. Only those inputs that are enabled will execute the clamp command. A basic block diagram of the modulation circuit is shown in Figure 11-1 and Figure 11-2.

The modulation FET is also shorted momentarily after Soft Reset and Inactivity timer time-out.

11.3 Tuning Capacitor

Each channel has internal tuning capacitors for external antenna tuning. The capacitor values are programmed by the Configuration registers up to 63 pF, 1 pF per step.

Note:	The user can control the tuning capacitor by programming the AFE Configuration registers.

11.4 Variable Attenuator

The variable attenuator is used to attenuate, via AGC control, the input signal voltage to avoid saturating the amplifiers and demodulators.

Note:	The variable attenuator function is accomplished by the device itself. The user cannot control its function.

11.5 Sensitivity Control

The sensitivity of each channel can be reduced by the channel's Configuration register sensitivity setting. This is used to desensitize the channel from optimum.

Note:	The user can desensitize the channel sensitivity by programming the AFE Configuration registers.

11.6 AGC Control

The AGC controls the variable attenuator to limit the internal signal voltage to avoid saturation of internal amplifiers and demodulators (Refer to **Section 11.4 "Variable Attenuator"**).

The signal levels from all 3 channels are combined such that AGC attenuates all 3 channels uniformly in respect to the channel with the strongest signal.

Note:	The AGC control function is accomplished by the device itself. The user cannot control its function.

11.7 Fixed Gain Amplifiers 1 and 2

FGA1 and FGA2 provides a maximum two-stage gain of 40 dB.

Note:	The user cannot control the gain of these two amplifiers.

11.8 Auto Channel Selection

The Auto Channel Selection feature is enabled if the Auto Channel Select bit AUTOCHSEL<8> in Configuration Register 5 (Register 11-6) is set, and disabled if the bit is cleared. When this feature is active (i.e., AUTOCHSE <8> = 1), the control circuit checks the demodulator output of each input channel immediately after the AGC settling time (T_{STAB}). If the output is high, it allows this channel to pass data, otherwise it is blocked.

The status of this operation is monitored by AFE Status Register 7 bits <8:6> (Register 11-8). These bits indicate the current status of the channel selection activity, and automatically updates for every Soft Reset period. The auto channel selection function resets after each Soft Reset (or after Inactivity timer time-out). Therefore, the blocked channels are reenabled after Soft Reset.

This feature can make the output signal cleaner by blocking any channel that was not high at the end of T_{AGC}. This function works only for demodulated data output, and is not applied for carrier clock or RSSI output.

11.9 Carrier Clock Detector

The Detector senses the input carrier cycles. The output of the Detector switches digitally at the signal carrier frequency. Carrier clock output is available when the output is selected by the DATOUT bit in the AFE Configuration Register 1 (Register 11-2).

11.10 Demodulator

The Demodulator consists of a full-wave rectifier, low pass filter, peak detector and Data Slicer that detects the envelope of the input signal.

11.11 Data Slicer

The Data Slicer consists of a reference generator and comparator. The Data Slicer compares the input with the reference voltage. The reference voltage comes from the minimum modulation depth requirement setting and input peak voltage. The data from all 3 channels are OR'd together and sent to the output enable filter.

11.12 Output Enable Filter

The Output Enable Filter enables the LFDATA output once the incoming signal meets the wake-up sequence requirements (see **Section 11.15 "Configurable Output Enable Filter"**).

11.13 RSSI (Received Signal Strength Indicator)

The RSSI provides a current which is proportional to the input signal amplitude (see **Section 11.31.3 "Received Signal Strength Indicator (RSSI) Output"**).

11.14 Analog Front-End Timers

The AFE has an internal 32 kHz RC oscillator. The oscillator is used in several timers:

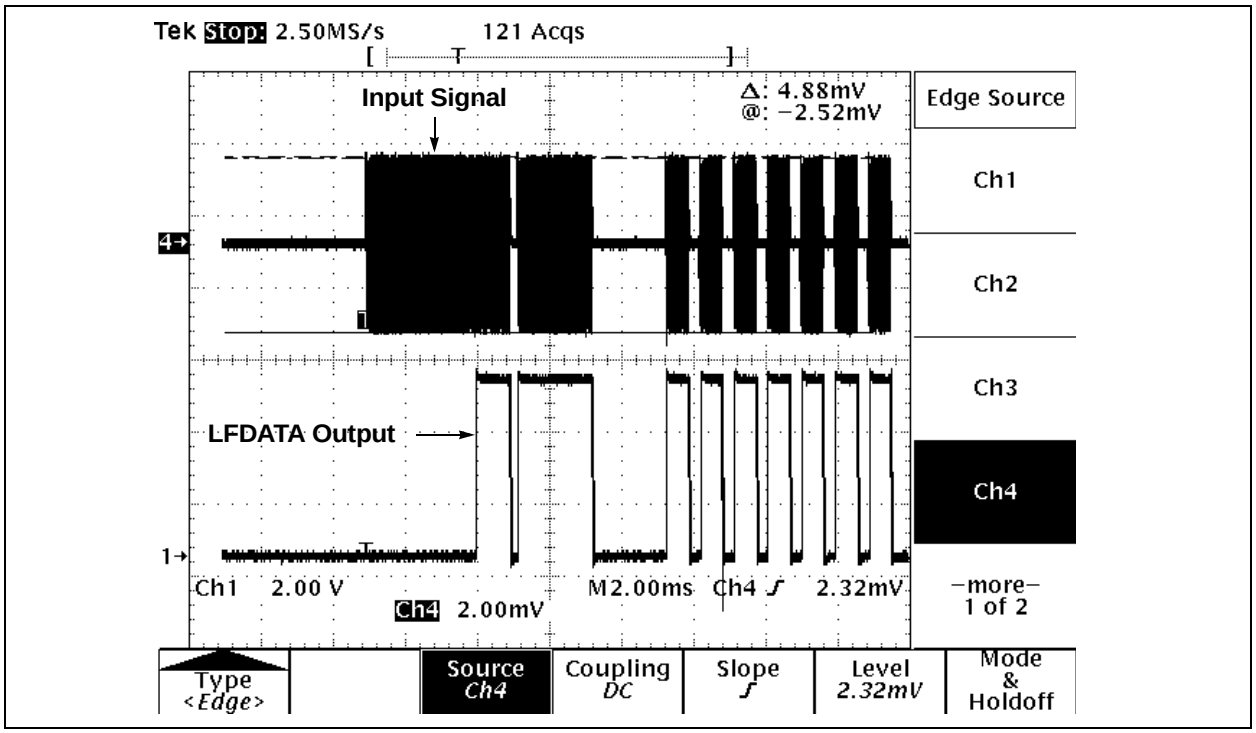
- Inactivity timer
- Alarm timer
- Pulse Width timer
- Period timer
- AGC settling timer

11.14.1 RC OSCILLATOR

The RC oscillator is low power, 32 kHz ± 10% over temperature and voltage variations.

Case I. When Output Enable Filter is disabled: Demodulated output is available immediately after the AGC stabilization time (TAGC). Figure 11-10 shows an example of demodulated output when the Output Enable Filter is disabled.

FIGURE 11-10: INPUT SIGNAL AND DEMODULATOR OUTPUT WHEN THE OUTPUT ENABLE FILTER IS DISABLED



Case II. When Output Enable Filter is enabled: Demodulated output is available only if the incoming signal meets the enable filter timing criteria that is defined in the Configuration Register 0 (Register 11-1). If the criteria is met, the output is available after the low timing (TOEL) of the Enable Filter. Figure 11-11 and Figure 11-12 shows examples of demodulated output when the Output Enable Filter is enabled.

TABLE 11-6: ANALOG FRONT-END CONFIGURATION REGISTERS SUMMARY

Register Name	Address	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration Register 0	0000	OEH		OEL		ALRTIND	LCZEN	LCYEN	LCXEN	R0PAR
Configuration Register 1	0001	DATOUT		Channel X Tuning Capacitor						R1PAR
Configuration Register 2	0010	RSSIFET	CLKDIV	Channel Y Tuning Capacitor						R2PAR
Configuration Register 3	0011	Unimplemented		Channel Z Tuning Capacitor						R3PAR
Configuration Register 4	0100	Channel X Sensitivity Control				Channel Y Sensitivity Control				R4PAR
Configuration Register 5	0101	AUTOCHSEL	AGCSIG	MODMIN	MODMIN	Channel Z Sensitivity Control				R5PAR
Column Parity Register 6	0110	Column Parity Bits								R6PAR
AFE Status Register 7	0111	Active Channel Indicators			AGCACT	Wake-up Channel Indicators			ALARM	PEI

REGISTER 11-1: CONFIGURATION REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OEH1	OEH0	OEL1	OEL0	ALRTIND	LCZEN	LCYEN	LCXEN	R0PAR
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 8-7 **OEH<1:0>**: Output Enable Filter High Time (TOEH) bit
00 = Output Enable Filter disabled (no wake-up sequence required, passes all signal to LFDATA)
01 = 1 ms
10 = 2 ms
11 = 4 ms

bit 6-5 **OEL<1:0>**: Output Enable Filter Low Time (TOEL) bit
00 = 1 ms
01 = 1 ms
10 = 2 ms
11 = 4 ms

bit 4 **ALRTIND**: $\overline{\text{ALERT}}$ bit, output triggered by:
1 = Parity error and/or expired Alarm timer (receiving noise, see **Section 11.14.3 “Alarm Timer”**)
0 = Parity error

bit 3 **LCZEN:** LCZ Enable bit
1 = Disabled
0 = Enabled

bit 2 **LCYEN:** LCY Enable bit
1 = Disabled
0 = Enabled

bit 1 **LCXEN:** LCX Enable bit
1 = Disabled
0 = Enabled

bit 0 **R0PAR**: Register Parity bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

12.2 Reset

The PIC12F635/PIC16F636/639 differentiates between various kinds of Reset:

a) Power-on Reset (POR)
b) Wake-up Reset (WUR)
c) WDT Reset during normal operation
d) WDT Reset during Sleep
e) $\overline{\text{MCLR}}$ Reset during normal operation
f) $\overline{\text{MCLR}}$ Reset during Sleep
g) Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

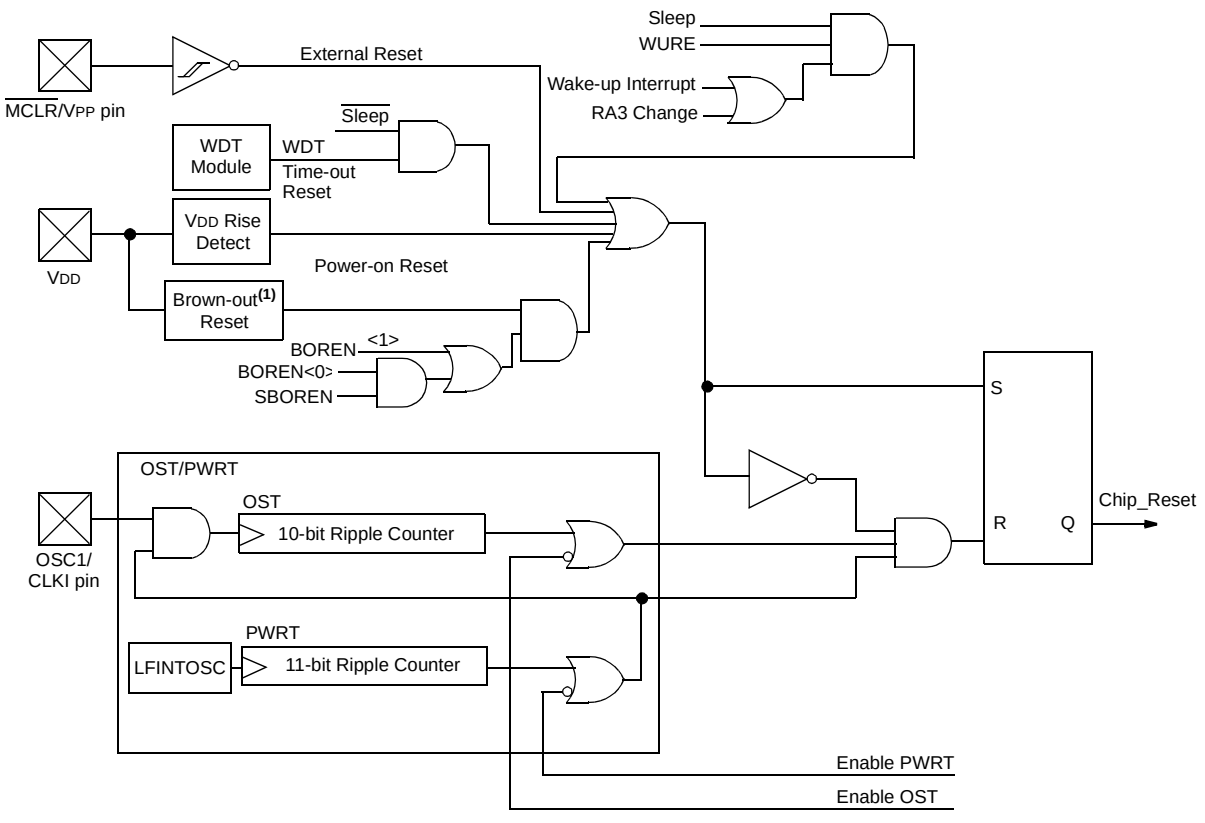
- Power-on Reset
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset

They are not affected by a WDT wake-up since this is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 12-3. These bits are used in software to determine the nature of the Reset. See Table 12-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 12-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 15.0 "Electrical Specifications"** for pulse width specifications.

FIGURE 12-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: Refer to the Configuration Word register (Register 12-1).

12.3 Power-on Reset

The on-chip POR circuit holds the chip in Reset until V_{DD} has reached a high enough level for proper operation. To take advantage of the POR, simply connect the $\overline{MCLR}$ pin through a resistor to V_{DD}. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for V_{DD} is required. See **Section 15.0 "Electrical Specifications"** for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until V_{DD} reaches V_{BOD} (see **Section 12.6 "Brown-out Reset (BOR)"**).

Note:	The POR circuit does not produce an internal Reset when V_{DD} declines. To re-enable the POR, V_{DD} must reach V_{SS} for a minimum of 100 µs.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to the Application Note *AN607, "Power-up Trouble Shooting"* (DS00607).

12.4 Wake-up Reset (WUR)

The PIC12F635/PIC16F636/639 has a modified wake-up from Sleep mechanism. When waking from Sleep, the WUR function resets the device and releases Reset when V_{DD} reaches an acceptable level.

If the $\overline{WURE}$ bit is enabled ('0') in the Configuration Word register, the device will Wake-up Reset from Sleep through one of the following events:

1. On any event that causes a wake-up event. The peripheral must be enabled to generate an interrupt or wake-up, GIE state is ignored.
2. When WURE is enabled, RA3 will always generate an interrupt-on-change signal during Sleep.

The $\overline{WUR}$, $\overline{POR}$ and $\overline{BOR}$ bits in the PCON register and the $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device Reset.

To allow WUR upon RA3 change:

1. Enable the WUR function, $\overline{WURE}$ Configuration Bit = 0.
2. Enable RA3 as an input, MCLRE Configuration Bit = 0.
3. Read PORTA to establish the current state of RA3.
4. Execute SLEEP instruction.
5. When RA3 changes state, the device will wake-up and then reset. The $\overline{WUR}$ bit in PCON will be cleared to '0'.

12.4.1 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from the 31 kHz LFINTOSC oscillator. For more information, see **Section 3.5 "Internal Clock Modes"**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level. A Configuration bit, $\overline{PWRTE}$, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip due to:

- V_{DD} variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 15.0 "Electrical Specifications"**).

Note:	Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

12.5 $\overline{MCLR}$

PIC12F635/PIC16F636/639 has a noise filter in the $\overline{MCLR}$ Reset path. The filter will ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{MCLR}$ pin low. See Figure 12-2 for the recommended $\overline{MCLR}$ circuit.

An internal $\overline{MCLR}$ option is enabled by clearing the MCLRE bit in the Configuration Word register. When cleared, $\overline{MCLR}$ is internally tied to V_{DD} and an internal weak pull-up is enabled for the $\overline{MCLR}$ pin. In-Circuit Serial Programming is not affected by selecting the internal $\overline{MCLR}$ option.

BTFSS **Bit Test f, Skip if Set**

Syntax:	[*label*] BTFSS f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a two-cycle instruction.

CALL **Call Subroutine**

Syntax:	[*label*] CALL k
Operands:	0 ≤ k ≤ 2047
Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>
Status Affected:	None
Description:	Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

CLRF **Clear f**

Syntax:	[*label*] CLRF f
Operands:	0 ≤ f ≤ 127
Operation:	00h → (f) 1 → Z
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

CLRW **Clear W**

Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W) 1 → Z
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

CLRWDT **Clear Watchdog Timer**

Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT 0 → WDT prescaler, 1 → $\overline{TO}$ 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

COMF **Complement f**

Syntax:	[*label*] COMF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	($\bar{f}$) → (destination)
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

DECF **Decrement f**

Syntax:	[*label*] DECF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) - 1 → (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

15.8 Thermal Considerations

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C						
Param No.	**Sym**	**Characteristic**		**Typ**	**Units**	**Conditions**
TH01	θJA	Thermal Resistance Junction to Ambient	PIC12F635	84.6	°C/W	8-pin PDIP package
				163.0	°C/W	8-pin SOIC package
				52.4	°C/W	8-pin DFN 4x4x0.9 mm package
				52.4	°C/W	8-pin DFN-S 6x5 mm package
			PIC16F636	69.8	°C/W	14-pin PDIP package
				85.0	°C/W	14-pin SOIC package
				100.4	°C/W	14-pin TSSOP package
				46.3	°C/W	16-pin QFN 4x0.9mm package
			PIC16F639	108.1	°C/W	20-pin SSOP package
TH02	θJC	Thermal Resistance Junction to Case	PIC12F635	41.2	°C/W	8-pin PDIP package
				38.8	°C/W	8-pin SOIC package
				3.0	°C/W	8-pin DFN 4x4x0.9 mm package
				3.0	°C/W	8-pin DFN-S 6x5 mm package
			PIC16F636	32.5	°C/W	14-pin PDIP package
				31.0	°C/W	14-pin SOIC package
				31.7	°C/W	14-pin TSSOP package
				2.6	°C/W	16-pin QFN 4x0.9mm package
			PIC16F639	32.2	°C/W	20-pin SSOP package
TH03	TJ	Junction Temperature		150	°C	For derated power calculations
TH04	PD	Power Dissipation		—	W	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation		—	W	PINTERNAL = IDD x VDD **(NOTE 1)**
TH06	PI/O	I/O Power Dissipation		—	W	PI/O = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH))
TH07	PDER	Derated Power		—	W	PDER = (TJ - TA)/θJA **(NOTE 2, 3)**

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature.

3: Maximum allowable power dissipation is the lower value of either the absolute maximum total power dissipation or derated power (PDER).

FIGURE 16-30: COMPARATOR RESPONSE TIME (RISING EDGE)

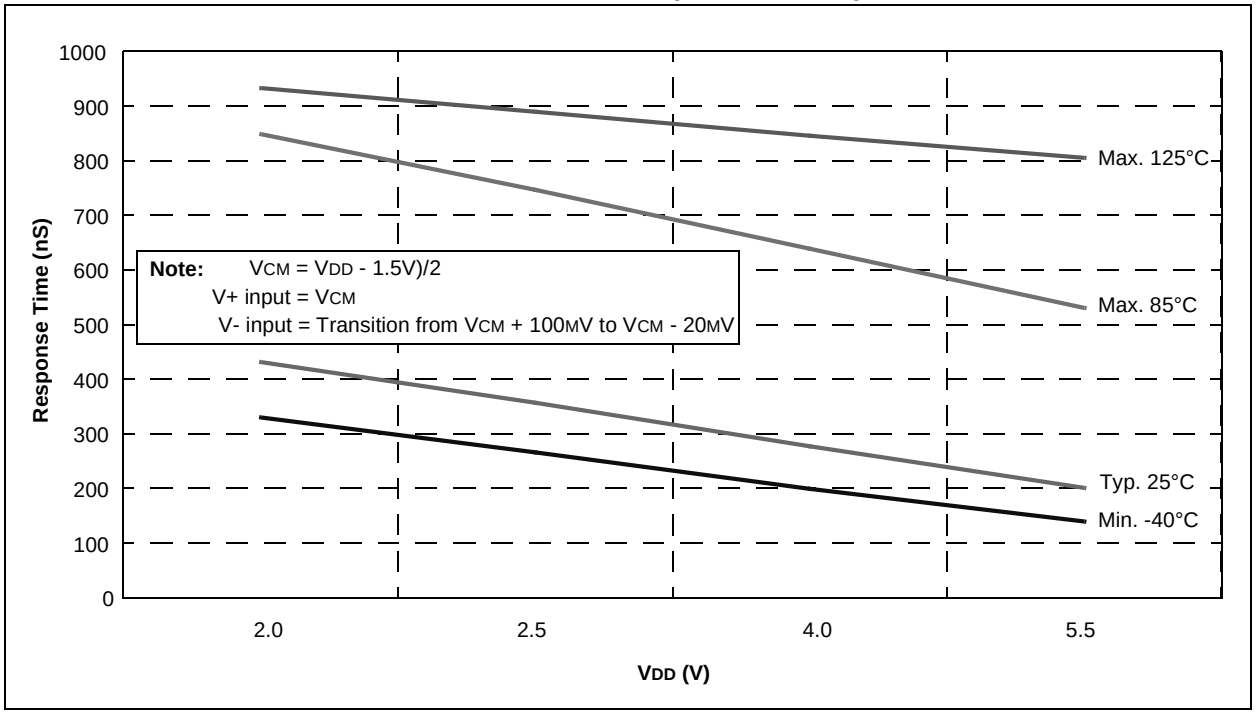
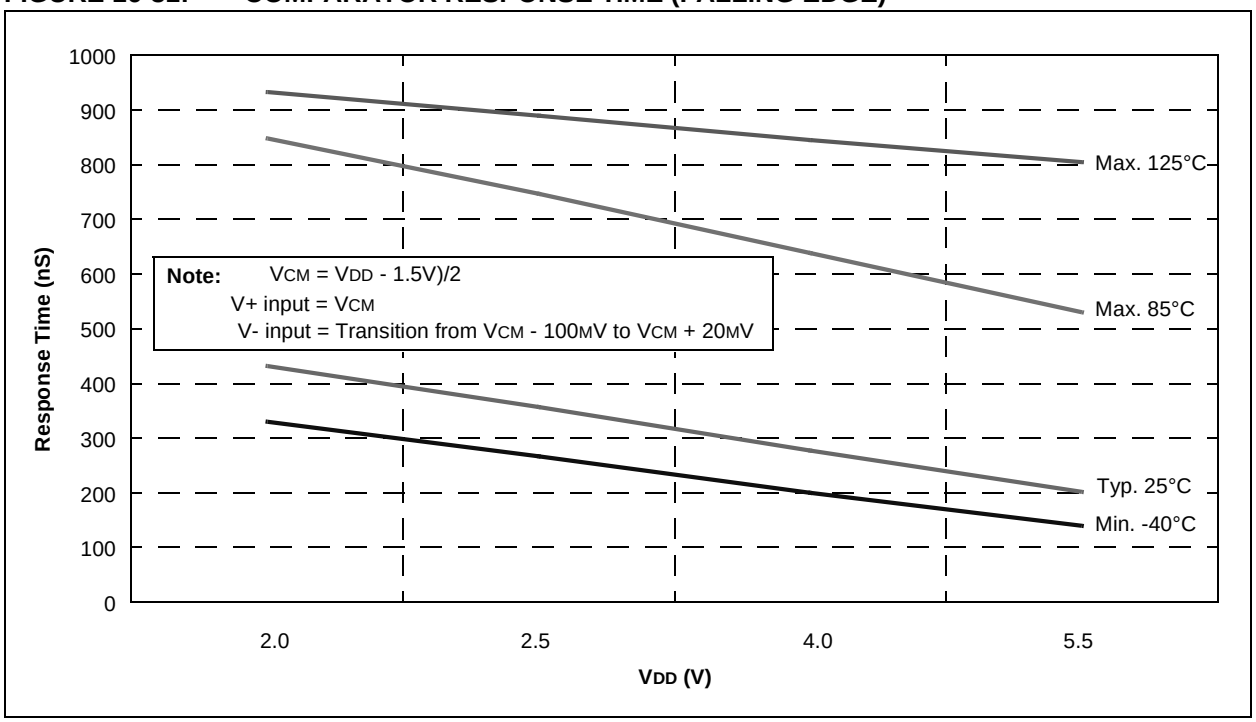
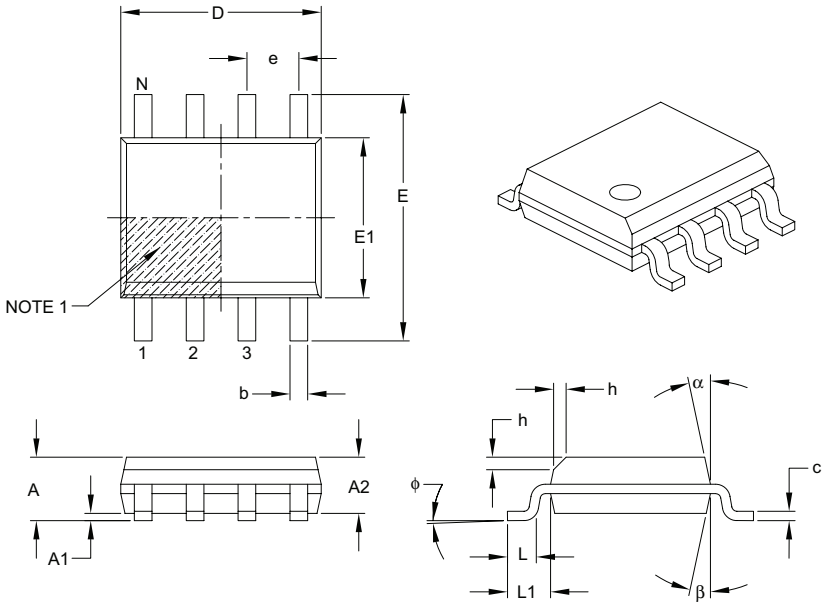


FIGURE 16-31: COMPARATOR RESPONSE TIME (FALLING EDGE)



8-Lead Plastic Small Outline (SN or OA) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B