Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f635-i-sn

NOTES:

FIGURE 2-4: PIC16F636/639 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr.(1)	00h	Indirect addr. (1)	80h	Accesses 00h-0Bh	100h	Accesses 80h-8Bh	180h
TMR0	01h	OPTION_REG	81h		101h		181h
PCL	02h	PCL	82h		102h		182h
STATUS	03h	STATUS	83h		103h		183h
FSR	04h	FSR	84h		104h		184h
PORTA	05h	TRISA	85h		105h		185h
	06h		86h		106h		186h
PORTC	07h	TRISC	87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah		10Ah		18Ah
INTCON	0Bh	INTCON	8Bh		10Bh		18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
	0Dh		8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh		10Fh		18Fh
T1CON	10h	OSCTUNE	90h	CRCON	110h		190h
	11h		91h	CRDAT0(2)	111h		191h
	12h		92h	CRDAT1(2)	112h		192h
	13h		93h	CRDAT2(2)	113h		193h
	14h	LVDCON	94h	CRDAT3(2)	114h		194h
	15h	WPUDA	95h		115h		195h
	16h	IOCA	96h		116h		196h
	17h	WDA	97h		117h		197h
WDTCON	18h		98h		118h		198h
CMCON0	19h	VRCON	99h		119h		199h
CMCON1	1Ah	EEDAT	9Ah		11Ah		19Ah
	1Bh	EEADR	9Bh		11Bh		19Bh
	1Ch	EECON1	9Ch		11Ch		19Ch
	1Dh	EECON2(1)	9Dh		11Dh		19Dh
	1Eh		9Eh		11Eh		19Eh
	1Fh		9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 32 Bytes	A0h		120h		1A0h
			BFh				
			C0h				
			EFh		16Fh		1EFh
		Accesses 70h-7Fh	F0h	Accesses 70h-7Fh	170h	Accesses Bank 0	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: CRDAT<3:0> registers are KEELOQ hardware peripheral related registers and require the execution of the "KEELOQ® Encoder License Agreement" regarding implementation of the module and access to related registers. The "KEELOQ® Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ or by contacting your local Microchip Sales Representative.

TABLE 2-1: PIC12F635 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR/ WUR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32,137
01h	TMR0	Timer0 Module Register								xxxx xxxx	61,137
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	32,137
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	26,137
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	32,137
05h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xx00	47,137
06h	—	Unimplemented								—	—
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	32,137
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(2)	0000 000x	28,137
0Ch	PIR1	EEIF	LVDIF	CRIF	—	C1IF	OSFIF	—	TMR1IF	000- 00-0	30,137
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	64,137
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	64,137
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	68,137
11h	—	Unimplemented								—	—
12h	—	Unimplemented								—	—
13h	—	Unimplemented								—	—
14h	—	Unimplemented								—	—
15h	—	Unimplemented								—	—
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	144,137
19h	CMCON0	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	79,137
1Ah	CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	82,137
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	—	Unimplemented								—	—
1Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset but will set again if the mismatch exists.

4.2.3 ULTRA LOW-POWER WAKE-UP

The Ultra Low-Power Wake-up (ULPWU) on RA0 allows a slow falling voltage to generate an interrupt-on-change on RA0 without excess current consumption. The mode is selected by setting the ULPWUE bit of the PCON register. This enables a small current sink which can be used to discharge a capacitor on RA0.

To use this feature, the RA0 pin is configured to output '1' to charge the capacitor, interrupt-on-change for RA0 is enabled and RA0 is configured as an input. The ULPWUE bit is set to begin the discharge and a SLEEP instruction is performed. When the voltage on RA0 drops below V_{IL}, an interrupt will be generated which will cause the device to wake-up. Depending on the state of the GIE bit of the INTCON register, the device will either jump to the interrupt vector (0004h) or execute the next instruction when the interrupt event occurs. See **Section 4.2.2 "Interrupt-on-Change"** and **Section 12.9.3 "PORTA Interrupt"** for more information.

This feature provides a low-power technique for periodically waking up the device from Sleep. The time-out is dependent on the discharge time of the RC circuit on RA0. See Example 4-2 for initializing the Ultra Low Power Wake-up module.

The series resistor provides overcurrent protection for the RA0 pin and can allow for software calibration of the time-out (see Figure 4-1). A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired interrupt delay. This technique will compensate for the affects of temperature, voltage and component accuracy. The Ultra Low-Power Wake-up peripheral can also be configured as a simple Programmable Low-Voltage Detect or temperature sensor.

Note:	For more information, refer to the Application Note *AN879,* "*Using the Microchip Ultra Low-Power Wake-up Module*" (DS00879).

EXAMPLE 4-2: ULTRA LOW-POWER WAKE-UP INITIALIZATION

```
BANKSEL PORTA        ;
BSF     PORTA,0      ;Set RA0 data latch
MOVLW   H'7'         ;Turn off
MOVWF   CMCON0       ; comparators
BANKSEL TRISA        ;
BCF     TRISA,0      ;Output high to
CALL    CapDelay     ; charge capacitor
BSF     PCON,ULPWUE  ;Enable ULP Wake-up
BSF     IOCA,0       ;Select RA0 IOC
BSF     TRISA,0      ;RA0 to input
MOVLW   B'10001000'  ;Enable interrupt
MOVWF   INTCON       ; and clear flag
SLEEP                ;Wait for IOC
NOP                  ;
```

6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 3-bit prescaler
- Optional LP oscillator
- Synchronous or asynchronous operation
- Timer1 gate (count enable) via comparator or $\overline{T1G}$ pin
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Comparator output synchronization to Timer1 clock

Figure 6-1 is a block diagram of the Timer1 module.

6.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer. When used with an external clock source, the module can be used as either a timer or counter.

6.2 Clock Source Selection

The TMR1CS bit of the T1CON register is used to select the clock source. When TMR1CS = 0, the clock source is FOSC/4. When TMR1CS = 1, the clock source is supplied externally.

Clock Source	T1OSCEN	FOSC Mode	T1CS
FOSC/4	x	xxx	x
T1CKI pin	x		1
T1LPOSC	1	LP or INTOSCIO	

6.10 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 6-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 6-1: T1CON: TIMER 1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV(1)	TMR1GE(2)	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **T1GINV:** Timer1 Gate Invert bit(1)
1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 6 **TMR1GE:** Timer1 Gate Enable bit(2)
If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 is on if Timer1 gate is active
0 = Timer1 is on

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
If INTOSC without CLKOUT oscillator is active:
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
Else:
This bit is ignored. LP oscillator is disabled.

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from T1CKI pin (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Note 1: T1GINV bit inverts the Timer1 gate logic, regardless of source.
2: TMR1GE bit must be set to use either $\overline{\text{T1G}}$ pin or C2OUT, as selected by the T1GSS bit of the CMCON1 register, as a Timer1 gate source.

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	00-- --10
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIE1	EEIE	LVDIE	CRIE	C2IE(1)	C1IE	OSFIE	—	TMR1IE	000- 00-0	000- 00-0
PIR1	EEIF	LVDIF	CRIF	C2IF(1)	C1IF	OSFIF	—	TMR1IF	000- 00-0	000- 00-0
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.
Note 1: PIC16F636/639 only.

REGISTER 7-2: CMCON0: COMPARATOR CONFIGURATION REGISTER (PIC16F636/639)

R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **C2OUT:** Comparator 2 Output bit

When C2INV = 0:
1 = C2 V_{IN}+ > C2 V_{IN}-
0 = C2 V_{IN}+ < C2 V_{IN}-

When C2INV = 1:
1 = C2 V_{IN}+ < C2 V_{IN}-
0 = C2 V_{IN}+ > C2 V_{IN}-

bit 6 **C1OUT:** Comparator 1 Output bit

When C1INV = 0:
1 = C1 V_{IN}+ > C1 V_{IN}-
0 = C1 V_{IN}+ < C1 V_{IN}-

When C1INV = 1:
1 = C1 V_{IN}+ < C1 V_{IN}-
0 = C1 V_{IN}+ > C1 V_{IN}-

bit 5 **C2INV:** Comparator 2 Output Inversion bit

1 = C2 output inverted
0 = C2 output not inverted

bit 4 **C1INV:** Comparator 1 Output Inversion bit

1 = C1 Output inverted
0 = C1 Output not inverted

bit 3 **CIS:** Comparator Input Switch bit

When CM<2:0> = 010:

1 = C1IN+ connects to C1 V_{IN}-
C2IN+ connects to C2 V_{IN}-
0 = C1IN- connects to C1 V_{IN}-
C2IN- connects to C2 V_{IN}-

When CM<2:0> = 001:
1 = C1IN+ connects to C1 V_{IN}-
0 = C1IN- connects to C1 V_{IN}-

bit 2-0 **CM<2:0>:** Comparator Mode bits (See Figure 7-5)

000 = Comparators off. CxIN pins are configured as analog
001 = Three inputs multiplexed to two comparators
010 = Four inputs multiplexed to two comparators
011 = Two common reference comparators
100 = Two independent comparators
101 = One independent comparator
110 = Two comparators with outputs and common reference
111 = Comparators off. CxIN pins are configured as digital I/O

7.11 Comparator Voltage Reference

The Comparator Voltage Reference module provides an internally generated voltage reference for the comparators. The following features are available:

- Independent from Comparator operation
- Two 16-level voltage ranges
- Output clamped to VSS
- Ratiometric with VDD
- Fixed Voltage Reference

The VRCON register (Register 7-5) controls the Voltage Reference module shown in Figure 7-10.

7.11.1 INDEPENDENT OPERATION

The comparator voltage reference is independent of the comparator configuration. Setting the VREN bit of the VRCON register will enable the voltage reference.

7.11.2 OUTPUT VOLTAGE SELECTION

The CVREF voltage reference has 2 ranges with 16 voltage levels in each range. Range selection is controlled by the VRR bit of the VRCON register. The 16 levels are set with the VR<3:0> bits of the VRCON register.

The CVREF output voltage is determined by the following equations:

EQUATION 7-1: CVREF OUTPUT VOLTAGE (INTERNAL CVREF)

$$VRR = 1 \text{ (low range):}$$
$$CVREF = (VR<3:0>/24) \times VDD$$
$$VRR = 0 \text{ (high range):}$$
$$CVREF = (VDD/4) + (VR<3:0> \times VDD/32)$$

EQUATION 7-2: CVREF OUTPUT VOLTAGE (EXTERNAL CVREF)

$$VRR = 1 \text{ (low range):}$$
$$CVREF = (VR<3:0>/24) \times VLADDER$$
$$VRR = 0 \text{ (high range):}$$
$$CVREF = (VLADDER/4) + (VR<3:0> \times VLADDER/32)$$
$$VLADDER = VDD \text{ or } ([VREF+] - [VREF-]) \text{ or } VREF+$$

The full range of VSS to VDD cannot be realized due to the construction of the module. See Figure 7-10.

7.11.3 OUTPUT CLAMPED TO VSS

The CVREF output voltage can be set to Vss with no power consumption by configuring VRCON as follows:

- VREN = 0
- VRR = 1
- VR<3:0> = 0000

This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.

7.11.4 OUTPUT RATIOMETRIC TO VDD

The comparator voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 15.0 "Electrical Specifications"**.

9.2 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD of the EECON1 register, as shown in Example 9-1. The data is available, in the very next cycle, in the EEDAT register. Therefore, it can be read in the next instruction. EEDAT holds this value until another read, or until it is written to by the user (during a write operation).

EXAMPLE 9-1: DATA EEPROM READ

```
BANKSEL  EEADR          ;
MOVLW    CONFIG_ADDR    ;
MOVWF    EEADR          ;Address to read
BSF      EECON1,RD      ;EE Read
MOVF     EEDAT,W        ;Move data to W
```

9.3 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDAT register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 9-2.

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit of the PIR1 register must be cleared by software.

EXAMPLE 9-2: DATA EEPROM WRITE

```
          BANKSEL EEADR          ;
          BSF     EECON1,WREN    ;Enable write
          BCF     INTCON,GIE     ;Disable INTs
Required  MOVLW   55h            ;Unlock write
Sequence  MOVWF   EECON2         ;
          MOVLW   AAh            ;
          MOVWF   EECON2         ;
          BSF     EECON1,WR      ;Start the write
          BSF     INTCON,GIE     ;Enable INTS
```

9.4 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM should be verified (see Example 9-3) to the desired value to be written.

EXAMPLE 9-3: WRITE VERIFY

```
BANKSEL  EEDAT      ;
MOVF     EEDAT,W    ;EEDAT not changed
                    ;from previous write
BSF      EECON1,RD  ;YES, Read the
                    ;value written
XORWF    EEDAT,W    ;
BTFSS    STATUS,Z   ;Is data the same
GOTO     WRITE_ERR  ;No, handle error
:                   ;Yes, continue
```

9.4.1 USING THE DATA EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). When variables in one section change frequently, while variables in another section do not change, it is possible to exceed the total number of write cycles to the EEPROM (specification D124) without exceeding the total number of write cycles to a single byte (specifications D120 and D120A). If this is the case, then a refresh of the array must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

FIGURE 11-1: FUNCTIONAL BLOCK DIAGRAM – ANALOG FRONT-END

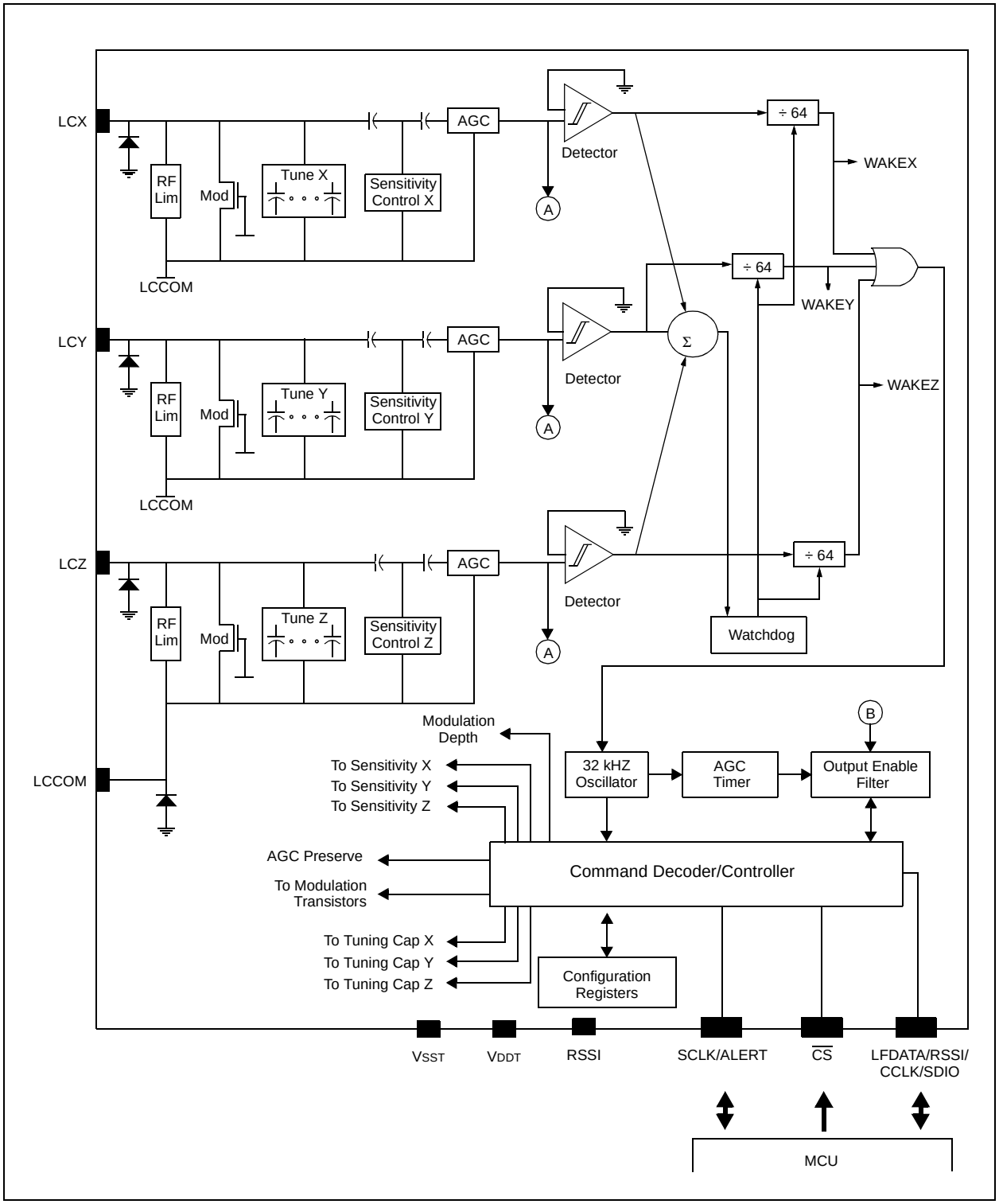
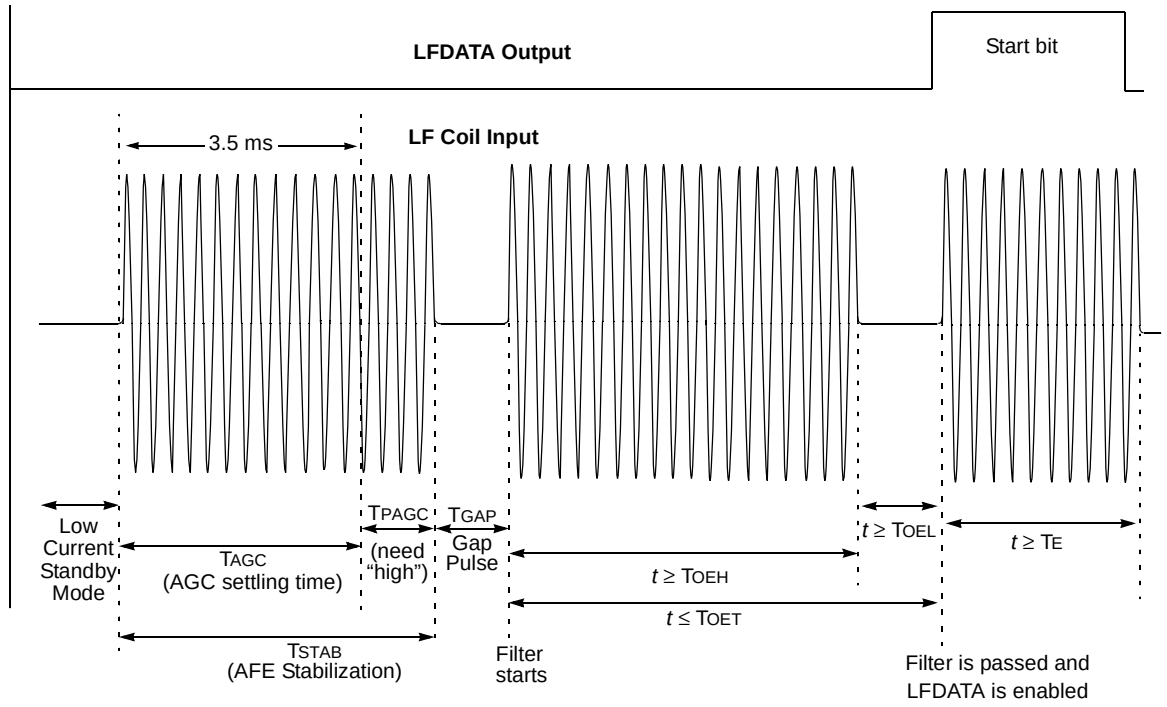


FIGURE 11-6: OUTPUT ENABLE FILTER TIMING EXAMPLE (DETAILED)



Legend:
- TAGC = AGC stabilization time
- TE = Time element of pulse
- TGAP = AGC stabilization gap
- TOEH = Minimum output enable filter high time
- TOEL = Minimum output enable filter low time
- TOET = Maximum output enable filter period
- TPAGC = High time after TAGC
- TSTAB = TAGC + TPAGC

FIGURE 11-11: INPUT SIGNAL AND DEMODULATOR OUTPUT (WHEN OUTPUT ENABLE FILTER IS ENABLED AND INPUT MEETS FILTER TIMING REQUIREMENTS)

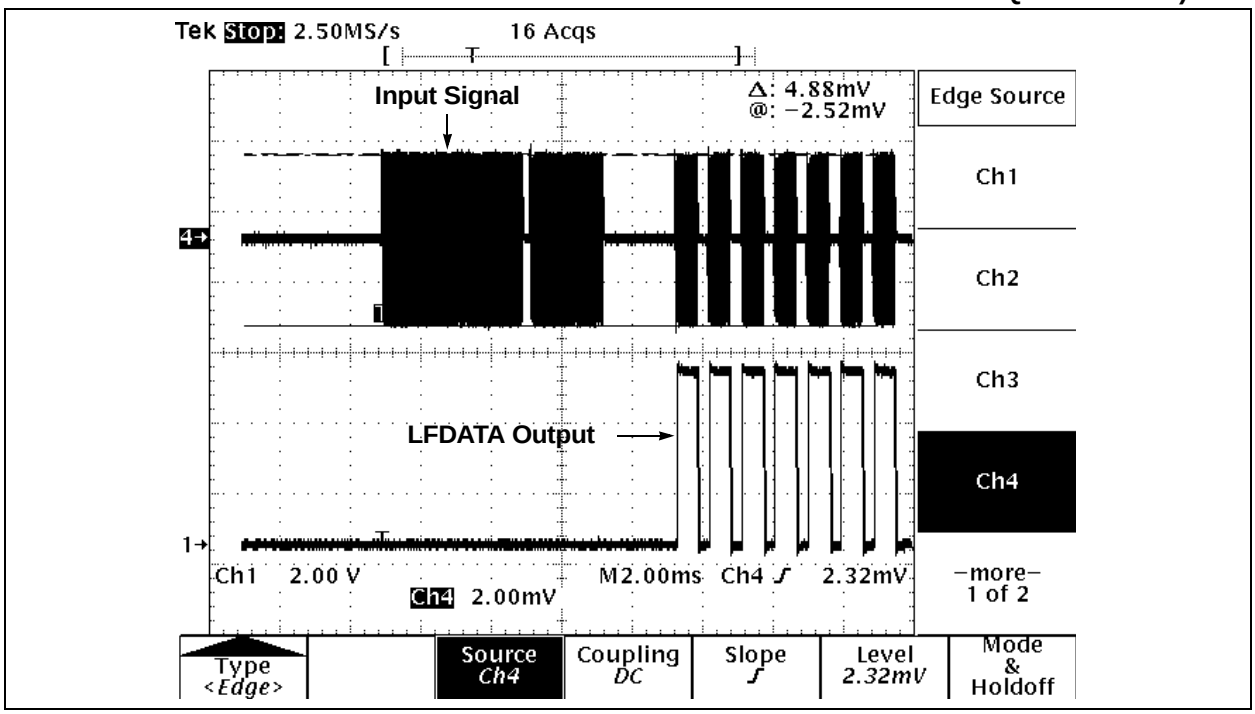
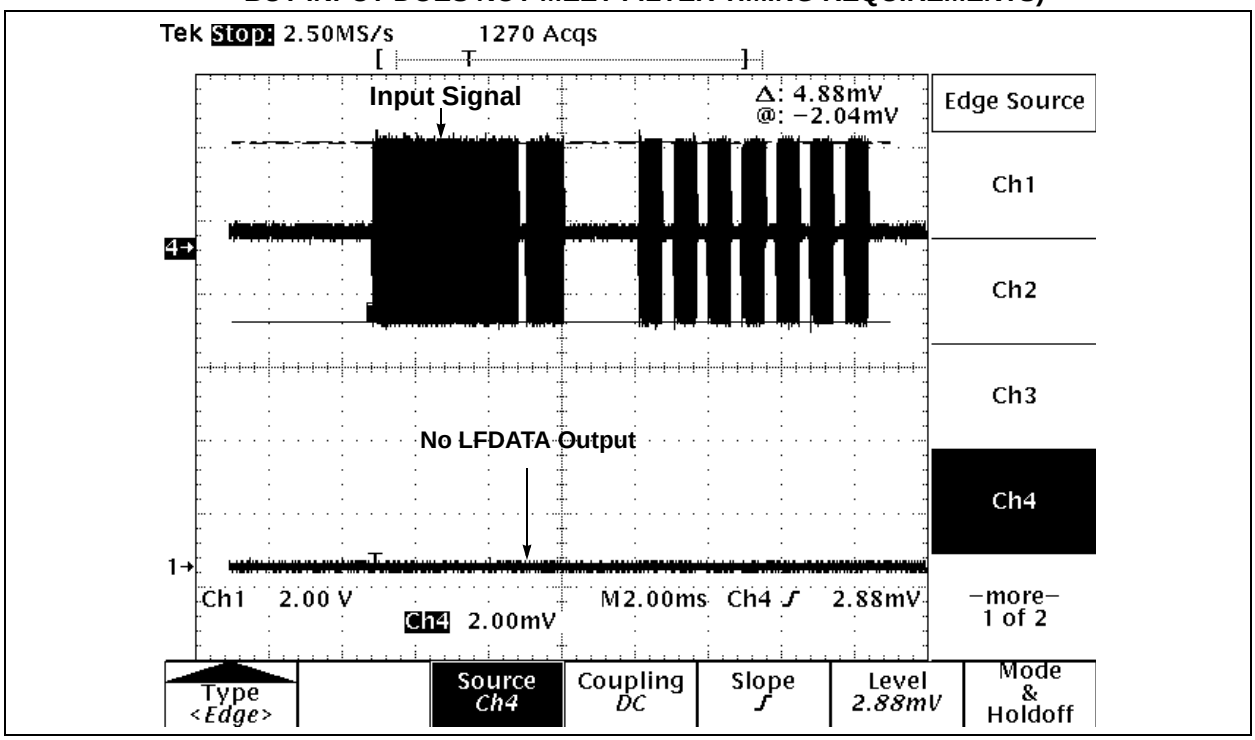


FIGURE 11-12: NO DEMODULATOR OUTPUT (WHEN OUTPUT ENABLE FILTER IS ENABLED BUT INPUT DOES NOT MEET FILTER TIMING REQUIREMENTS)



15.7 DC Characteristics: PIC16F639-I (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial Supply Voltage 2.0V ≤ VDD ≤ 3.6V				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VOH	**Output High Voltage**					
D090		I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 3.6V (Ind.)
D092		OSC2/CLKOUT (RC mode)	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 3.6V (Ind.) IOH = -1.0 mA, VDD = 3.6V (Ext.)
		Digital Output High Voltage					Analog Front-End (AFE) section
D093		LFDATA/SDIO for Analog Front-End (AFE)	VDD – 0.5	—	—	V	IOH = -400 µA, VDD = 2.0V
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	—	50*	pF	
D102	IULP	**Ultra Low-power Wake-up Current**	—	200	—	nA	
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh(1)	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 9.4.1 "Using the Data EEPROM"** for additional information

FIGURE 16-16: BOR IPD vs. VDD OVER TEMPERATURE

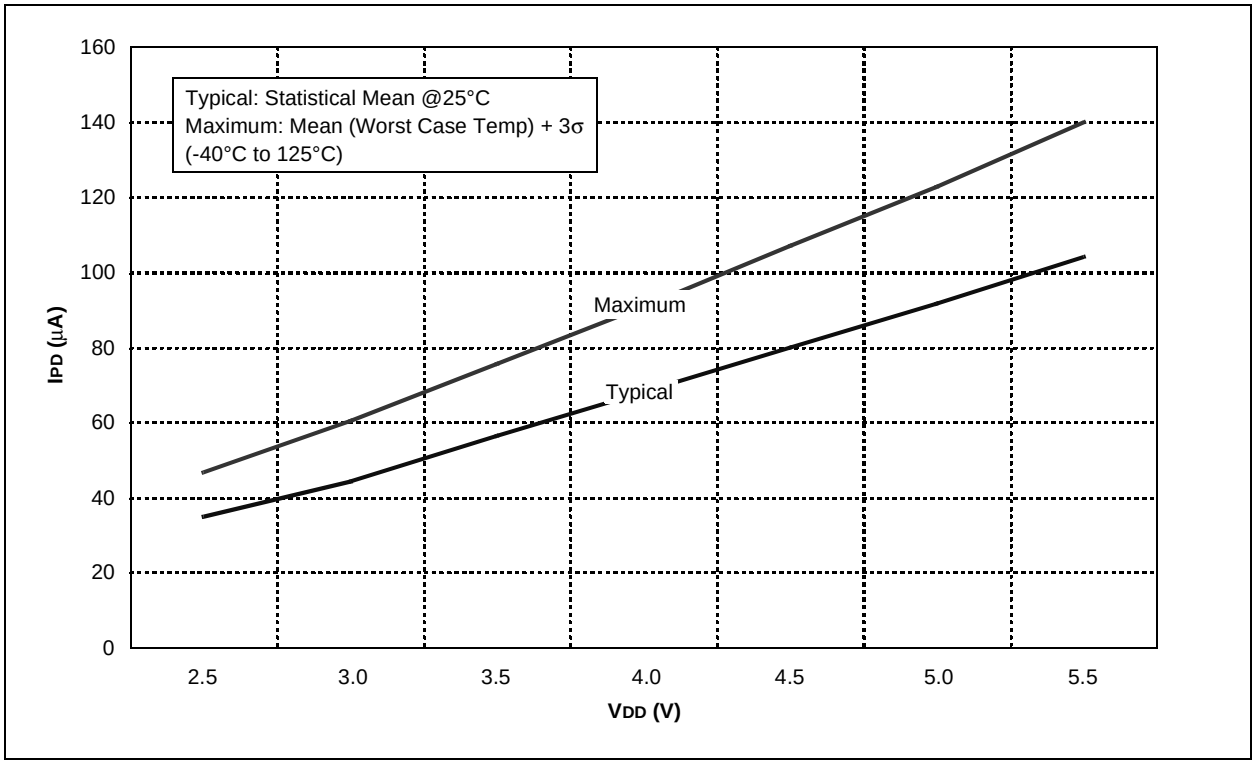


FIGURE 16-17: TYPICAL WDT IPD vs. VDD OVER TEMPERATURE

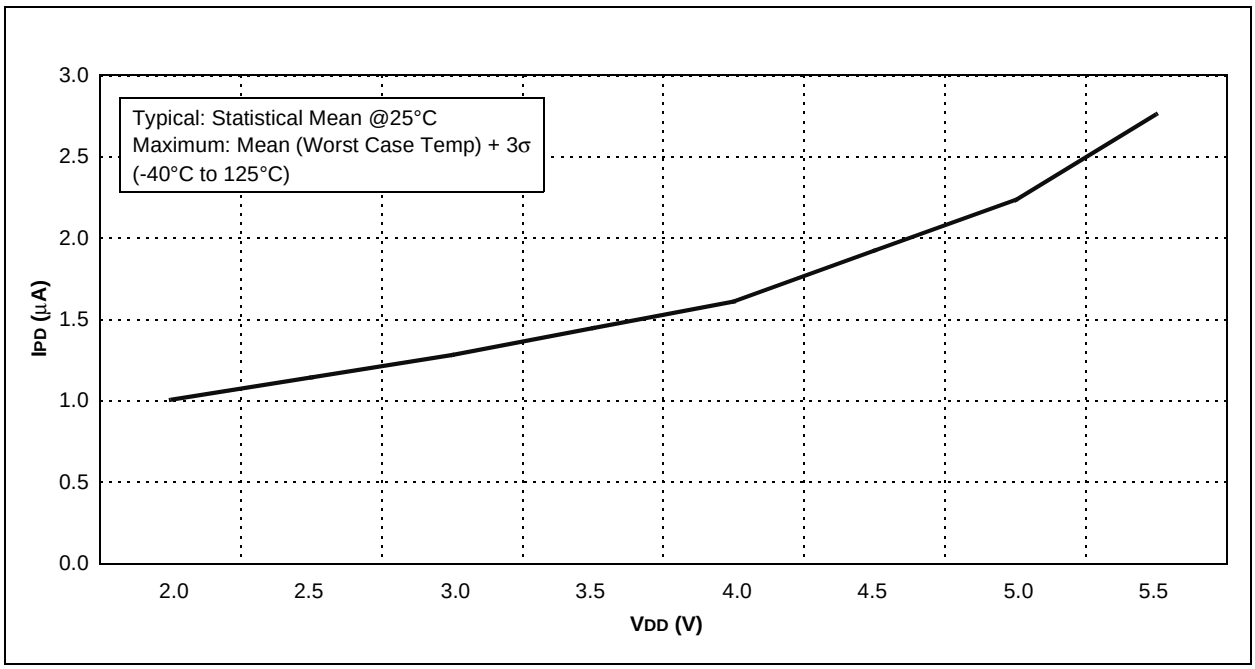


FIGURE 16-26: VOH vs. IOH OVER TEMPERATURE (VDD = 5.0V)

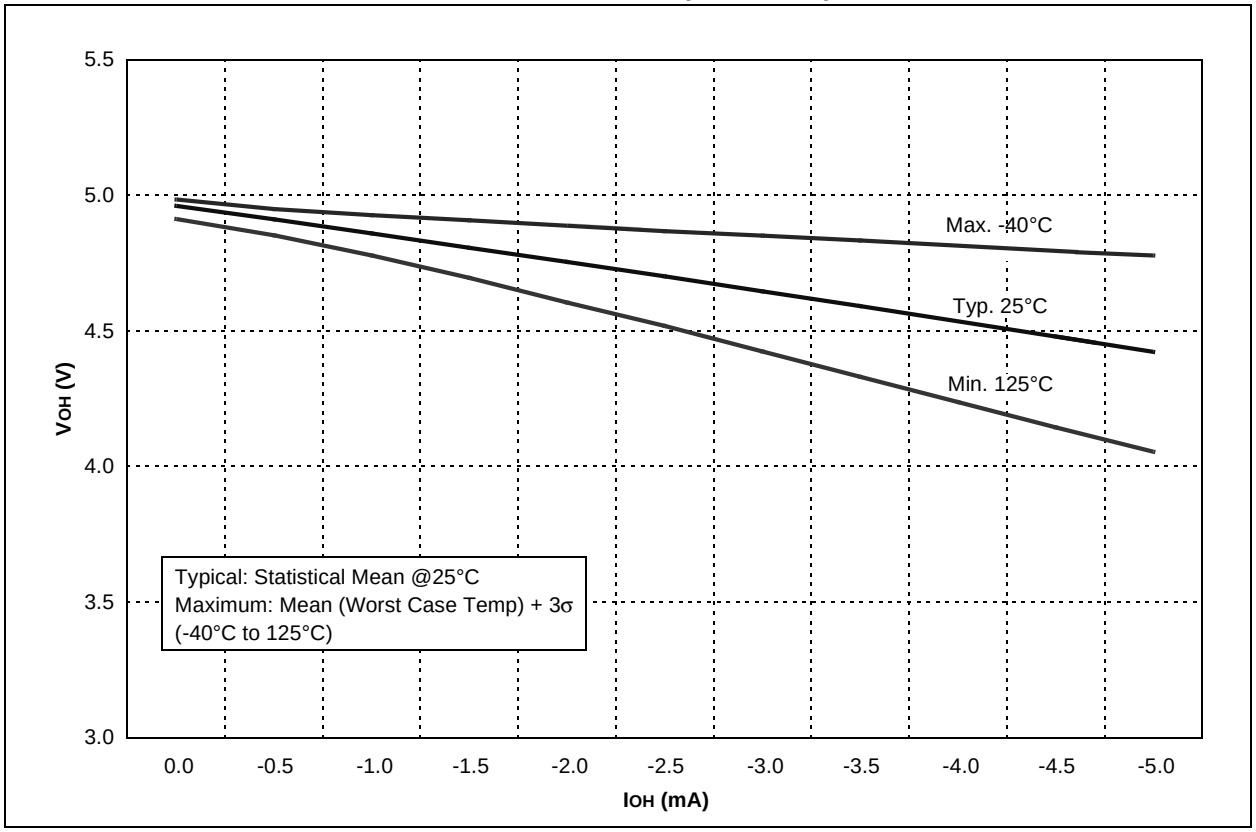


FIGURE 16-27: TTL INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

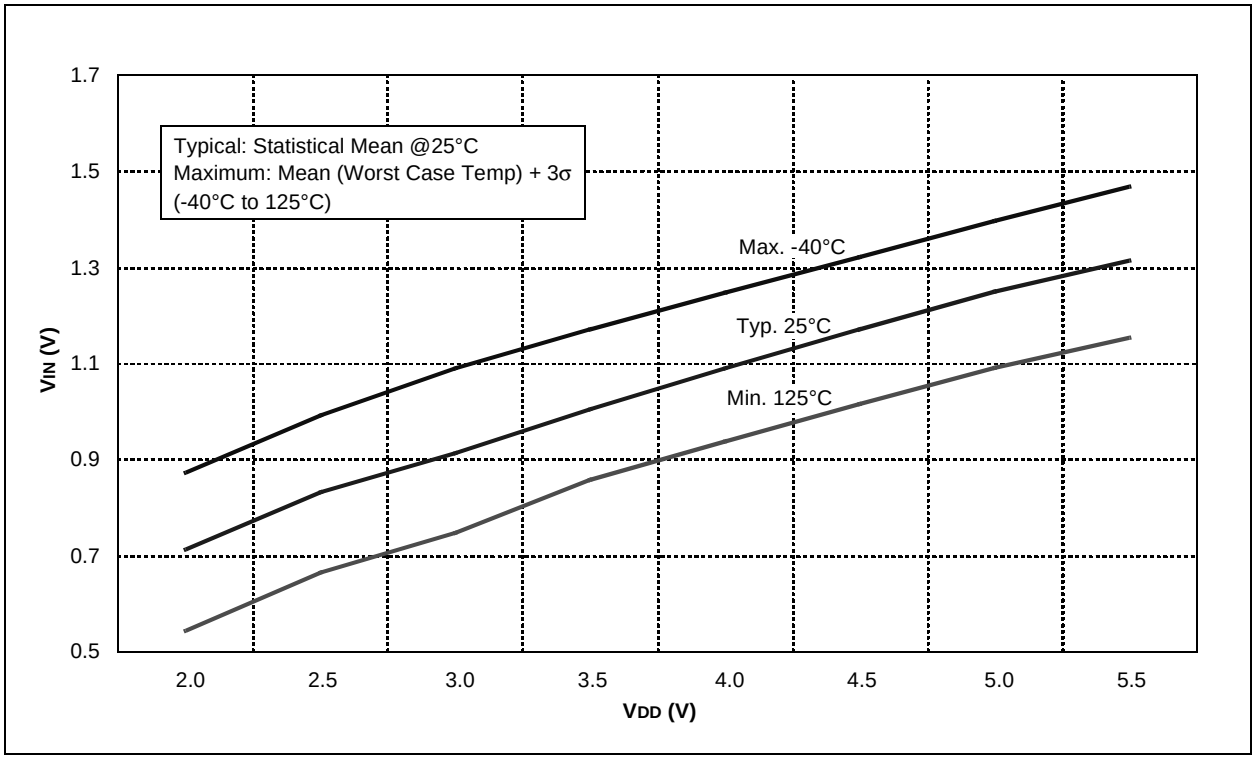


FIGURE 16-36: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (25°C)

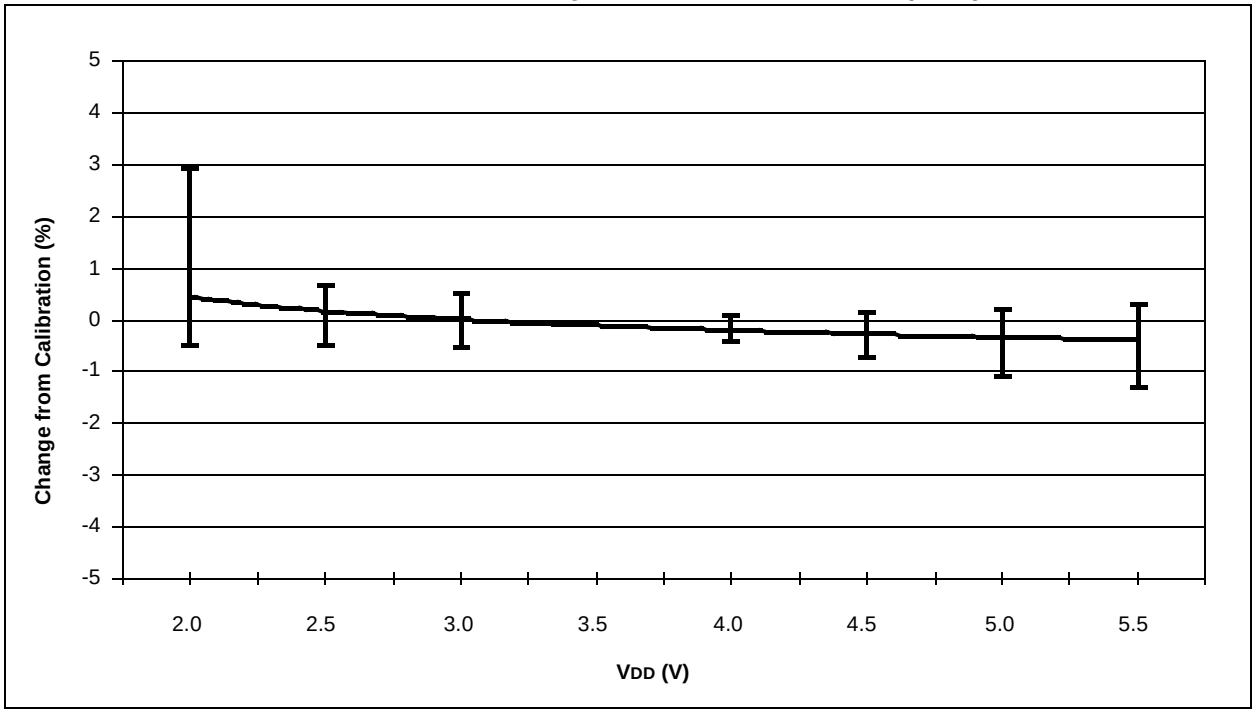
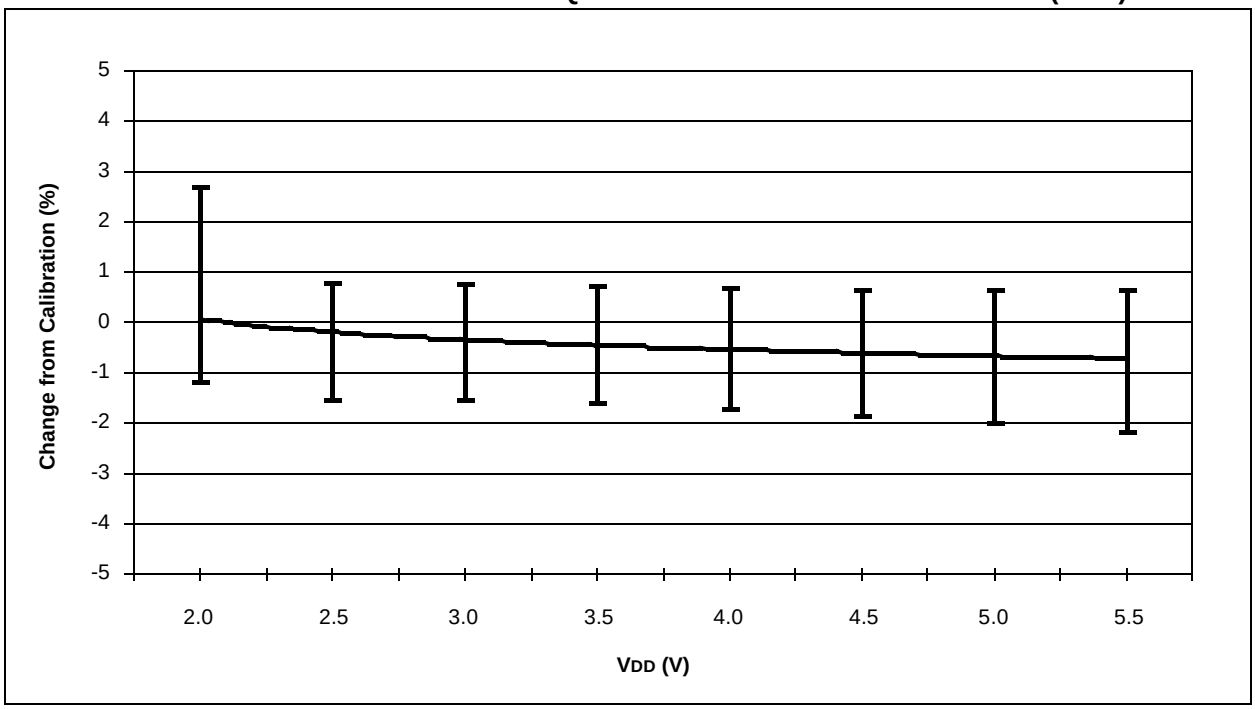


FIGURE 16-37: TYPICAL HFINTOSC FREQUENCY CHANGE OVER DEVICE VDD (85°C)

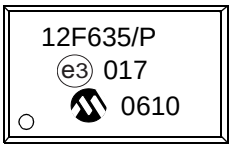


17.0 PACKAGING INFORMATION

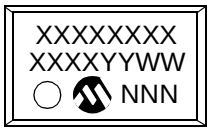
17.1 Package Marking Information

8-Lead PDIP

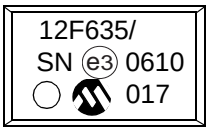
Example



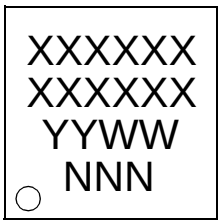
8-Lead SOIC



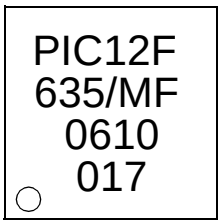
Example



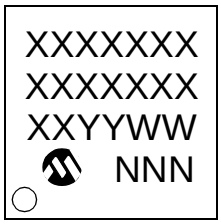
8-Lead DFN (4x4x0.9 mm)



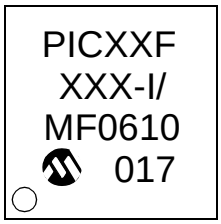
Example



8-Lead DFN-S (6x5 mm)



Example



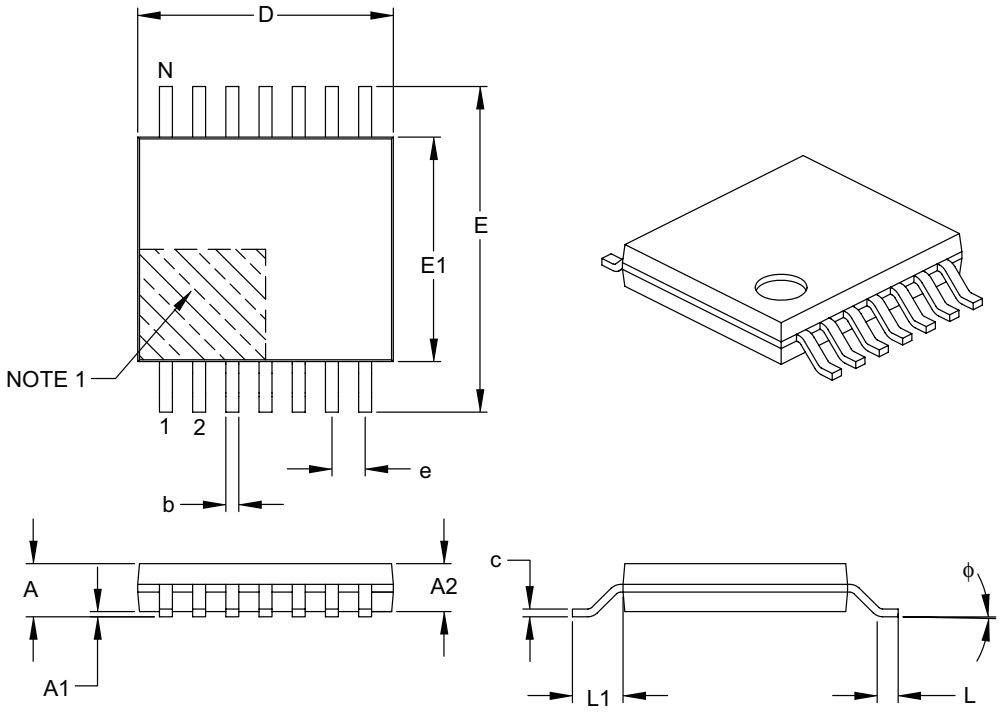
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard PIC device marking consists of Microchip part number, year code, week code and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B