Welcome to <u>E-XFL.COM</u>

What is "**<u>Embedded - Microcontrollers</u>**"?

"<u>Embedded - Microcontrollers</u>" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**<u>Embedded - Microcontrollers</u>**"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f635t-i-md

TABLE 1-2:   PIC16F636 PINOUT DESCRIPTIONS

Name	Function	Input Type	Output Type	Description
RA0/C1IN+/ICSPDAT/ULPWU	RA0	TTL	—	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down. Selectable Ultra Low-Power Wake-up pin.
	C1IN+	AN	—	Comparator 1 input – positive.
	ICSPDAT	TTL	CMOS	Serial programming data I/O.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
RA1/C1IN-/VREF/ICSPCLK	RA1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	C1IN-	AN	—	Comparator 1 input – negative.
	VREF	AN	—	External voltage reference
	ICSPCLK	ST	—	Serial programming clock.
RA2/T0CKI/INT/C1OUT	RA2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T0CKI	ST	—	External clock for Timer0.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator 1 output.
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear Reset. Pull-up enabled when configured as $\overline{\text{MCLR}}$.
	VPP	HV	—	Programming voltage.
RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT	RA4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate.
	OSC2	—	XTAL	XTAL connection.
	CLKOUT	—	CMOS	T$_{OSC}$/4 reference clock.
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T1CKI	ST	—	Timer1 clock.
	OSC1	XTAL	—	XTAL connection.
	CLKIN	ST	—	T$_{OSC}$ reference clock.
RC0/C2IN+	RC0	TTL	CMOS	General purpose I/O.
	C2IN+	AN	—	Comparator 1 input – positive.
RC1/C2IN-	RC1	TTL	CMOS	General purpose I/O.
	C2IN-	AN	—	Comparator 1 input – negative.
RC2	RC2	TTL	CMOS	General purpose I/O.
RC3	RC3	TTL	CMOS	General purpose I/O.
RC4/C2OUT	RC4	TTL	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator 2 output.
RC5	RC5	TTL	CMOS	General purpose I/O.
VDD	VDD	D	—	Power supply for microcontroller.
VSS	VSS	D	—	Ground reference for microcontroller.

Legend: AN = Analog input or output   CMOS = CMOS compatible input or output   D = Direct
HV = High Voltage   ST = Schmitt Trigger input with CMOS levels
TTL = TTL compatible input   XTAL = Crystal

REGISTER 4-3: **WDA: WEAK PULL-UP/PULL-DOWN DIRECTION REGISTER**

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6   **Unimplemented**: Read as '0'

bit 5-4   **WDA<5:4>**: Pull-up/Pull-down Selection bits
1 = Pull-up selected
0 = Pull-down selected

bit 3   **Unimplemented**: Read as '0'

bit 2-0   **WDA<2:0>**: Pull-up/Pull-down Selection bits
1 = Pull-up selected
0 = Pull-down selected

Note 1:   The weak pull-up/pull-down device is enabled only when the global $\overline{\text{RAPU}}$ bit is enabled, the pin is in Input mode (TRIS = 1), the individual WDA bit is enabled (WDA = 1) and the pin is not configured as an analog input or clock function.

2:   RA3 pull-up is enabled when the pin is configured as $\overline{\text{MCLR}}$ in the Configuration Word register and the device is not in Programming mode.

REGISTER 4-4: **WPUDA: WEAK PULL-UP/PULL-DOWN ENABLE REGISTER**

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPUDA5[3]	WPUDA4[3]	—	WPUDA2	WPUDA1	WPUDA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6   **Unimplemented**: Read as '0'

bit 5-4   **WPUDA<5:4>**: Pull-up/Pull-down Direction Selection bits[3]
1 = Pull-up/pull-down enabled
0 = Pull-up/pull-down disabled

bit 3   **Unimplemented**: Read as '0'

bit 2-0   **WPUDA<2:0>**: Pull-up/Pull-down Direction Selection bits
1 = Pull-up/pull-down enabled
0 = Pull-up/pull-down disabled

Note 1:   The weak pull-up/pull-down direction device is enabled only when the global $\overline{\text{RAPU}}$ bit is enabled, the pin is in Input mode (TRIS = 1), the individual WPUDA bit is enabled (WPUDA = 1) and the pin is not configured as an analog input or clock function.

2:   RA3 pull-up is enabled when the pin is configured as $\overline{\text{MCLR}}$ in the Configuration Word register and the device is not in Programming mode.

3:   WPUDA5 bit can be written if INTOSC is enabled and T1OSC is disabled; otherwise, the bit can not be written and reads as '1'. WPUDA4 bit can be written if not configured as OSC2; otherwise, the bit can not be written and reads as '1'

5.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (shared with Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow

Figure 5-1 is a block diagram of the Timer0 module.

5.1 Timer0 Operation

When used as a timer, the Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

5.1.1 8-BIT TIMER MODE

When used as a timer, the Timer0 module will increment every instruction cycle (without prescaler). Timer mode is selected by clearing the T0CS bit of the OPTION register to '0'.
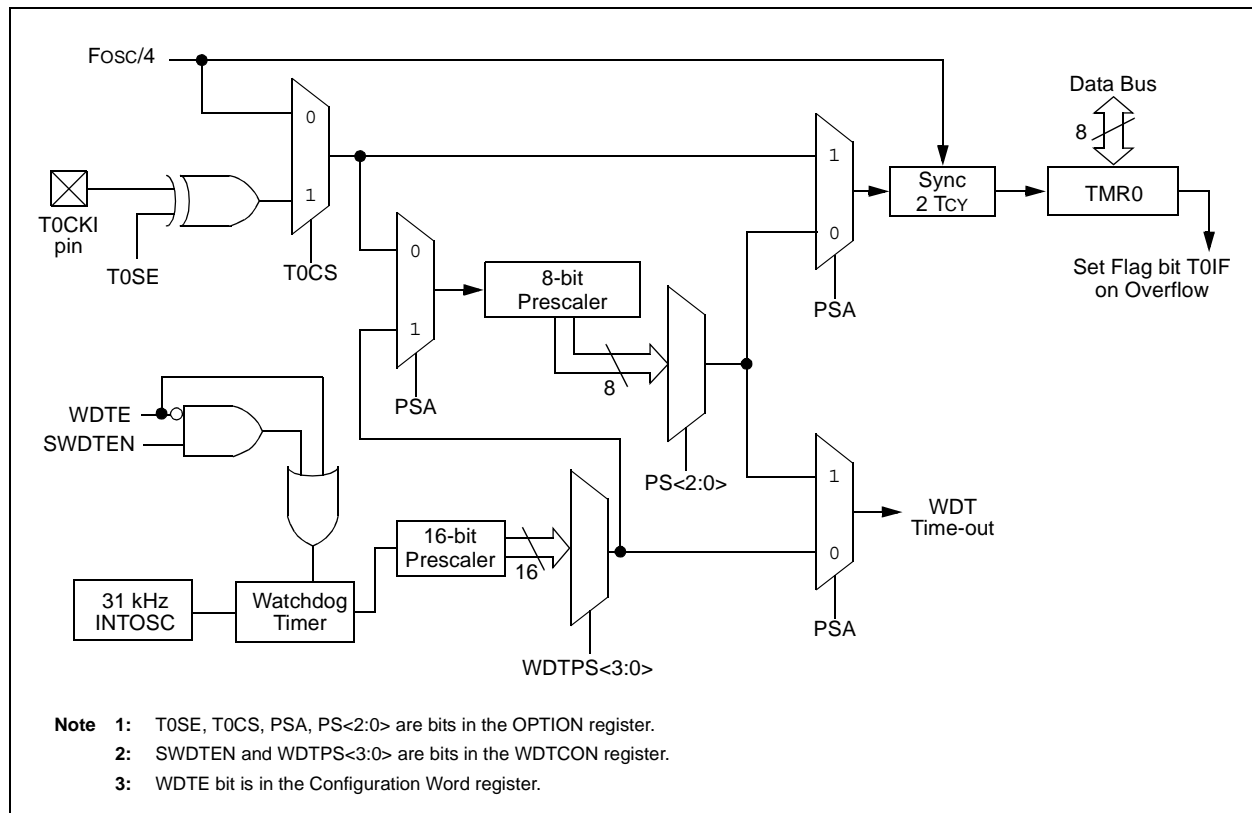
When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note:	The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

5.1.2 8-BIT COUNTER MODE

When used as a counter, the Timer0 module will increment on every rising or falling edge of the T0CKI pin. The incrementing edge is determined by the T0SE bit of the OPTION register. Counter mode is selected by setting the T0CS bit of the OPTION register to '1'.

FIGURE 5-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.
2: SWDTEN and WDTPS<3:0> are bits in the WDTCON register.
3: WDTE bit is in the Configuration Word register.

REGISTER 7-3:   CMCON1: COMPARATOR CONFIGURATION REGISTER (PIC12F635)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
—	—	—	—	—	—	T1GSS	CMSYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-2   **Unimplemented:** Read as '0'

bit 1   **T1GSS:** Timer1 Gate Source Select bit[1]

    1 = Timer1 Gate Source is $\overline{\text{T1G}}$ pin (pin should be configured as digital input)
    0 = Timer1 Gate Source is comparator output

bit 0   **CMSYNC:** Comparator Output Synchronization bit[2]

    1 = Output is synchronized with falling edge of Timer1 clock
    0 = Output is asynchronous

Note 1:   Refer to **Section 6.6 "Timer1 Gate"**.
    2:   Refer to Figure 7-2.

REGISTER 7-4:   CMCON1: COMPARATOR CONFIGURATION REGISTER (PIC16F636/639)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
—	—	—	—	—	—	T1GSS	C2SYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-2   **Unimplemented:** Read as '0'

bit 1   **T1GSS:** Timer1 Gate Source Select bit[1]

    1 = Timer1 gate source is $\overline{\text{T1G}}$ pin (pin should be configured as digital input)
    0 = Timer1 gate source is Comparator C2 output

bit 0   **C2SYNC:** Comparator C2 Output Synchronization bit[2]

    1 = Output is synchronized with falling edge of Timer1 clock
    0 = Output is asynchronous

Note 1:   Refer to **Section 6.6 "Timer1 Gate"**.
    2:   Refer to Figure 7-4.

9.2 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD of the EECON1 register, as shown in Example 9-1. The data is available, in the very next cycle, in the EEDAT register. Therefore, it can be read in the next instruction. EEDAT holds this value until another read, or until it is written to by the user (during a write operation).

EXAMPLE 9-1: DATA EEPROM READ

```
BANKSEL    EEADR          ;
MOVLW      CONFIG_ADDR    ;
MOVWF      EEADR          ;Address to read
BSF        EECON1,RD      ;EE Read
MOVF       EEDAT,W        ;Move data to W
```

9.3 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDAT register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 9-2.

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit of the PIR1 register must be cleared by software.

EXAMPLE 9-2: DATA EEPROM WRITE

```
          BANKSEL EEADR          ;
          BSF        EECON1,WREN  ;Enable write
          BCF        INTCON,GIE   ;Disable INTs
          MOVLW      55h          ;Unlock write
Required  MOVWF      EECON2       ;
Sequence  MOVLW      AAh          ;
          MOVWF      EECON2       ;
          BSF        EECON1,WR    ;Start the write
          BSF        INTCON,GIE   ;Enable INTS
```

9.4 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM should be verified (see Example 9-3) to the desired value to be written.

EXAMPLE 9-3: WRITE VERIFY

```
BANKSEL    EEDAT      ;
MOVF       EEDAT,W    ;EEDAT not changed
                      ;from previous write
BSF        EECON1,RD  ;YES, Read the
                      ;value written
XORWF      EEDAT,W    ;
BTFSS      STATUS,Z   ;Is data the same
GOTO       WRITE_ERR  ;No, handle error
:                     ;Yes, continue
```

9.4.1 USING THE DATA EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). When variables in one section change frequently, while variables in another section do not change, it is possible to exceed the total number of write cycles to the EEPROM (specification D124) without exceeding the total number of write cycles to a single byte (specifications D120 and D120A). If this is the case, then a refresh of the array must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

NOTES:

11.6 AGC Control

The AGC controls the variable attenuator to limit the internal signal voltage to avoid saturation of internal amplifiers and demodulators (Refer to **Section 11.4 "Variable Attenuator"**).

The signal levels from all 3 channels are combined such that AGC attenuates all 3 channels uniformly in respect to the channel with the strongest signal.

Note:	The AGC control function is accomplished by the device itself. The user cannot control its function.

11.7 Fixed Gain Amplifiers 1 and 2

FGA1 and FGA2 provides a maximum two-stage gain of 40 dB.

Note:	The user cannot control the gain of these two amplifiers.

11.8 Auto Channel Selection

The Auto Channel Selection feature is enabled if the Auto Channel Select bit AUTOCHSEL<8> in Configuration Register 5 (Register 11-6) is set, and disabled if the bit is cleared. When this feature is active (i.e., AUTOCHSE <8> = 1), the control circuit checks the demodulator output of each input channel immediately after the AGC settling time (T_{STAB}). If the output is high, it allows this channel to pass data, otherwise it is blocked.

The status of this operation is monitored by AFE Status Register 7 bits <8:6> (Register 11-8). These bits indicate the current status of the channel selection activity, and automatically updates for every Soft Reset period. The auto channel selection function resets after each Soft Reset (or after Inactivity timer time-out). Therefore, the blocked channels are reenabled after Soft Reset.

This feature can make the output signal cleaner by blocking any channel that was not high at the end of T_{AGC}. This function works only for demodulated data output, and is not applied for carrier clock or RSSI output.

11.9 Carrier Clock Detector

The Detector senses the input carrier cycles. The output of the Detector switches digitally at the signal carrier frequency. Carrier clock output is available when the output is selected by the DATOUT bit in the AFE Configuration Register 1 (Register 11-2).

11.10 Demodulator

The Demodulator consists of a full-wave rectifier, low pass filter, peak detector and Data Slicer that detects the envelope of the input signal.

11.11 Data Slicer

The Data Slicer consists of a reference generator and comparator. The Data Slicer compares the input with the reference voltage. The reference voltage comes from the minimum modulation depth requirement setting and input peak voltage. The data from all 3 channels are OR'd together and sent to the output enable filter.

11.12 Output Enable Filter

The Output Enable Filter enables the LFDATA output once the incoming signal meets the wake-up sequence requirements (see **Section 11.15 "Configurable Output Enable Filter"**).

11.13 RSSI (Received Signal Strength Indicator)

The RSSI provides a current which is proportional to the input signal amplitude (see **Section 11.31.3 "Received Signal Strength Indicator (RSSI) Output"**).

11.14 Analog Front-End Timers

The AFE has an internal 32 kHz RC oscillator. The oscillator is used in several timers:
• Inactivity timer
• Alarm timer
• Pulse Width timer
• Period timer
• AGC settling timer

11.14.1 RC OSCILLATOR

The RC oscillator is low power, 32 kHz ± 10% over temperature and voltage variations.

FIGURE 11-3: **BIDIRECTIONAL PASSIVE KEYLESS ENTRY (PKE) SYSTEM APPLICATION EXAMPLE**

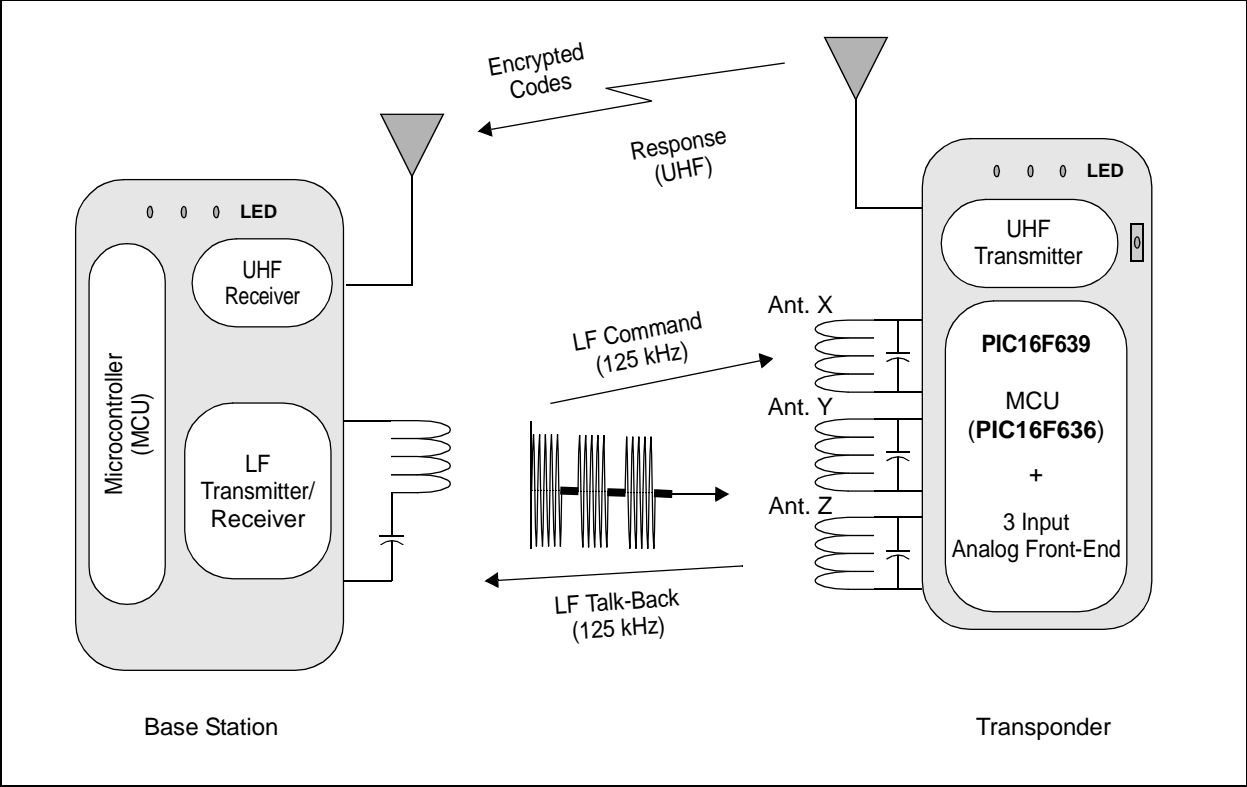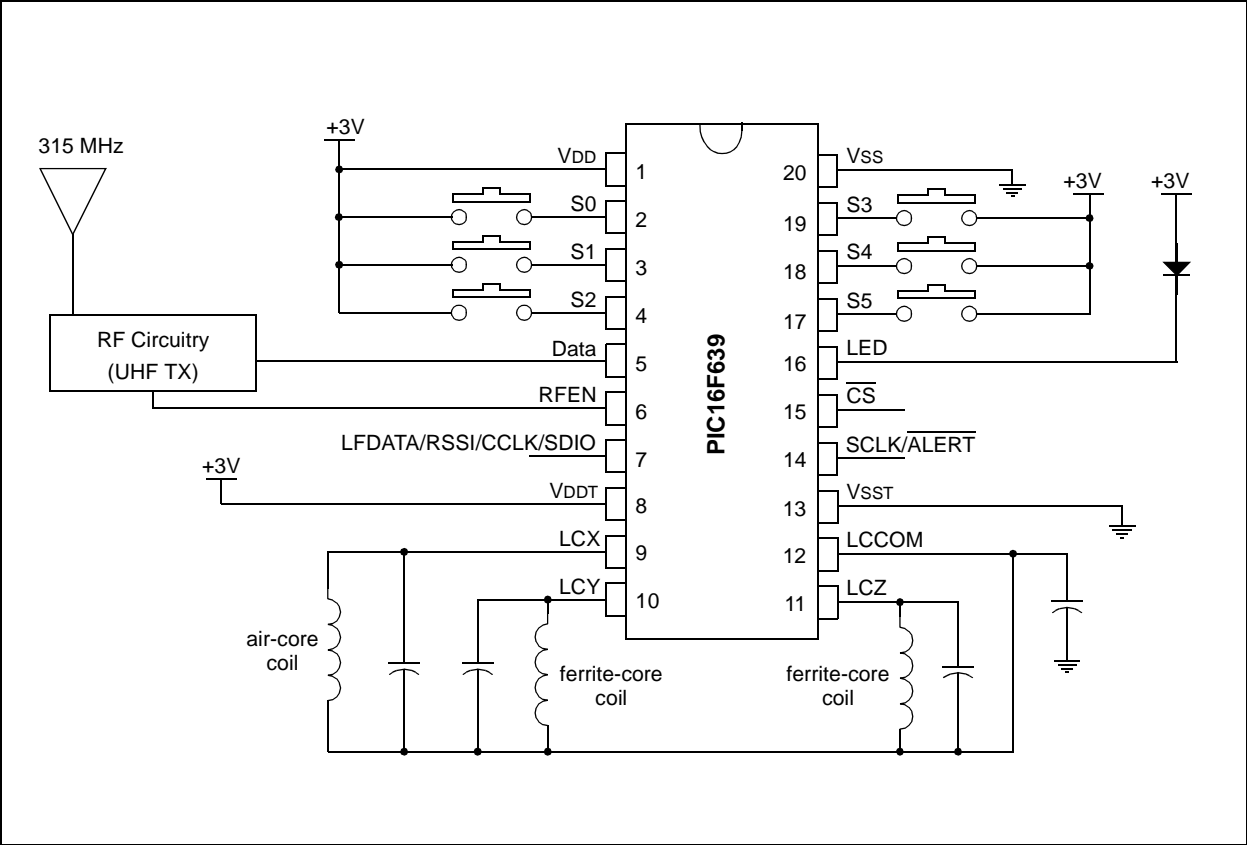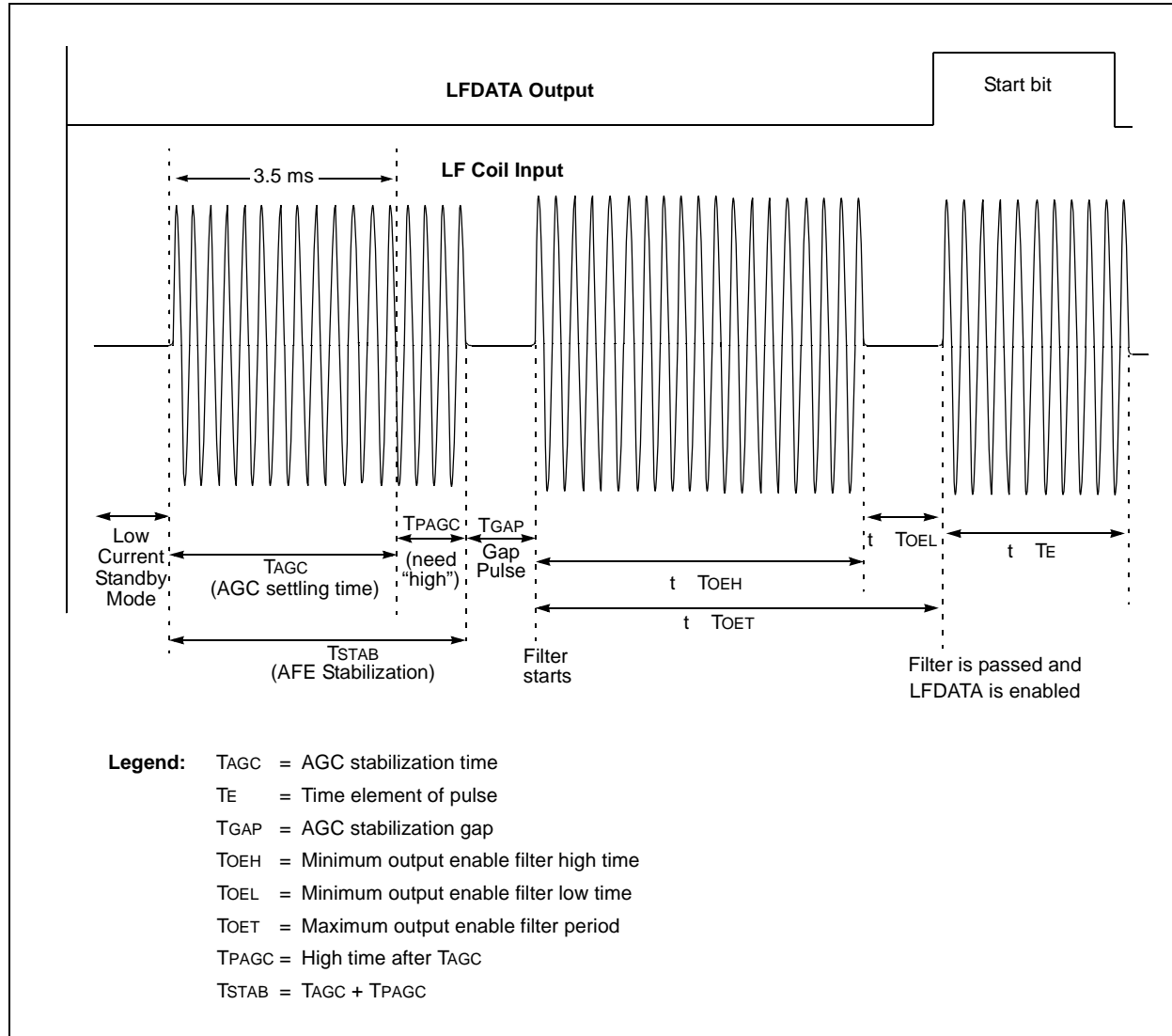**FIGURE 11-4:** **PASSIVE KEYLESS ENTRY (PKE) TRANSPONDER CONFIGURATION EXAMPLE**

FIGURE 11-6: OUTPUT ENABLE FILTER TIMING EXAMPLE (DETAILED)

Legend:

T_{AGC}	=	AGC stabilization time
T_E	=	Time element of pulse
T_{GAP}	=	AGC stabilization gap
T_{OEH}	=	Minimum output enable filter high time
T_{OEL}	=	Minimum output enable filter low time
T_{OET}	=	Maximum output enable filter period
T_{PAGC}	=	High time after T_{AGC}
T_{STAB}	=	$T_{AGC} + T_{PAGC}$

PIC12F635/PIC16F636/639

FIGURE 11-19: DETAILED SPI INTERFACE TIMING (AFE)
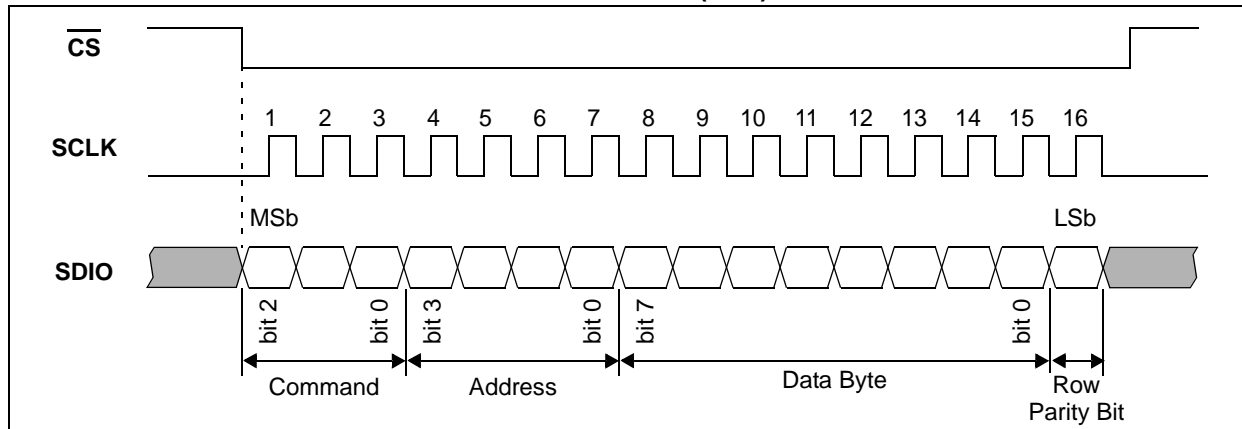
11.32.2.1 Clamp On Command

This command results in activating (turning on) the modulation transistors of all enabled channels; channels enabled in Configuration Register 0 (Register 11-1).

11.32.2.2 Clamp Off Command

This command results in de-activating (turning off) the modulation transistors of all channels.

11.32.2.3 Sleep Command

This command places the AFE in Sleep mode – minimizing current draw by disabling all but the essential circuitry. Any other command wakes the AFE (example: Clamp Off command).

11.32.2.4 Soft Reset Command

The AFE issues a Soft Reset when it receives an external Soft Reset command. The external Soft Reset command is typically used to end a SPI communication sequence or to initialize the AFE for the next signal detection sequence, etc. See **Section 11.20 "Soft Reset"** for more details on Soft Reset.

If a Soft Reset command is sent during a "Clamp-on" condition, the AFE still keeps the "Clamp-on" condition after the Soft Reset execution. The Soft Reset is executed in Active mode only, not in Standby mode. The SPI Soft Reset command is ignored if the AFE is not in Active mode.

11.32.2.5 AGC Preserve On Command

This command results in preserving the AGC level during each AGC settling time and apply the value to the data slicing circuit for the following data stream. The preserved AGC value is reset by a Soft Reset, and a new AGC value is acquired and preserved when it starts a new AGC settling time. This feature is disabled by an AGC Preserve Off command (see **Section 11.19 "AGC Preserve"**).

11.32.2.6 AGC Preserve Off Command

This command disables the AGC preserve feature and returns the AFE to the normal AGC tracking mode, fast tracking during AGC settling time and slow tracking after that (see **Section 11.19 "AGC Preserve"**).

11.32.3 CONFIGURATION REGISTERS

The AFE includes 8 Configuration registers, including a column parity register and AFE Status Register. All registers are readable and writable via SPI, except STATUS register, which is readable only. Bit 0 of each register is a row parity bit (except for the AFE Status Register 7) that makes the register contents an odd number.

12.0 SPECIAL FEATURES OF THE CPU

The PIC12F635/PIC16F636/639 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset
  - Power-on Reset (POR)
  - Wake-up Reset (WUR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator selection
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming™

The PIC12F635/PIC16F636/639 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a nominal 64 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer Wake-up
- An Interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options (see Register 12-1).

12.1 Configuration Bits

The Configuration Word bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 12-1. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "PIC12F6XX/16F6XX Memory Programming Specification" (DS41204) for more information.

FIGURE 12-2: **RECOMMENDED MCLR CIRCUIT**
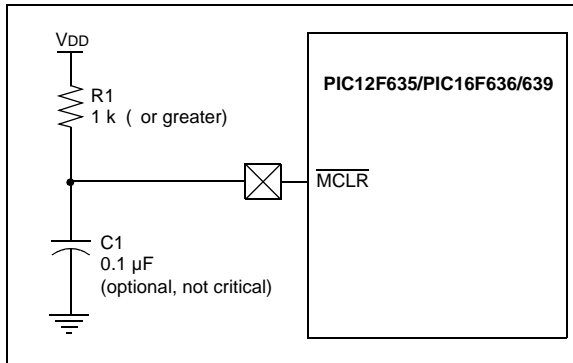
12.6   Brown-out Reset (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register select one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = 01, the SBOREN bit of the PCON register enables/disables the BOR allowing it to be controlled in software. By selecting BOREN<1:0>, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 12-1 for the Configuration Word definition.

If V_{DD} falls below V_{BOD} for greater than parameter (T_{BOD}) (see **Section 15.0 "Electrical Specifications"**), the Brown-out situation will reset the device. This will occur regardless of V_{DD} slew rate. A Reset is not ensured to occur if V_{DD} falls below V_{BOD} for less than parameter (T_{BOD}).

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until V_{DD} rises above V_{BOD} (see Figure 12-3). The Power-up Timer will now be invoked, if enabled and will keep the chip in Reset an additional nominal 64 ms.

> **Note:** The Power-up Timer is enabled by the PWRTE bit in the Configuration Word register.

If V_{DD} drops below V_{BOD} while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once V_{DD} rises above V_{BOD}, the Power-up Timer will execute a 64 ms Reset.

FIGURE 12-3:   **BROWN-OUT RESET SITUATIONS**

Note 1:   Nominal 64 ms delay only if PWRTE bit is programmed to '0'.
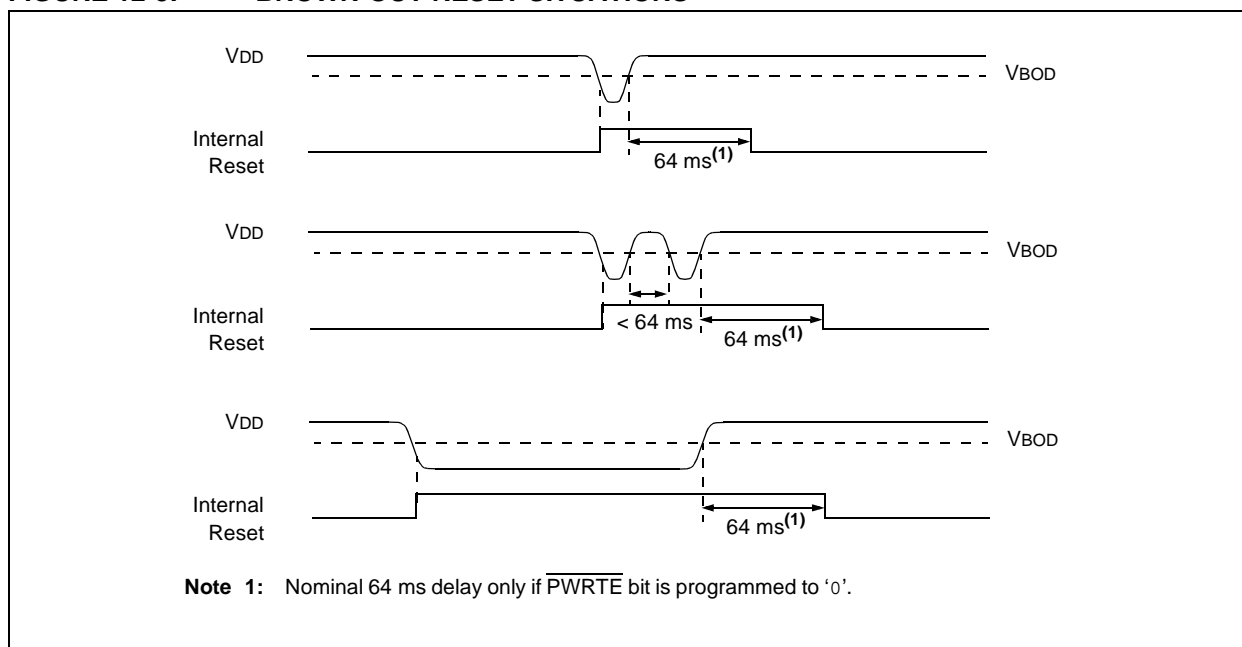
RLF	**Rotate Left f through Carry**
Syntax:	[label] RLF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.

```
 ┌──────────────────────────────┐
 └─◄─ C ◄── Register f ──◄──┘
```
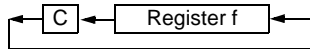
Words:	1
Cycles:	1
<u>Example:</u>	RLF REG1,0

Before Instruction
```
REG1   =   1110 0110
C      =   0
```
After Instruction
```
REG1   =   1110 0110
W      =   1100 1100
C      =   1
```

RRF	**Rotate Right f through Carry**
Syntax:	[label] RRF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

```
 ┌──────────────────────────────┐
 └─► C ──► Register f ──►──┘
```

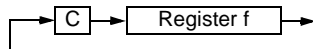| **SLEEP**	**Enter Sleep mode**
Syntax:	[label] SLEEP
Operands:	None
Operation:	00h → WDT, 0 → WDT prescaler, 1 → $\overline{TO}$, 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

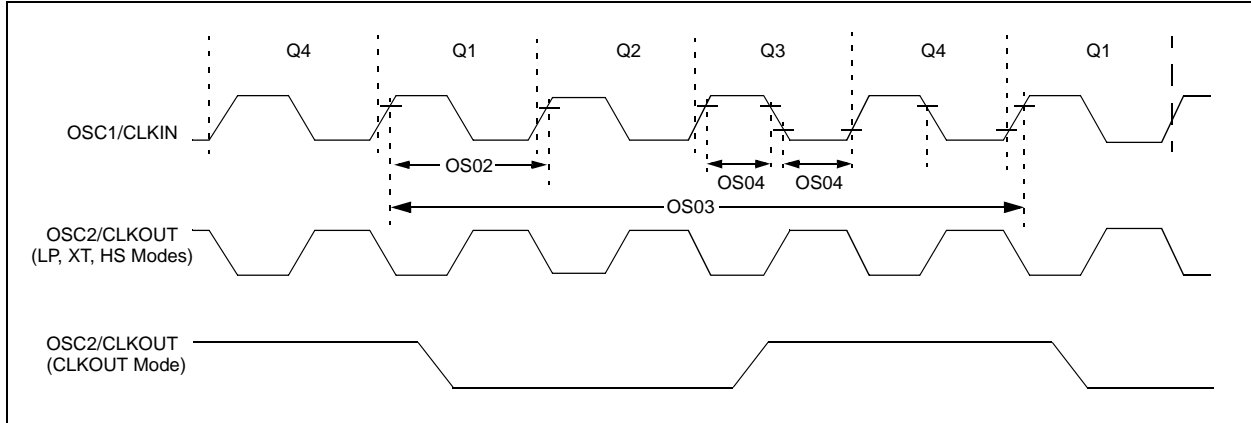| **SUBLW**	**Subtract W from literal**
Syntax:	[label] SUBLW k
Operands:	0 ≤ k ≤ 255
Operation:	k - (W) → (W)
Status Affected:	C, DC, Z
Description:	The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

C = 0	W > k
C = 1	W ≤ k
DC = 0	W<3:0> > k<3:0>
DC = 1	W<3:0> ≤ k<3:0>

15.10 AC Characteristics: PIC12F635/PIC16F636/639 (Industrial, Extended)

FIGURE 15-5:   CLOCK TIMING

TABLE 15-1:   CLOCK OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C TA +125°C							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
OS01	FOSC	External CLKIN Frequency[1]	DC	—	37	kHz	LP Oscillator mode
			DC	—	4	MHz	XT Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	—	20	MHz	EC Oscillator mode
		Oscillator Frequency[1]	—	32.768	—	kHz	LP Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
			1	—	20	MHz	HS Oscillator mode
			DC	—	4	MHz	RC Oscillator mode
OS02	TOSC	External CLKIN Period[1]	27	—		µ s	LP Oscillator mode
			250	—		ns	XT Oscillator mode
			50	—		ns	HS Oscillator mode
			50	—		ns	EC Oscillator mode
		Oscillator Period[1]	—	30.5	—	µs	LP Oscillator mode
			250	—	10,000	ns	XT Oscillator mode
			50	—	1,000	ns	HS Oscillator mode
			250	—	—	ns	RC Oscillator mode
OS03	TCY	Instruction Cycle Time[1]	200	TCY	DC	ns	TCY = 4/FOSC
OS04*	TosH, TosL	External CLKIN High, External CLKIN Low	2	—	—	µs	LP oscillator
			100	—	—	ns	XT oscillator
			20	—	—	ns	HS oscillator
OS05*	TosR, TosF	External CLKIN Rise, External CLKIN Fall	0	—	50	ns	LP oscillator
			0	—	25	ns	XT oscillator
			0	—	15	ns	HS oscillator

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1:   Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

## 16.0   DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are ensured to operate properly only within the specified range.

> **Note:**   The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3) or (mean - 3) respectively, where   is a standard deviation, over each temperature range.

FIGURE 16-1:   TYPICAL IDD vs. FOSC OVER VDD (EC MODE)
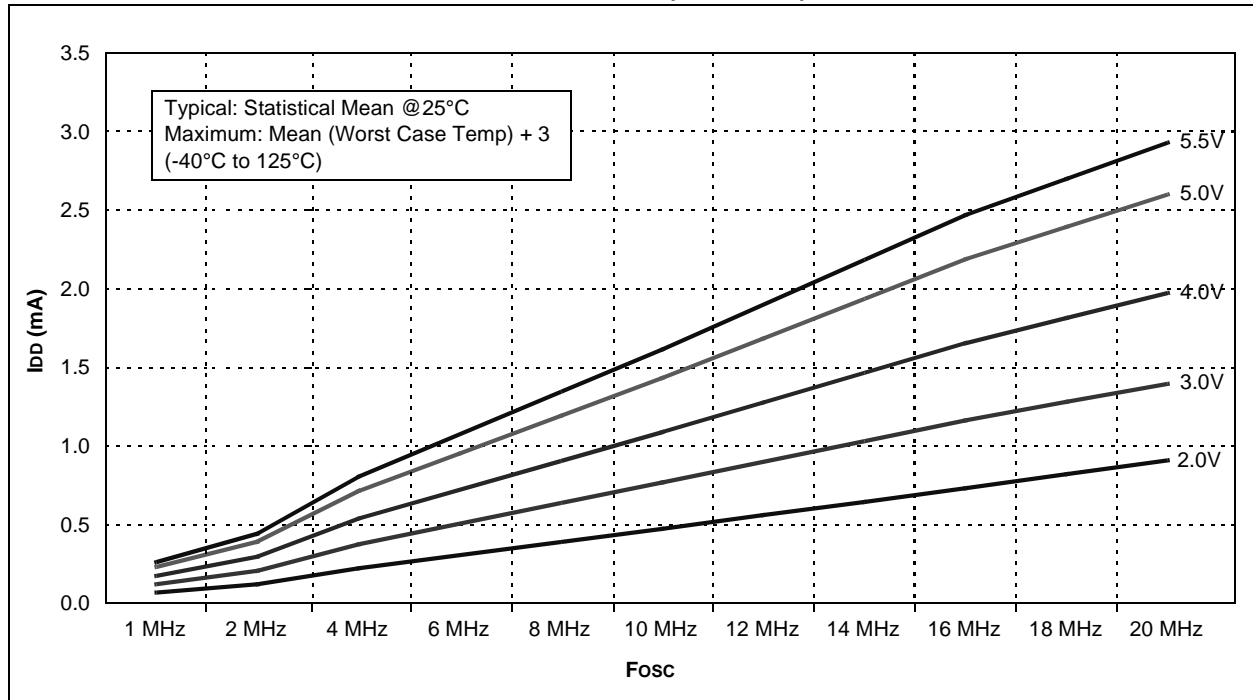
PIC12F635/PIC16F636/639

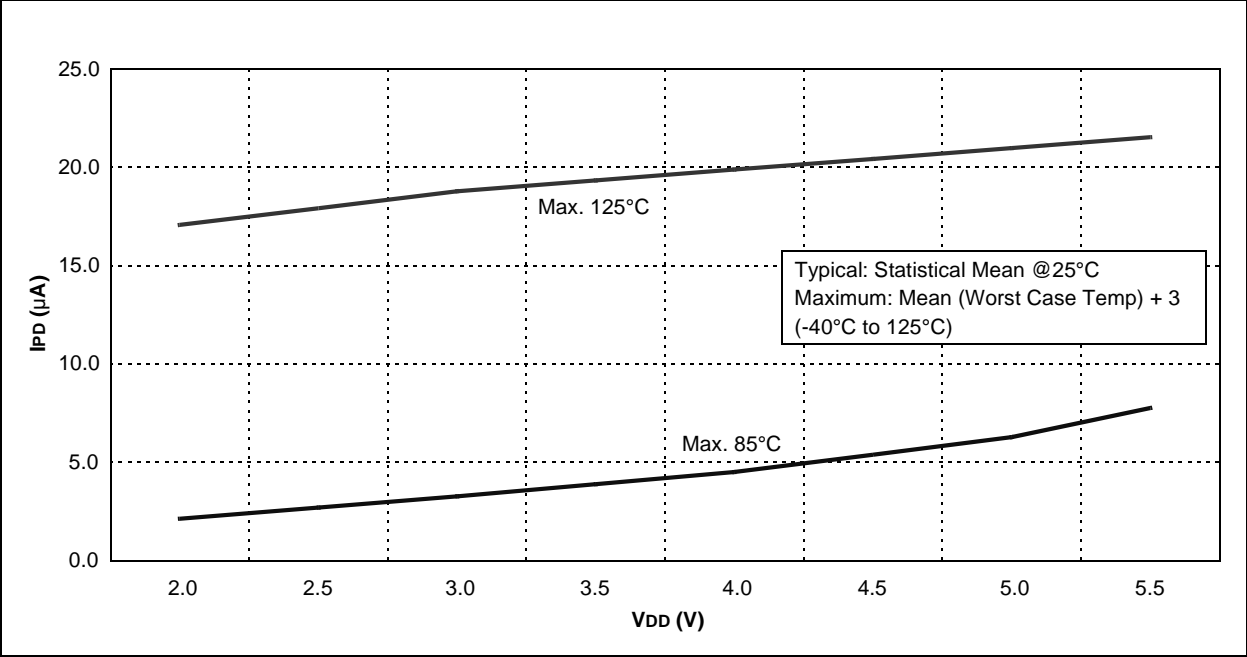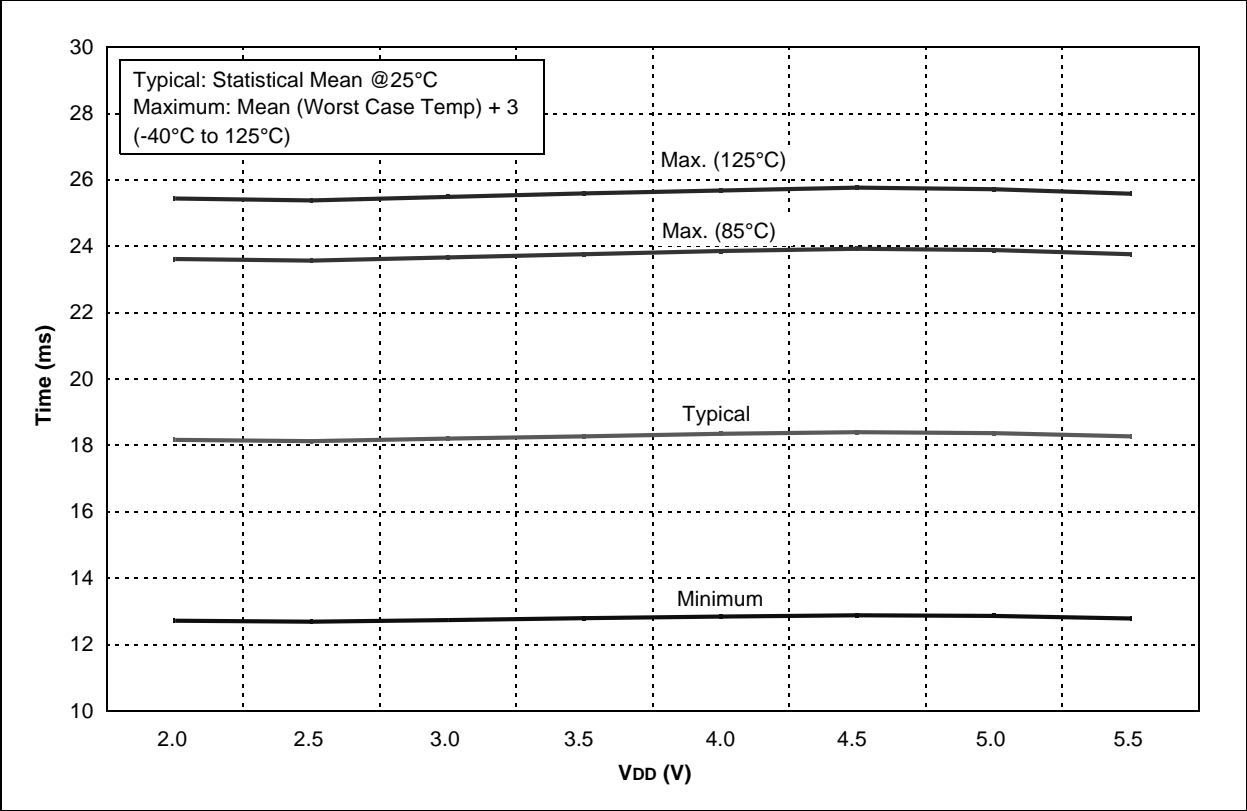**FIGURE 16-18:** **MAXIMUM WDT I**PD **vs. V**DD **OVER TEMPERATURE**

FIGURE 16-19: **WDT PERIOD vs. V**DD **OVER TEMPERATURE**

© 2007 Microchip Technology Inc.
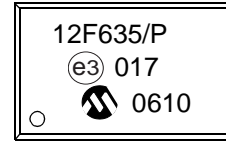
17.0   PACKAGING INFORMATION

17.1   Package Marking Information

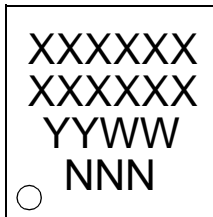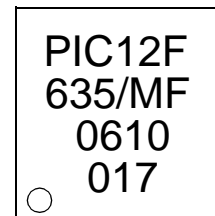8-Lead PDIP   Example

```
┌─────────────────┐              ┌─────────────────┐
│  XXXXXXX        │              │  12F635/P       │
│  XXXXXNNN       │              │  (e3) 017       │
│○    🅜 YYWW      │              │○    🅜 0610      │
└─────────────────┘              └─────────────────┘
```

8-Lead SOIC   Example

```
┌─────────────────┐              ┌─────────────────┐
│  XXXXXXXX       │              │  12F635/        │
│  XXXXYYWW       │              │  SN (e3) 0610   │
│  ○  🅜 NNN       │              │  ○  🅜 017       │
└─────────────────┘              └─────────────────┘
```
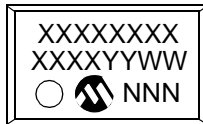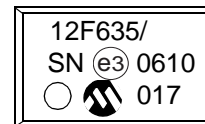
8-Lead DFN (4x4x0.9 mm)   Example

```
┌─────────────────┐              ┌─────────────────┐
│  XXXXXX         │              │  PIC12F         │
│  XXXXXX         │              │  635/MF         │
│   YYWW          │              │   0610          │
│○    NNN         │              │○     017        │
└─────────────────┘              └─────────────────┘
```

8-Lead DFN-S (6x5 mm)   Example

```
┌─────────────────┐              ┌─────────────────┐
│  XXXXXXX        │              │  PICXXF         │
│  XXXXXXX        │              │  XXX-I/         │
│  XXYYWW         │              │  MF0610         │
│   🅜 NNN         │              │   🅜 017         │
│○                │              │○                │
└─────────────────┘              └─────────────────┘
```
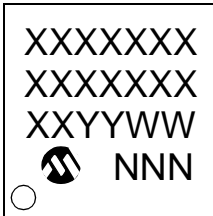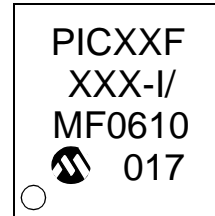
| **Legend:**	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

*   Standard PIC device marking consists of Microchip part number, year code, week code and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

BOTTOM VIEW

NOTE 2
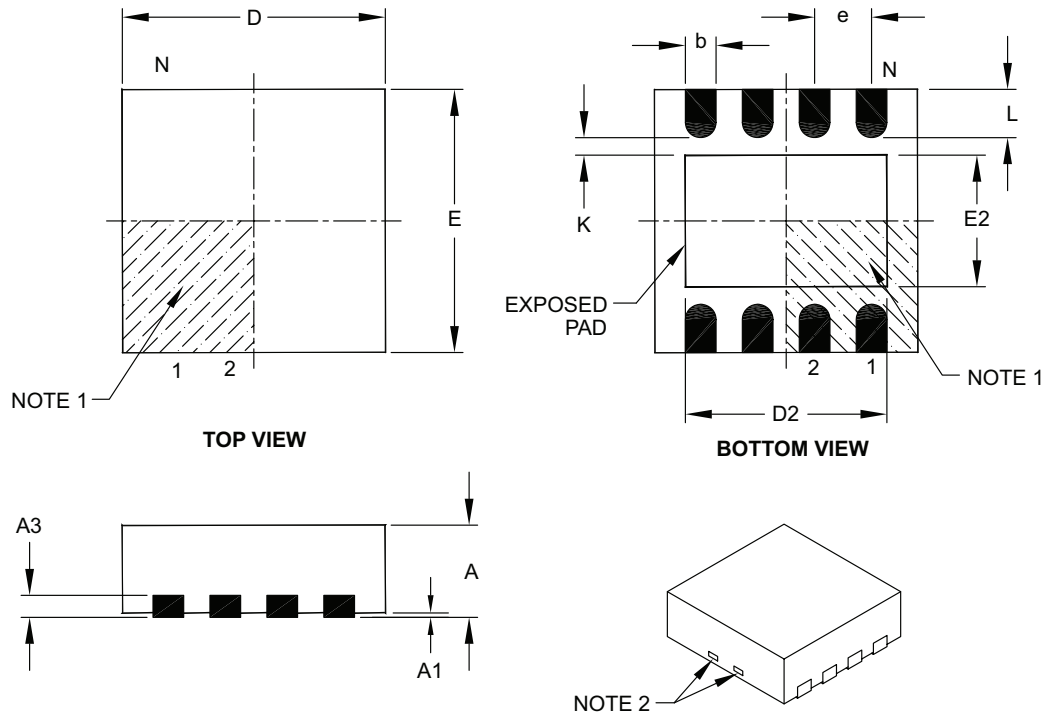
	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.80 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Width	E2	0.00	2.20	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Length	D2	0.00	3.00	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.55	0.65
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131C

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

BOTTOM VIEW
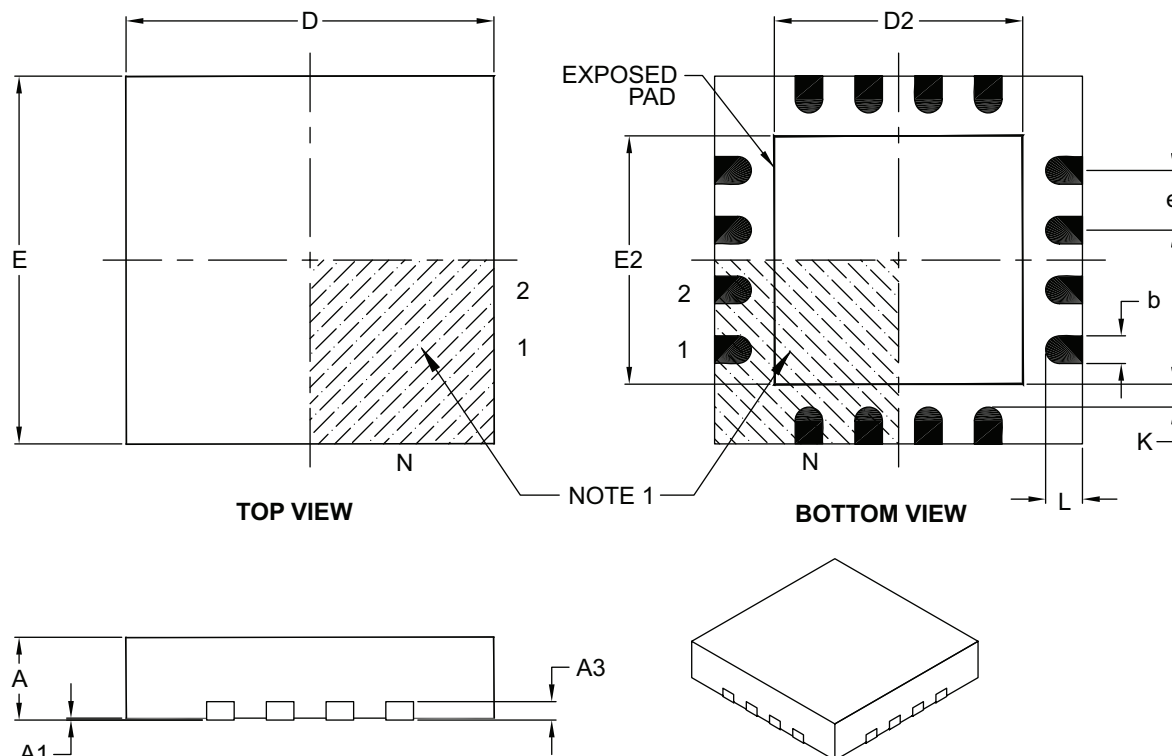
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B