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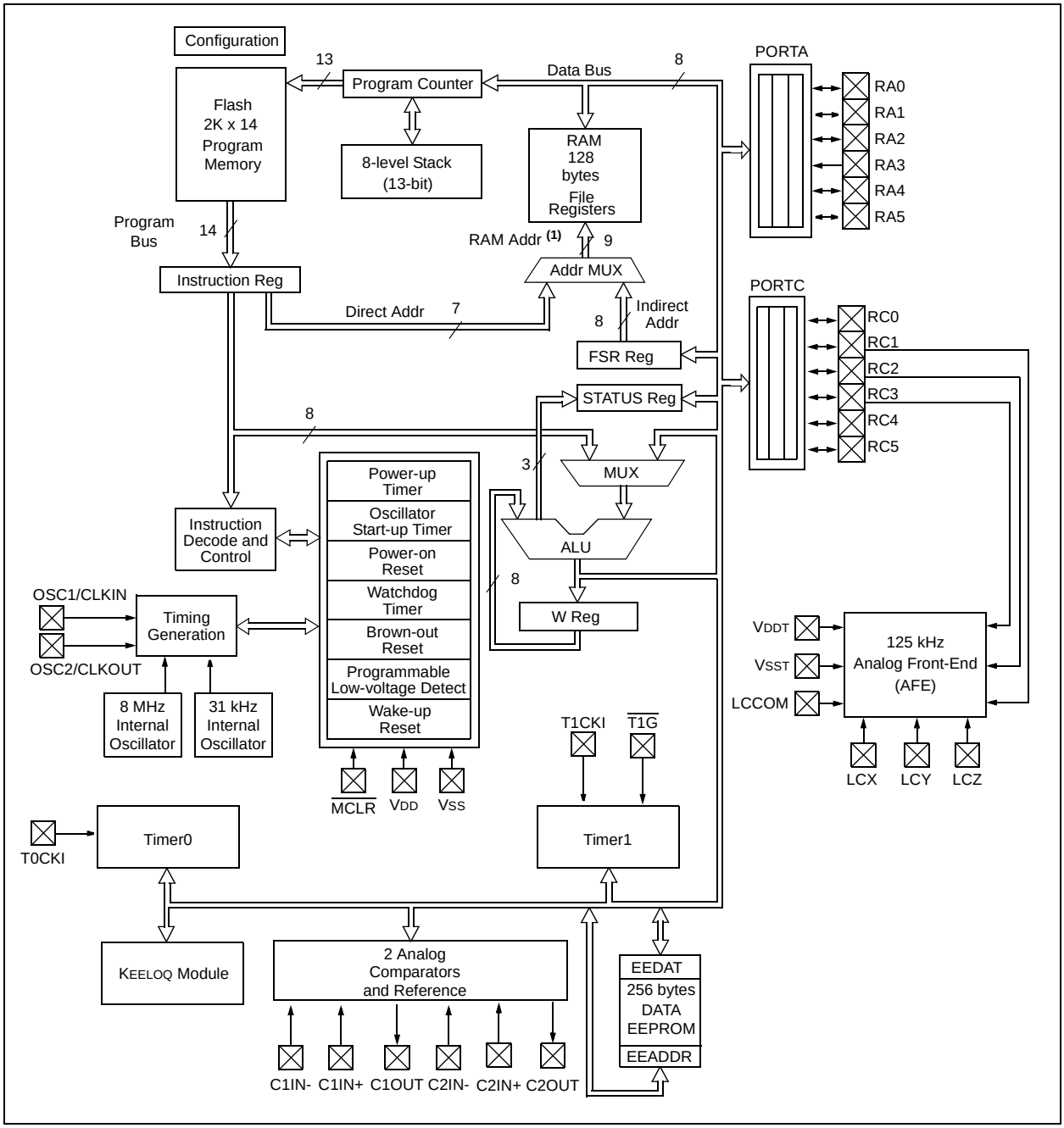
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f635t-i-sn

FIGURE 1-3: PIC16F639 BLOCK DIAGRAM



2.2.1 GENERAL PURPOSE REGISTER

The register file is organized as 64 x 8 for the PIC12F635 and 128 x 8 for the PIC16F636/639. Each register is accessed, either directly or indirectly, through the File Select Register, FSR (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Figure 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-4: PIC16F636/639 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr.(1)	00h	Indirect addr. (1)	80h	Accesses 00h-0Bh	100h	Accesses 80h-8Bh	180h
TMR0	01h	OPTION_REG	81h		101h		181h
PCL	02h	PCL	82h		102h		182h
STATUS	03h	STATUS	83h		103h		183h
FSR	04h	FSR	84h		104h		184h
PORTA	05h	TRISA	85h		105h		185h
	06h		86h		106h		186h
PORTC	07h	TRISC	87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah		10Ah		18Ah
INTCON	0Bh	INTCON	8Bh		10Bh		18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
	0Dh		8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh		10Fh		18Fh
T1CON	10h	OSCTUNE	90h	CRCON	110h		190h
	11h		91h	CRDAT0(2)	111h		191h
	12h		92h	CRDAT1(2)	112h		192h
	13h		93h	CRDAT2(2)	113h		193h
	14h	LVDCON	94h	CRDAT3(2)	114h		194h
	15h	WPUDA	95h		115h		195h
	16h	IOCA	96h		116h		196h
	17h	WDA	97h		117h		197h
WDTCON	18h		98h		118h		198h
CMCON0	19h	VRCON	99h		119h		199h
CMCON1	1Ah	EEDAT	9Ah		11Ah		19Ah
	1Bh	EEADR	9Bh		11Bh		19Bh
	1Ch	EECON1	9Ch		11Ch		19Ch
	1Dh	EECON2(1)	9Dh		11Dh		19Dh
	1Eh		9Eh		11Eh		19Eh
	1Fh		9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 32 Bytes	A0h		120h		1A0h
			BFh				
			C0h				
			EFh		16Fh		1EFh
		Accesses 70h-7Fh	F0h	Accesses 70h-7Fh	170h	Accesses Bank 0	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: CRDAT<3:0> registers are KEELOQ hardware peripheral related registers and require the execution of the "KEELOQ® Encoder License Agreement" regarding implementation of the module and access to related registers. The "KEELOQ® Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ or by contacting your local Microchip Sales Representative.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (GPR and SFR)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS,` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF, BSF, SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see **Section 13.0 "Instruction Set Summary"**

Note 1: The C and DC bits operate as a $\overline{Borrow}$ and Digit $\overline{Borrow}$ out bit, respectively, in subtraction.

REGISTER 2-1: STATUS: STATUS REGISTER

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
`1` = Bank 2, 3 (100h-1FFh)
`0` = Bank 0, 1 (00h-FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
`00` = Bank 0 (00h-7Fh)
`01` = Bank 1 (80h-FFh)
`10` = Bank 2 (100h-17Fh)
`11` = Bank 3 (180h-1FFh)

bit 4 **$\overline{TO}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Borrow}$ bit (`ADDWF, ADDLW, SUBLW, SUBWF` instructions)(1)
`1` = A carry-out from the 4th low-order bit of the result occurred
`0` = No carry-out from the 4th low-order bit of the result

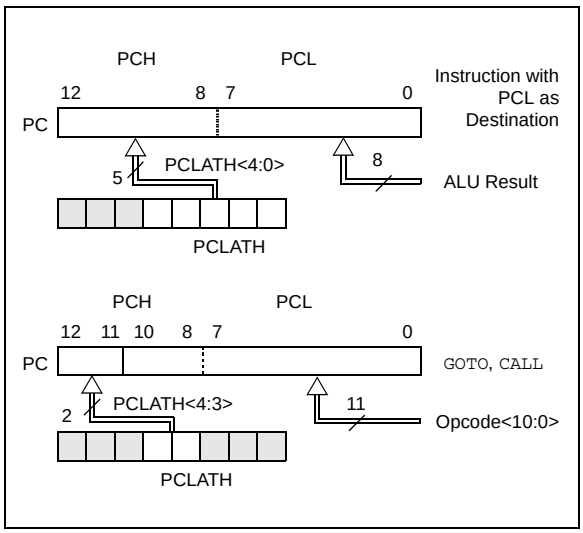
bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF, ADDLW, SUBLW, SUBWF` instructions)(1)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF, RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-5 shows the two situations for the loading of the PC. The upper example in Figure 2-5 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-5 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-5: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper 5 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). Care should be exercised when jumping into a look-up table or program branch table (computed GOTO) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, "*Implementing a Table Read*" (DS00556).

2.3.2 STACK

The PIC12F635/PIC16F636/639 family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1:	There are no Status bits to indicate stack overflow or stack underflow conditions.
2:	There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit of the STATUS register, as shown in Figure 2-6.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
            MOVLW   0x20    ;initialize pointer
            MOVWF   FSR     ;to RAM
NEXT        CLRF    INDF    ;clear INDF register
            INCF    FSR     ;INC POINTER
            BTFSS   FSR,4   ;all done?
            GOTO    NEXT    ;no clear next
CONTINUE                    ;yes continue
```

4.0 I/O PORTS

There are as many as twelve general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

4.1 PORTA and the TRISA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 4-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). The exception is RA3, which is input only and its TRIS bit will always read as '1'. Example 4-1 shows how to initialize PORTA.

Note:	PORTA = GPIO TRISA = TRISIO

Reading the PORTA register (Register 4-1) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. RA3 reads '0' when MCLRE = 1.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

Note:	The CMCON0 register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 4-1: INITIALIZING PORTA

```
BANKSEL PORTA          ;
CLRF    PORTA          ;Init PORTA
MOVLW   07h            ;Set RA<2:0> to
MOVWF   CMCON0         ;digital I/O
BSF     STATUS,RP0     ;Bank 1
BCF     STATUS,RP1     ;
MOVLW   0Ch            ;Set RA<3:2> as inputs
MOVWF   TRISA          ;and set RA<5:4,1:0>
                       ;as outputs
```

4.2 Additional Pin Functions

Every PORTA pin on the PIC12F635/PIC16F636/639 has an interrupt-on-change option and a weak pull-up/pull-down option. RA0 has an Ultra Low-Power Wake-up option. The next three sections describe these functions.

4.2.1 WEAK PULL-UP/PULL-DOWN

Each of the PORTA pins, except RA3, has an internal weak pull-up and pull-down. The WDA bits select either a pull-up or pull-down for an individual port bit. Individual control bits can turn on the pull-up or pull-down. These pull-ups/pull-downs are automatically turned off when the port pin is configured as an output, as an alternate function or on a Power-on Reset, setting the $\overline{\text{RAPU}}$ bit of the OPTION register. A weak pull-up on RA3 is enabled when configured as $\overline{\text{MCLR}}$ in the Configuration Word register and disabled when high voltage is detected, to reduce current consumption through RA3, while in Programming mode.

Note:	PORTA = GPIO TRISA = TRISIO

6.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 interrupt enable bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note:	The TMR1H:TTMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

6.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set

The device will wake-up on an overflow and execute the next instruction. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

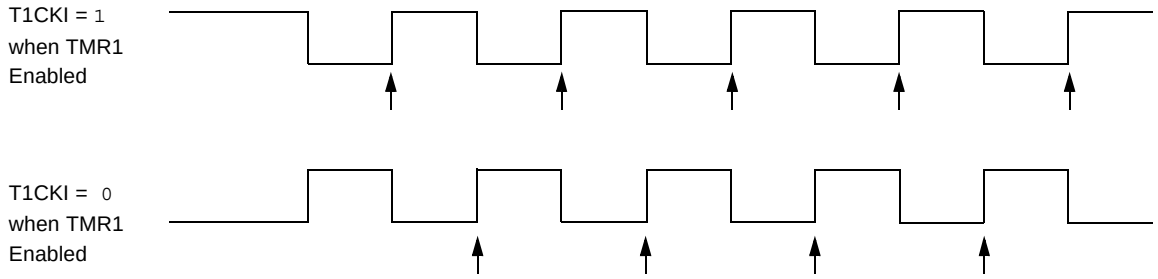
6.9 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see **Section 7.0 “Comparator Module”**.

FIGURE 6-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

9.2 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD of the EECON1 register, as shown in Example 9-1. The data is available, in the very next cycle, in the EEDAT register. Therefore, it can be read in the next instruction. EEDAT holds this value until another read, or until it is written to by the user (during a write operation).

EXAMPLE 9-1: DATA EEPROM READ

```
BANKSEL  EEADR          ;
MOVLW    CONFIG_ADDR    ;
MOVWF    EEADR          ;Address to read
BSF      EECON1,RD      ;EE Read
MOVF     EEDAT,W        ;Move data to W
```

9.3 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDAT register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 9-2.

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit of the PIR1 register must be cleared by software.

EXAMPLE 9-2: DATA EEPROM WRITE

```
          BANKSEL EEADR          ;
          BSF     EECON1,WREN    ;Enable write
          BCF     INTCON,GIE     ;Disable INTs
Required  MOVLW   55h            ;Unlock write
Sequence  MOVWF   EECON2         ;
          MOVLW   AAh            ;
          MOVWF   EECON2         ;
          BSF     EECON1,WR      ;Start the write
          BSF     INTCON,GIE     ;Enable INTS
```

9.4 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM should be verified (see Example 9-3) to the desired value to be written.

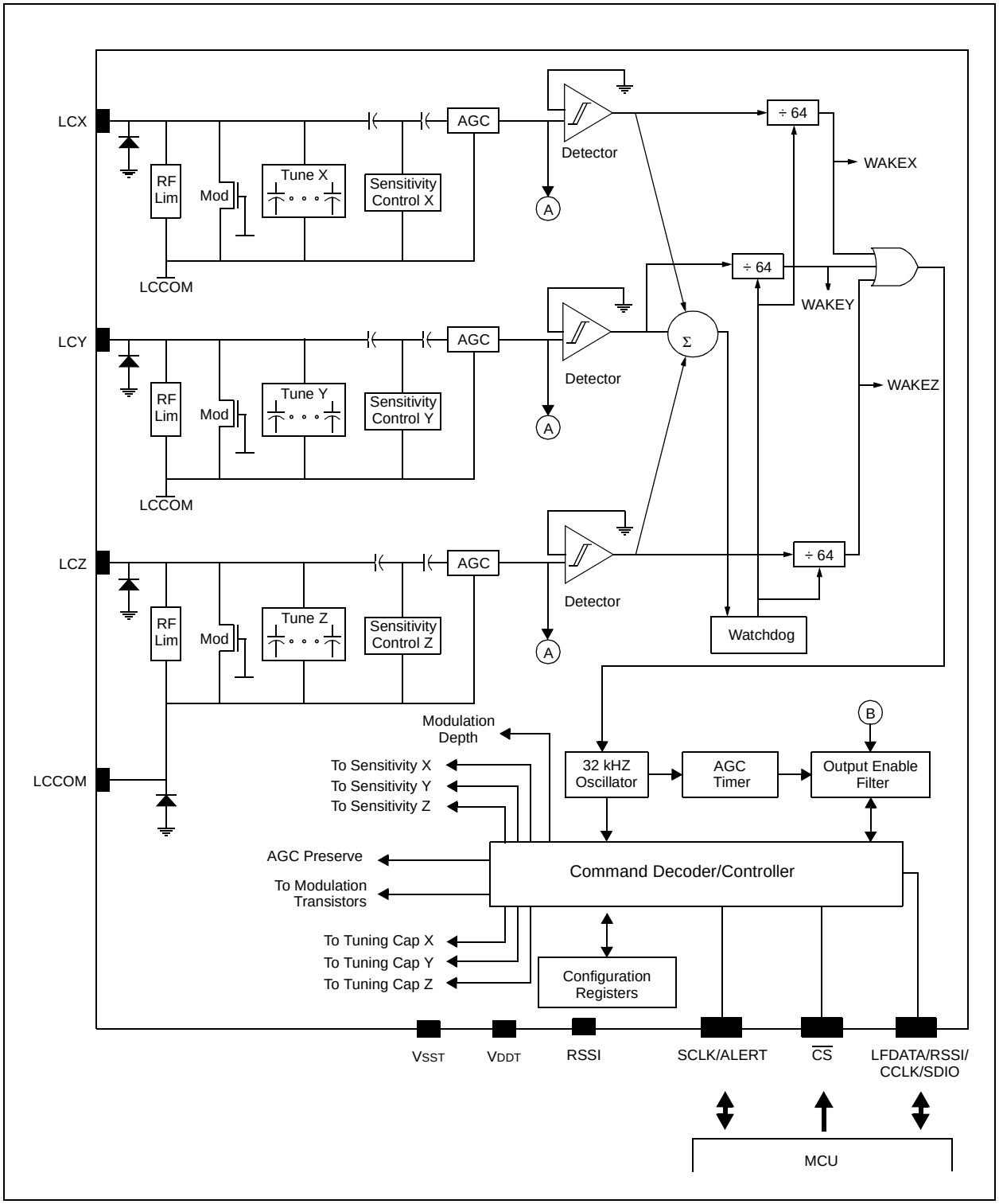
EXAMPLE 9-3: WRITE VERIFY

```
BANKSEL  EEDAT      ;
MOVF     EEDAT,W    ;EEDAT not changed
                    ;from previous write
BSF      EECON1,RD  ;YES, Read the
                    ;value written
XORWF    EEDAT,W    ;
BTFSS    STATUS,Z   ;Is data the same
GOTO     WRITE_ERR  ;No, handle error
:                   ;Yes, continue
```

9.4.1 USING THE DATA EEPROM

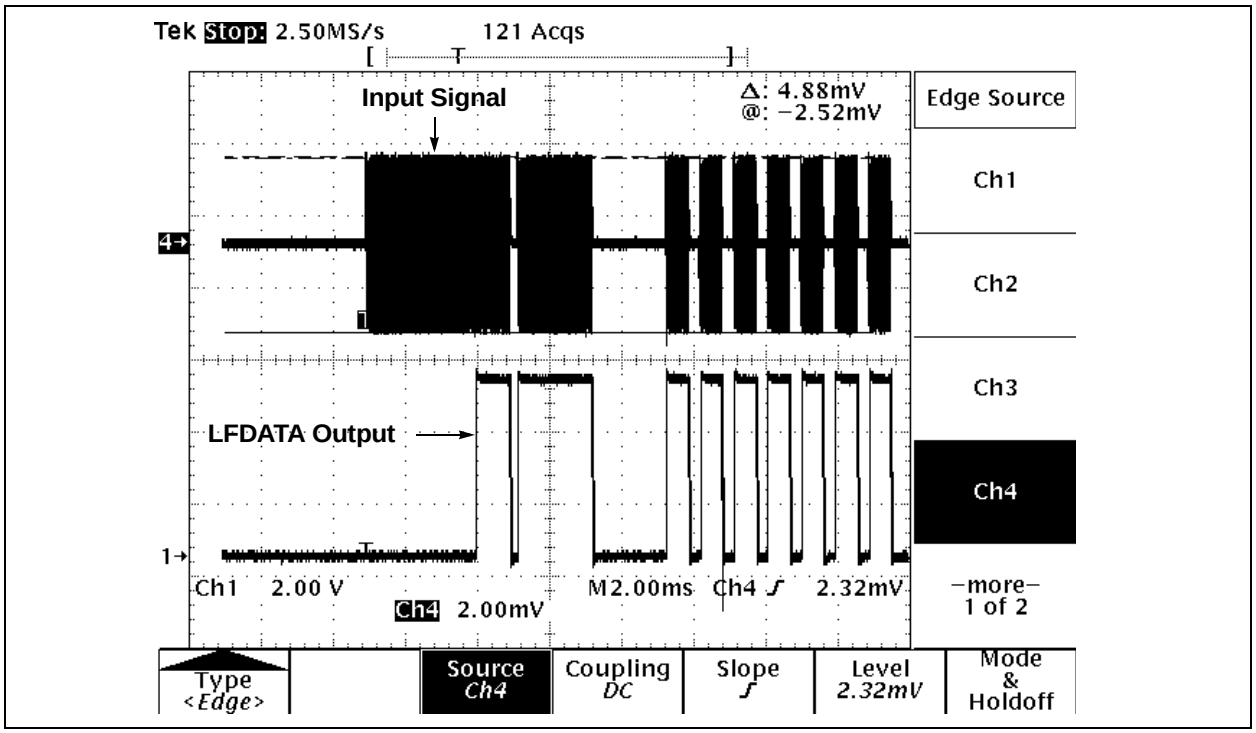
The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). When variables in one section change frequently, while variables in another section do not change, it is possible to exceed the total number of write cycles to the EEPROM (specification D124) without exceeding the total number of write cycles to a single byte (specifications D120 and D120A). If this is the case, then a refresh of the array must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

FIGURE 11-1: FUNCTIONAL BLOCK DIAGRAM – ANALOG FRONT-END



Case I. When Output Enable Filter is disabled: Demodulated output is available immediately after the AGC stabilization time (TAGC). Figure 11-10 shows an example of demodulated output when the Output Enable Filter is disabled.

FIGURE 11-10: INPUT SIGNAL AND DEMODULATOR OUTPUT WHEN THE OUTPUT ENABLE FILTER IS DISABLED



Case II. When Output Enable Filter is enabled: Demodulated output is available only if the incoming signal meets the enable filter timing criteria that is defined in the Configuration Register 0 (Register 11-1). If the criteria is met, the output is available after the low timing (TOEL) of the Enable Filter. Figure 11-11 and Figure 11-12 shows examples of demodulated output when the Output Enable Filter is enabled.

RLF **Rotate Left f through Carry**

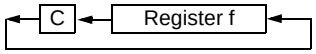
Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register ‘f’ are rotated one bit to the left through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.



Words: 1

Cycles: 1

Example:

```
RLF     REG1,0
```

Before Instruction

```
REG1    =   1110 0110
C       =   0
```

After Instruction

```
REG1    =   1110 0110
W       =   1100 1100
C       =   1
```

RRF **Rotate Right f through Carry**

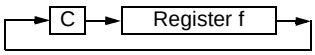
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register ‘f’ are rotated one bit to the right through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.



SLEEP **Enter Sleep mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into Sleep mode with the oscillator stopped.

SUBLW **Subtract W from literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Description: The W register is subtracted (2’s complement method) from the eight-bit literal ‘k’. The result is placed in the W register.

C = 0	W > k
C = 1	W ≤ k
DC = 0	W<3:0> > k<3:0>
DC = 1	W<3:0> ≤ k<3:0>

15.1 DC Characteristics: PIC12F635/PIC16F636-I (Industrial) PIC12F635/PIC16F636-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001			2.0	—	5.5	V	FOSC < = 4 MHz
D001A			2.0	—	5.5	V	FOSC < = 8 MHz, HFINTOSC, EC
D001B			3.0	—	5.5	V	FOSC < = 10 MHz
D001C			4.5	—	5.5	V	FOSC < = 20 MHz
D002	VDR	**RAM Data Retention Voltage(1)**	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See **Section 12.3 "Power-on Reset"** for details.
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See **Section 12.3 "Power-on Reset"** for details.
D005	VBOD	**Brown-out Reset**	2.0	2.1	2.2	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

15.8 Thermal Considerations

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C						
Param No.	**Sym**	**Characteristic**		**Typ**	**Units**	**Conditions**
TH01	θJA	Thermal Resistance Junction to Ambient	PIC12F635	84.6	°C/W	8-pin PDIP package
				163.0	°C/W	8-pin SOIC package
				52.4	°C/W	8-pin DFN 4x4x0.9 mm package
				52.4	°C/W	8-pin DFN-S 6x5 mm package
			PIC16F636	69.8	°C/W	14-pin PDIP package
				85.0	°C/W	14-pin SOIC package
				100.4	°C/W	14-pin TSSOP package
				46.3	°C/W	16-pin QFN 4x0.9mm package
			PIC16F639	108.1	°C/W	20-pin SSOP package
TH02	θJC	Thermal Resistance Junction to Case	PIC12F635	41.2	°C/W	8-pin PDIP package
				38.8	°C/W	8-pin SOIC package
				3.0	°C/W	8-pin DFN 4x4x0.9 mm package
				3.0	°C/W	8-pin DFN-S 6x5 mm package
			PIC16F636	32.5	°C/W	14-pin PDIP package
				31.0	°C/W	14-pin SOIC package
				31.7	°C/W	14-pin TSSOP package
				2.6	°C/W	16-pin QFN 4x0.9mm package
			PIC16F639	32.2	°C/W	20-pin SSOP package
TH03	TJ	Junction Temperature		150	°C	For derated power calculations
TH04	PD	Power Dissipation		—	W	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation		—	W	PINTERNAL = IDD x VDD **(NOTE 1)**
TH06	PI/O	I/O Power Dissipation		—	W	PI/O = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH))
TH07	PDER	Derated Power		—	W	PDER = (TJ - TA)/θJA **(NOTE 2, 3)**

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature.

3: Maximum allowable power dissipation is the lower value of either the absolute maximum total power dissipation or derated power (PDER).

TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
30	TMCL	$\overline{\text{MCLR}}$ Pulse Width (low)	2 5	— —	— —	µs µs	VDD = 5V, -40°C to +85°C VDD = 5V
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	10 10	16 16	29 31	ms ms	VDD = 5V, -40°C to +85°C VDD = 5V
32	TOST	Oscillation Start-up Timer Period**(1, 2)**	—	1024	—	TOSC	**(NOTE 3)**
33*	TPWRT	Power-up Timer Period	40	65	140	ms	
34*	TIOZ	I/O High-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	—	2.0	µs	
35	VBOR	Brown-out Reset Voltage	2.0	—	2.2	V	**(NOTE 4)**
36*	VHYST	Brown-out Reset Hysteresis	—	50	—	mV	
37*	TBOR	Brown-out Reset Minimum Detection Period	100	—	—	µs	VDD ≤ VBOR

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

2: By design.

3: Period of the slower clock.

4: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

FIGURE 16-4: MAXIMUM IDD vs. FOSC OVER VDD (HS MODE)

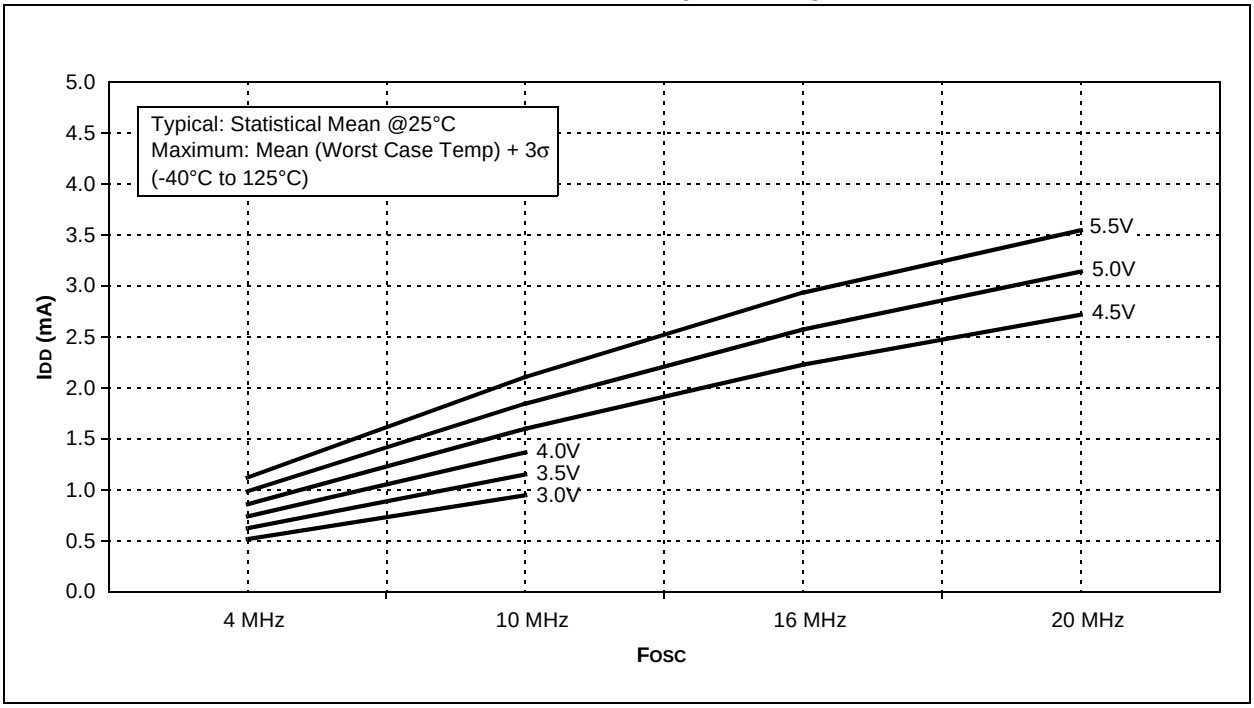


FIGURE 16-5: TYPICAL IDD vs. VDD OVER FOSC (XT MODE)

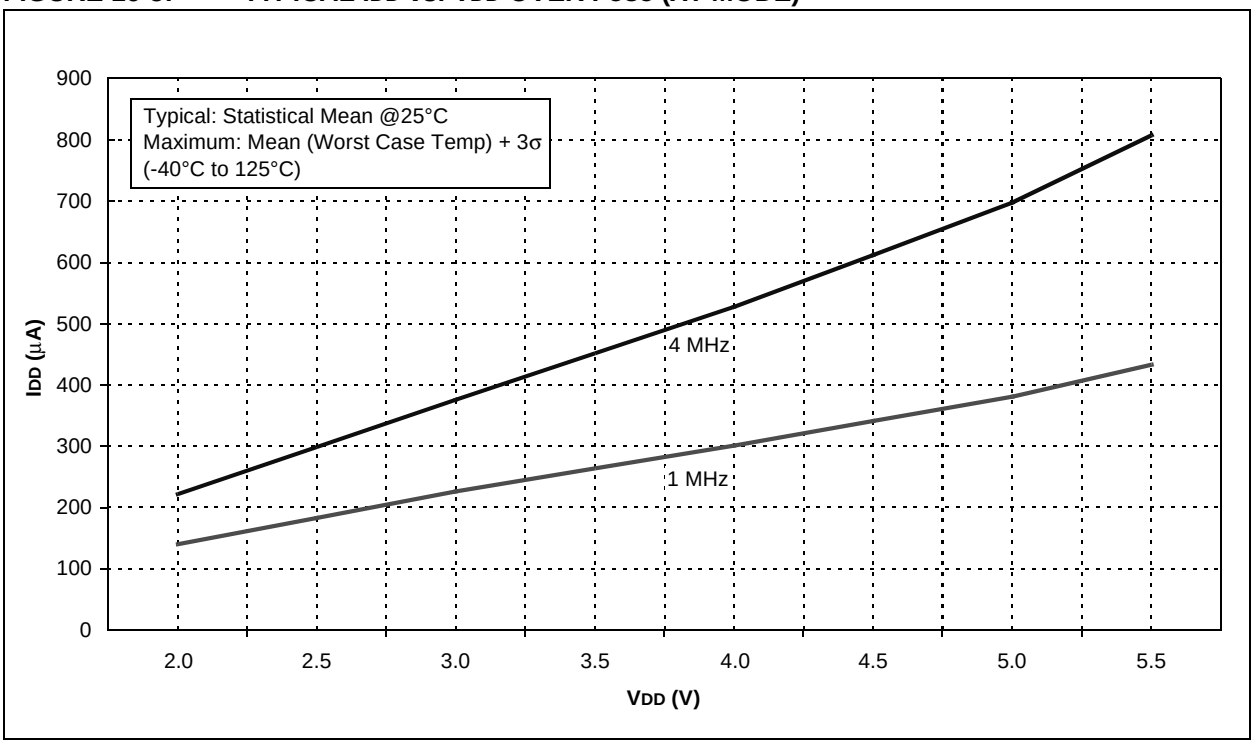


FIGURE 16-32: LFINTOSC FREQUENCY vs. VDD OVER TEMPERATURE (31 kHz)

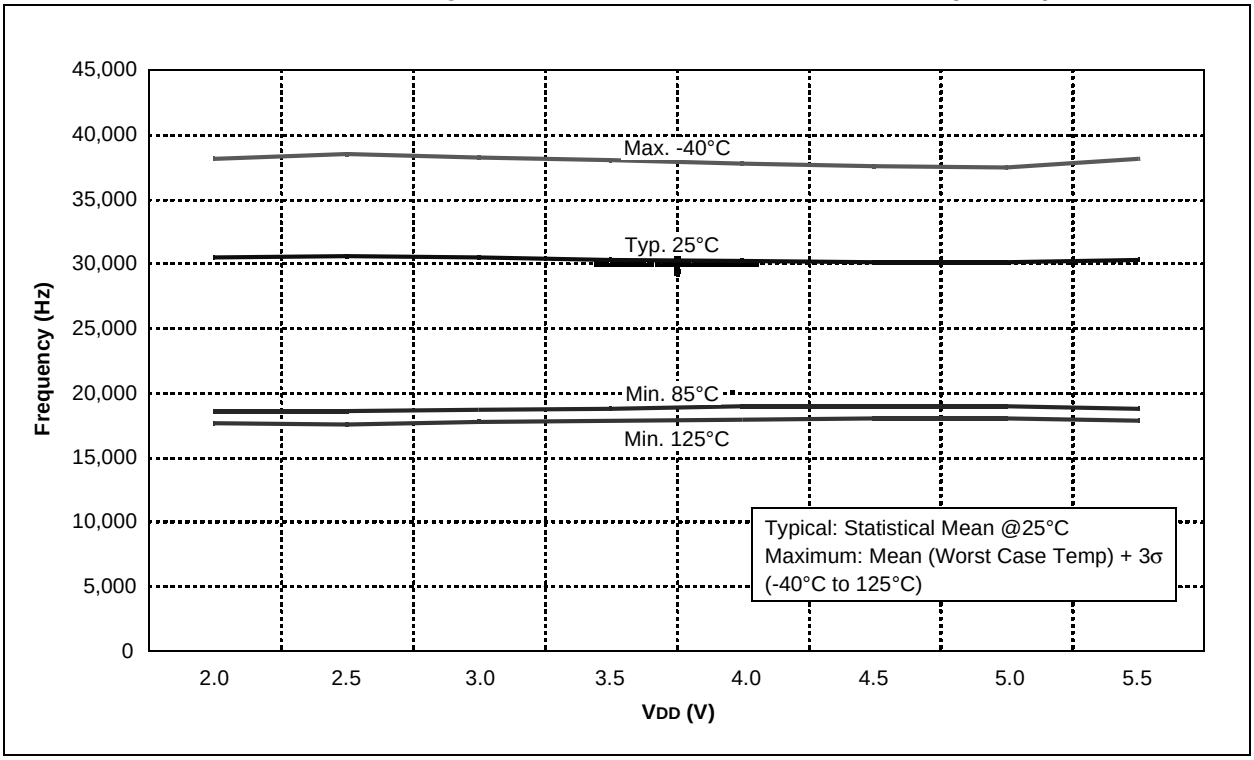
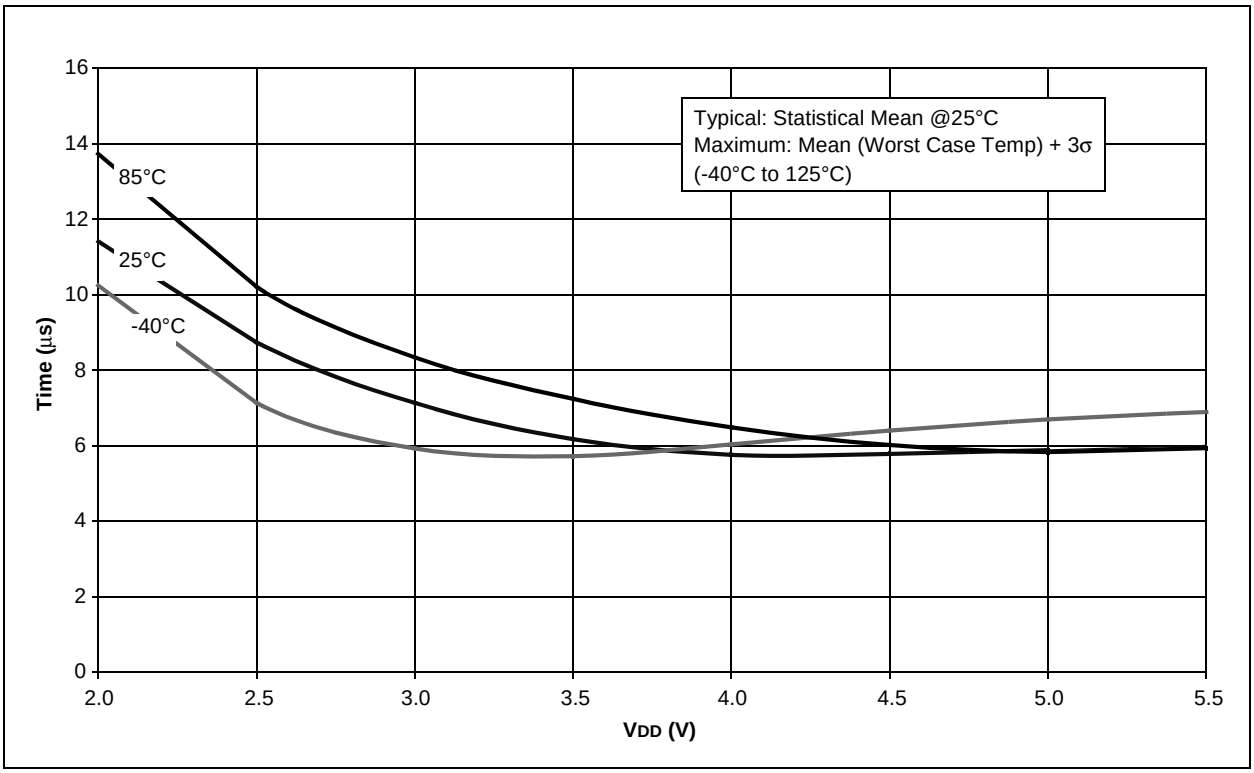


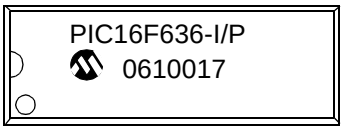
FIGURE 16-33: TYPICAL HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE



17.1 Package Marking Information (Continued)

14-Lead PDIP

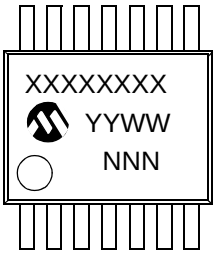
Example



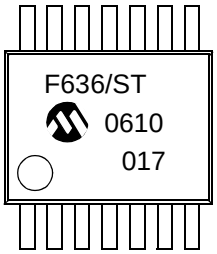
14-Lead SOIC

Example

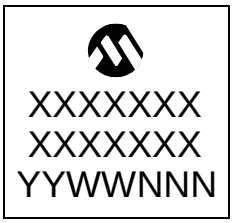
14-Lead TSSOP



Example

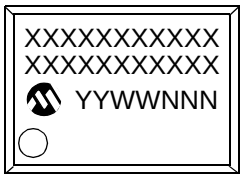


16-Lead QFN

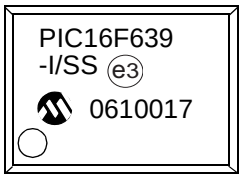


Example

20-Lead SSOP

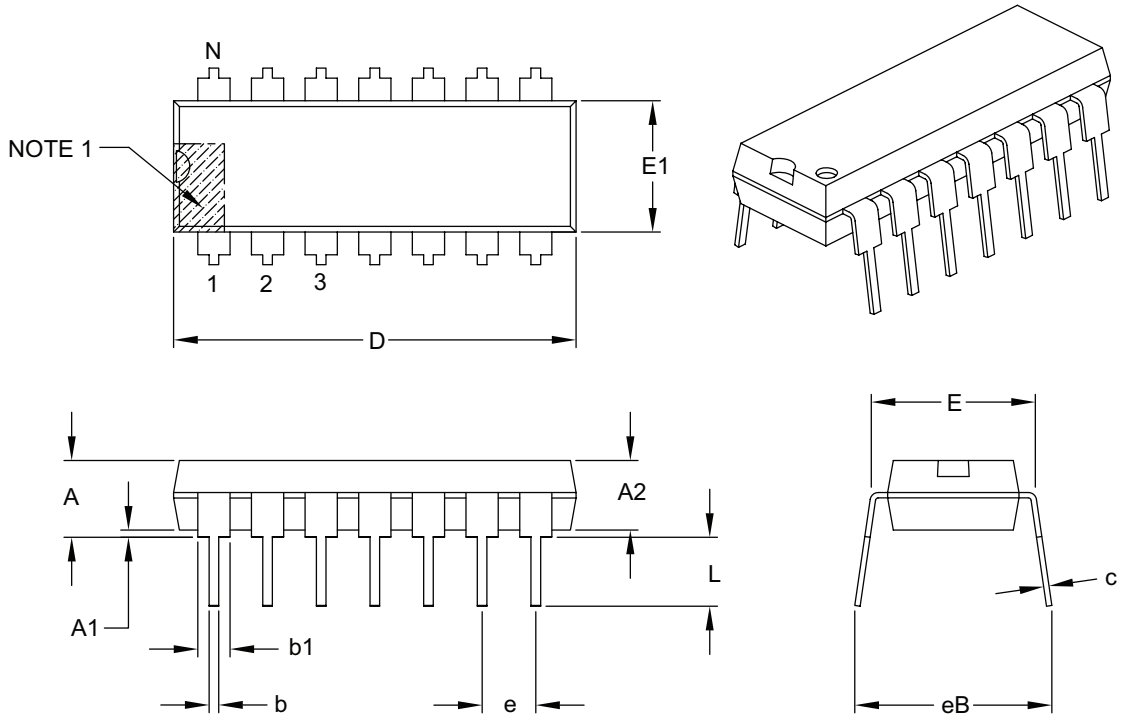


Example



14-Lead Plastic Dual In-Line (P or PD) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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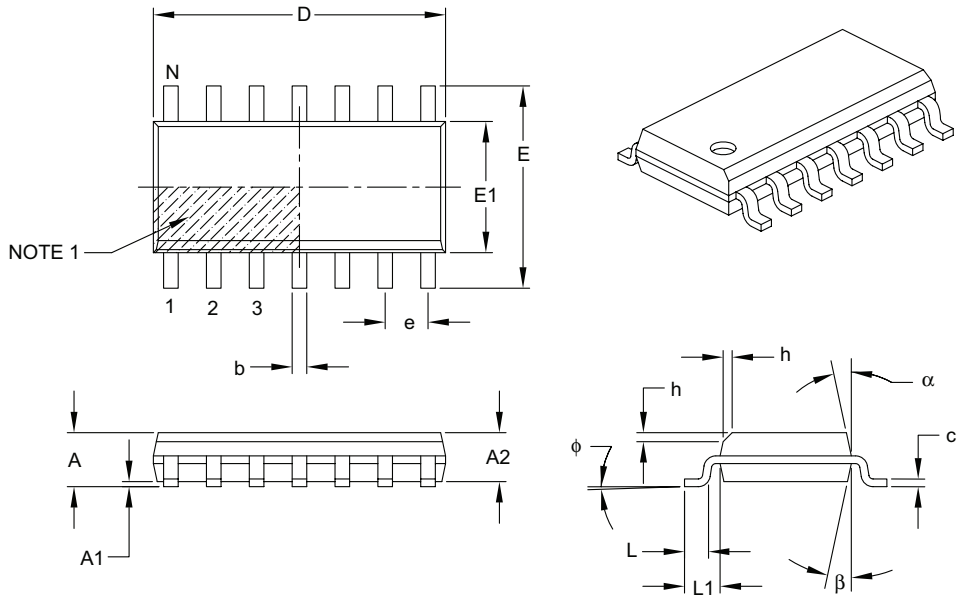
14-Lead Plastic Small Outline (SL or OD) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC12F635(1, 2), PIC16F636(1, 2), PIC16F639(1, 2) VDD range 2.0V to 5.5V	
Temperature Range:	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)	
Package:	MD = Dual-Flat, No Leads, 8-pin (4x4x0.9 mm) MF = Dual-Flat, No Leads, Saw Sing. (6x5 mm) ML = Dual-Flat, No Leads, 16-pin (4x4x0.9 mm) P = Plastic DIP (300 mil body, 5.30 mm) SL = 14-lead Small Outline (3.90 mm) SN = 8-lead Small Outline (3.90 mm) SS = 20-Lead Plastic Shrink Small Outline (5.30 mm) ST = 14-Lead Thin Shrink Small Outline (4.4 mm)	
Pattern:	3-Digit Pattern Code for QTP (blank otherwise)	

Examples:

a) PIC12F635-E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301

b) PIC12F635-I/S = Industrial Temp., SOIC package, 20 MHz

Note 1: F = Standard Voltage Range

2: T = in tape and reel PLCC.