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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16f636-e-p">https://www.e-xfl.com/product-detail/microchip-technology/pic16f636-e-p</a>

# PIC12F635/PIC16F636/639

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## 2.2.1 GENERAL PURPOSE REGISTER

The register file is organized as 64 x 8 for the PIC12F635 and 128 x 8 for the PIC16F636/639. Each register is accessed, either directly or indirectly, through the File Select Register, FSR (see **Section 2.4 “Indirect Addressing, INDF and FSR Registers”**).

## 2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Figure 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the “core” are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

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## 3.3 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are: Oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.
- Internal clock sources are contained internally within the Oscillator module. The Oscillator module has two internal oscillators: the 8 MHz High-Frequency Internal Oscillator (HFINTOSC) and the 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Select (SCS) bit of the OSCCON register. See **Section 3.6 “Clock Switching”** for additional information.

## 3.4 External Clock Modes

### 3.4.1 OSCILLATOR START-UP TIMER (OST)

If the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the Oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 3-1.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see **Section 3.7 “Two-Speed Clock Start-up Mode”**).

**TABLE 3-1: OSCILLATOR DELAY EXAMPLES**

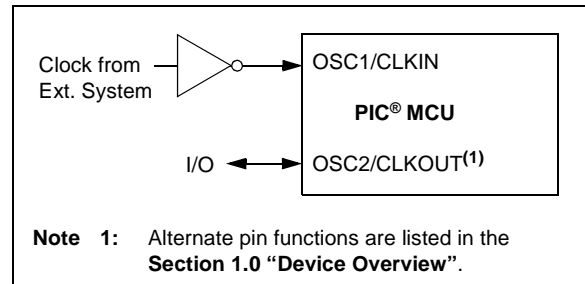
Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	LFINTOSC HFINTOSC	31 kHz 125 kHz to 8 MHz	Oscillator Warm-Up Delay (TWARM)
Sleep/POR	EC, RC	DC – 20 MHz	2 instruction cycles
LFINTOSC (31 kHz)	EC, RC	DC – 20 MHz	1 cycle of each
Sleep/POR	LP, XT, HS	32 kHz to 20 MHz	1024 Clock Cycles (OST)
LFINTOSC (31 kHz)	HFINTOSC	125 kHz to 8 MHz	1 $\mu$ s (approx.)

### 3.4.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 3-2 shows the pin connections for EC mode.

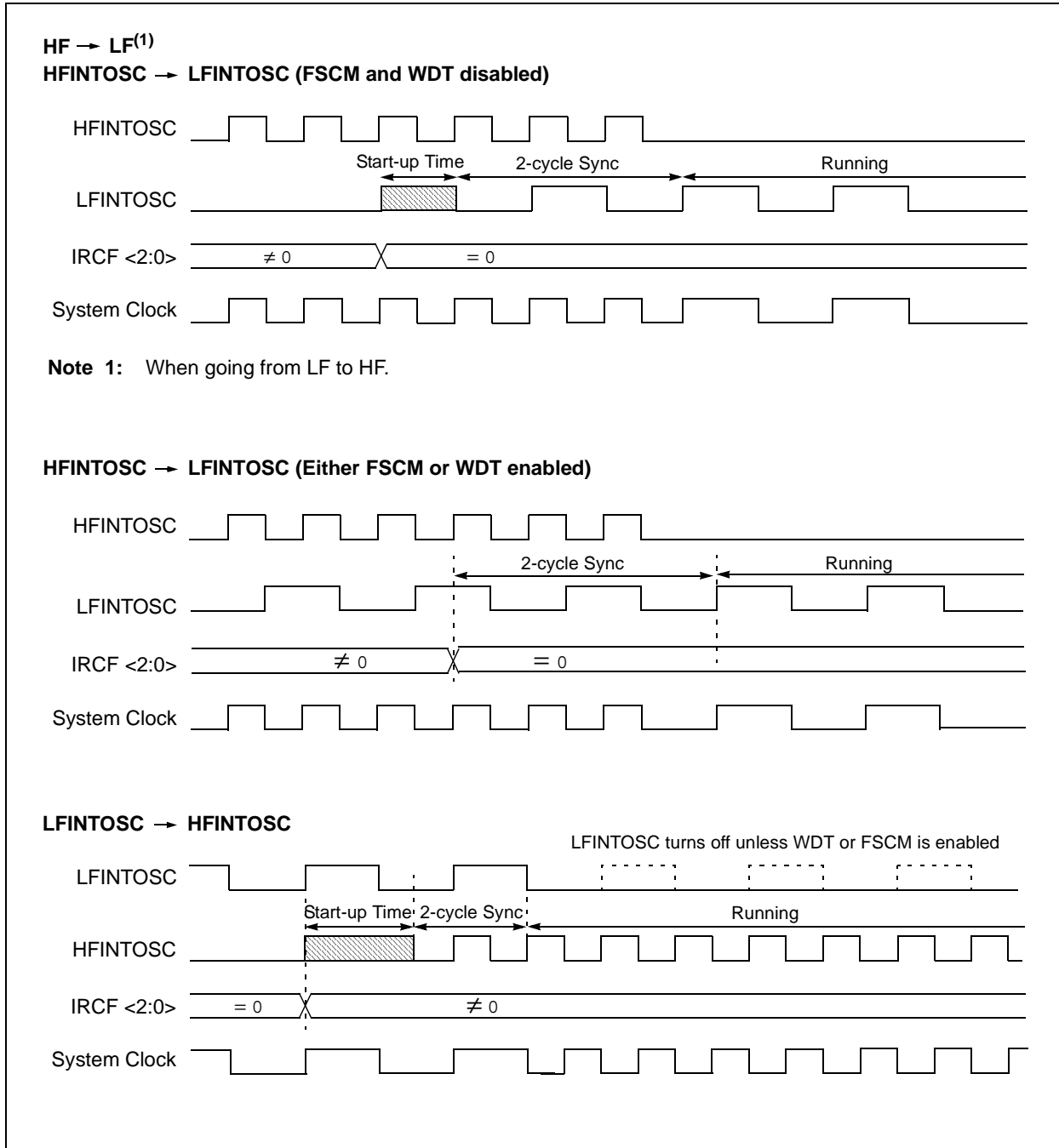
The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

**FIGURE 3-2: EXTERNAL CLOCK (EC) MODE OPERATION**



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**FIGURE 3-6: INTERNAL OSCILLATOR SWITCH TIMING**

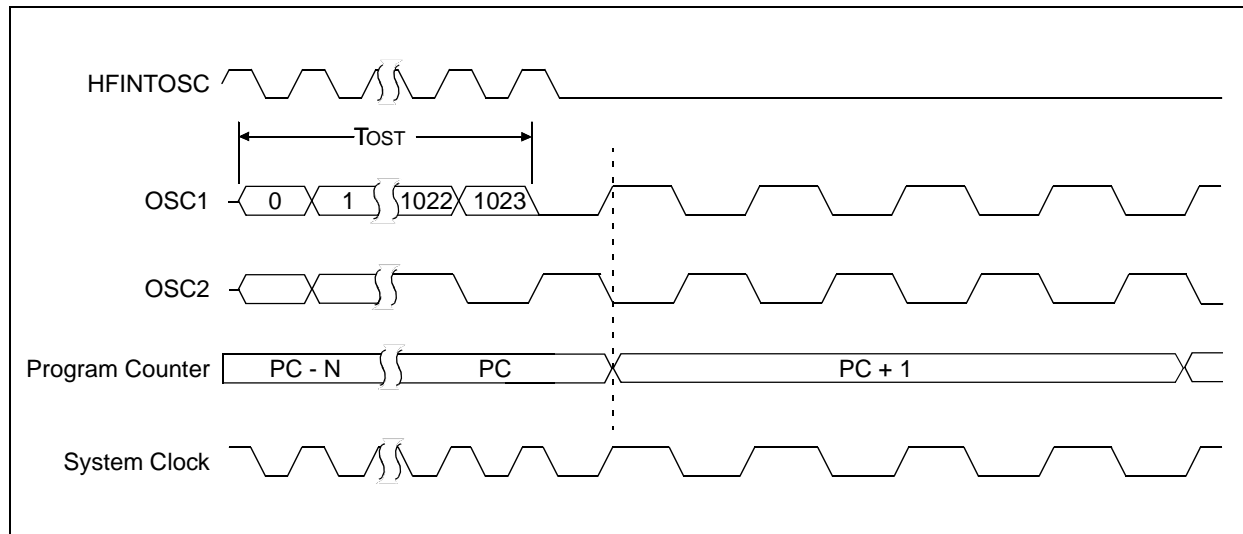


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## 3.7.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCCON register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or the internal oscillator.

**FIGURE 3-7: TWO-SPEED START-UP**



## 6.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 interrupt enable bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

**Note:** The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

## 6.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set

The device will wake-up on an overflow and execute the next instruction. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

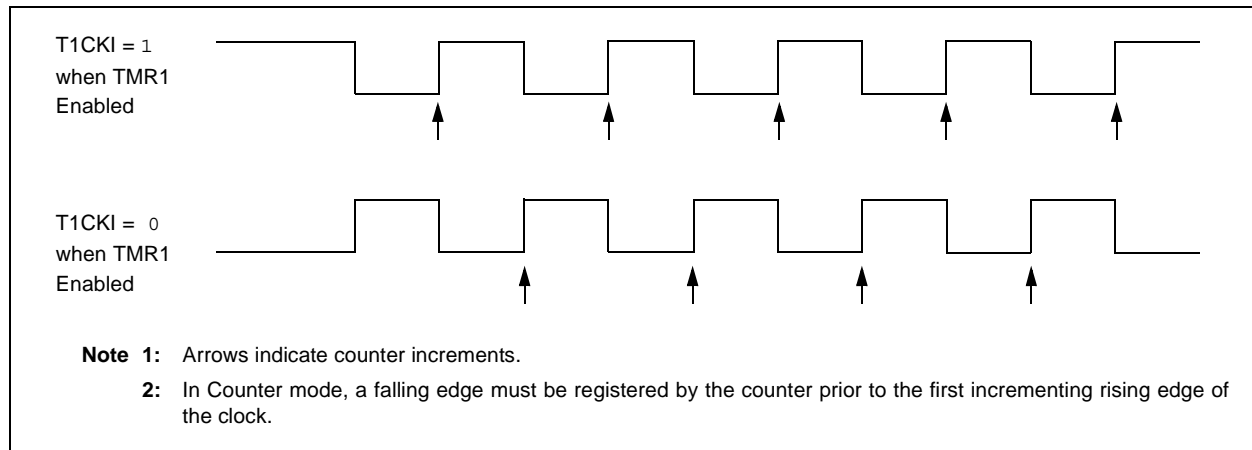
## 6.9 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see **Section 7.0 “Comparator Module”**.

**FIGURE 6-2: TIMER1 INCREMENTING EDGE**



## 7.2 Analog Input Connection Considerations

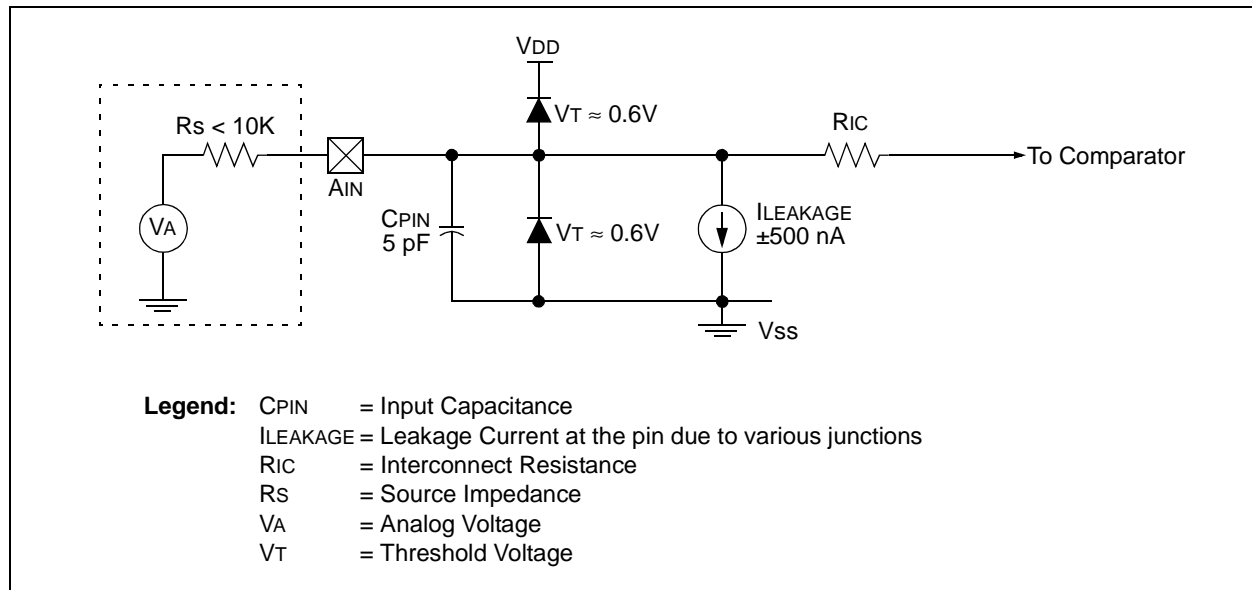
A simplified circuit for an analog input is shown in Figure 7-5. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to  $V_{DD}$  and  $V_{SS}$ . The analog input, therefore, must be between  $V_{SS}$  and  $V_{DD}$ . If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 k $\Omega$  is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

**Note 1:** When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

**2:** Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

**FIGURE 7-5: ANALOG INPUT MODEL**





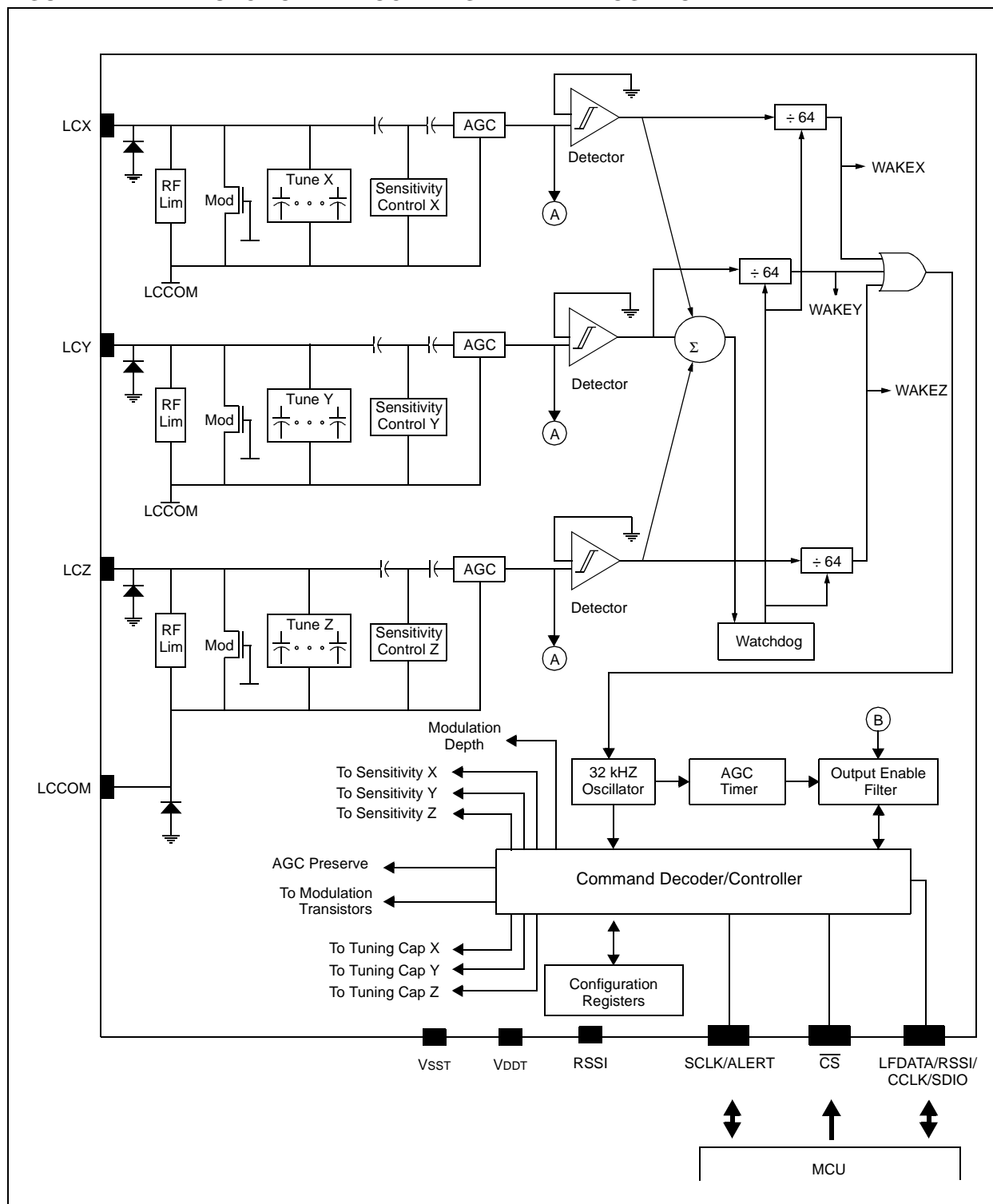
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NOTES:

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FIGURE 11-1: FUNCTIONAL BLOCK DIAGRAM – ANALOG FRONT-END



**TABLE 11-1: TYPICAL OUTPUT ENABLE FILTER TIMING**

OEH <1:0>	OEL <1:0>	TOEH (ms)	TOEL (ms)	TOET (ms)
01	00	1	1	3
01	01	1	1	3
01	10	1	2	4
01	11	1	4	6
10	00	2	1	4
10	01	2	1	4
10	10	2	2	5
10	11	2	4	8
11	00	4	1	6
11	01	4	1	6
11	10	4	2	8
11	11	4	4	10
00	xx	Filter Disabled		

**Note 1:** Typical at room temperature and VDD = 3.0V, 32 kHz oscillator.

TOEH is measured from the rising edge of the demodulator output to the first falling edge. The pulse width must fall within  $TOEH \leq t \leq TOET$ .

TOEL is measured from the falling edge of the demodulator output to the rising edge of the next pulse. The pulse width must fall within  $TOEL \leq t \leq TOET$ .

TOET is measured from rising edge to the next rising edge (i.e., the sum of TOEH and TOEL). The pulse width must be  $t \leq TOET$ . If the Configuration Register 0 (Register 11-1), OEL<8:7> is set to '00', then TOEH must not exceed TOET and TOEL must not exceed TINACT.

The filter will reset, requiring a complete new successive high and low period to enable LFDATA, under the following conditions.

- The received high is not greater than the configured minimum TOEH value.
- During TOEH, a loss of signal > 56  $\mu$ s. A loss of signal < 56  $\mu$ s may or may not cause a filter Reset.
- The received low is not greater than the configured minimum TOEL value.
- The received sequence exceeds the maximum TOET value:
  - $TOEH + TOEL > TOET$
  - or  $TOEH > TOET$
  - or  $TOEL > TOET$
- A Soft Reset SPI command is received.

If the filter resets due to a long high ( $TOEH > TOET$ ), the high-pulse timer will not begin timing again until after a gap of TE and another low-to-high transition occurs on the demodulator output.

Disabling the output enable filter disables the TOEH and TOEL requirement and the AFE passes all received LF data. See Figure 11-10, Figure 11-11 and Figure 11-12 for examples.

When viewed from an application perspective, from the pin input, the actual output enable filter timing must factor in the analog delays in the input path (such as demodulator charge and discharge times).

- $TOEH - TDR + TDF$
- $TOEL + TDR - TDF$

The output enable filter starts immediately after TGAP, the gap after AGC stabilization period.

## 11.16 Input Sensitivity Control

The AFE is designed to have typical input sensitivity of 3 mVPP. This means any input signal with amplitude greater than 3 mVPP can be detected. The AFE's internal AGC loop regulates the detecting signal amplitude when the input level is greater than approximately 20 mVPP. This signal amplitude is called "AGC-active level". The AGC loop regulates the input voltage so that the input signal amplitude range will be kept within the linear range of the detection circuits without saturation. The AGC Active Status bit AGCACT<5>, in the AFE Status Register 7 (Register 11-8) is set if the AGC loop regulates the input voltage.

Table 11-2 shows the input sensitivity comparison when the AGCSIG option is used. When AGCSIG option bit is set, the demodulated output is available only when the AGC loop is active (see Table 11-1). The AFE has also input sensitivity reduction options per each channel. The Configuration Register 3 (Register 11-4), Configuration Register 4 (Register 11-5) and Configuration Register 5 (Register 11-6) have the option to reduce the channel gains from 0 dB to approximately -30 dB.

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## 11.31.2 CARRIER CLOCK OUTPUT

When the Carrier Clock output is selected, the LFDATA output is a square pulse of the input carrier clock and available as soon as the AGC stabilization time (TAGC) is completed. There are two Configuration register options for the carrier clock output: (a) clock divide-by one or (b) clock divide-by four, depending on bit DATOUT<7> of Configuration Register 2 (Register 11-3). The carrier clock output is available immediately after the AGC settling time. The Output Enable Filter, AGCSIG, and MODMIN options are applicable for the carrier clock output in the same way as the demodulated output. The input channel can be individually enabled or disabled for the output. If more than one channel is enabled, the output is the sum of each output of all enabled channels. Therefore, the carrier clock output waveform is not as precise as when only one channel is enabled. It is recommended to enable one channel only if a precise output waveform is desired.

There will be no valid output if all three channels are disabled. See Figure 11-13 for carrier clock output examples.

### Related Configuration register bits:

- Configuration Register 1 (Register 11-2), DATOUT <8:7>:

<u>bit 8</u>	<u>bit 7</u>
0	0: Demodulator Output
0	1: Carrier Clock Output
1	0: RSSI Output
1	1: RSSI Output
- Configuration Register 2 (Register 11-3), CLKDIV<7>:

0:	Carrier Clock/1
1:	Carrier Clock/4
- Configuration Register 0 (Register 11-1): all bits are affected
- Configuration Register 5 (Register 11-6)

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## 12.3 Power-on Reset

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the POR, simply connect the  $\overline{\text{MCLR}}$  pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See **Section 15.0 “Electrical Specifications”** for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until VDD reaches VBOD (see **Section 12.6 “Brown-out Reset (BOR)”**).

**Note:** The POR circuit does not produce an internal Reset when VDD declines. To re-enable the POR, VDD must reach VSS for a minimum of 100  $\mu\text{s}$ .

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to the Application Note AN607, “Power-up Trouble Shooting” (DS00607).

## 12.4 Wake-up Reset (WUR)

The PIC12F635/PIC16F636/639 has a modified wake-up from Sleep mechanism. When waking from Sleep, the WUR function resets the device and releases Reset when VDD reaches an acceptable level.

If the  $\overline{\text{WURE}}$  bit is enabled ('0') in the Configuration Word register, the device will Wake-up Reset from Sleep through one of the following events:

1. On any event that causes a wake-up event. The peripheral must be enabled to generate an interrupt or wake-up, GIE state is ignored.
2. When WURE is enabled, RA3 will always generate an interrupt-on-change signal during Sleep.

The  $\overline{\text{WUR}}$ ,  $\overline{\text{POR}}$  and  $\overline{\text{BOR}}$  bits in the PCON register and the  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits in the STATUS register can be used to determine the cause of device Reset.

To allow WUR upon RA3 change:

1. Enable the WUR function,  $\overline{\text{WURE}}$  Configuration Bit = 0.
2. Enable RA3 as an input, MCLRE Configuration Bit = 0.
3. Read PORTA to establish the current state of RA3.
4. Execute SLEEP instruction.
5. When RA3 changes state, the device will wake-up and then reset. The  $\overline{\text{WUR}}$  bit in PCON will be cleared to '0'.

## 12.4.1 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from the 31 kHz LFINTOSC oscillator. For more information, see **Section 3.5 “Internal Clock Modes”**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A Configuration bit, PWRT $\overline{\text{E}}$ , can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip due to:

- VDD variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 15.0 “Electrical Specifications”**).

**Note:** Voltage spikes below VSS at the  $\overline{\text{MCLR}}$  pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100  $\Omega$  should be used when applying a “low” level to the  $\overline{\text{MCLR}}$  pin, rather than pulling this pin directly to VSS.

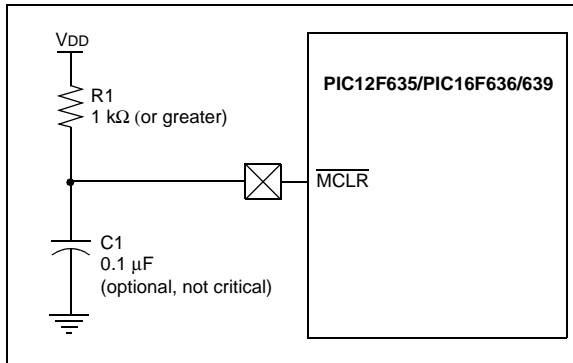
## 12.5 $\overline{\text{MCLR}}$

PIC12F635/PIC16F636/639 has a noise filter in the  $\overline{\text{MCLR}}$  Reset path. The filter will ignore small pulses.

It should be noted that a WDT Reset does not drive  $\overline{\text{MCLR}}$  pin low. See Figure 12-2 for the recommended  $\overline{\text{MCLR}}$  circuit.

An internal  $\overline{\text{MCLR}}$  option is enabled by clearing the MCLRE bit in the Configuration Word register. When cleared,  $\overline{\text{MCLR}}$  is internally tied to VDD and an internal weak pull-up is enabled for the  $\overline{\text{MCLR}}$  pin. In-Circuit Serial Programming is not affected by selecting the internal  $\overline{\text{MCLR}}$  option.

**FIGURE 12-2: RECOMMENDED  $\overline{\text{MCLR}}$  CIRCUIT**



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## 12.10 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Since the lower 16 bytes of all banks are common in the PIC12F635/PIC16F636/639 (see Figure 2-2), temporary holding registers, W\_TEMP and STATUS\_TEMP, should be placed in here. These 16 locations do not require banking and therefore, make it easier to context save and restore. The same code shown in Example 12-1 can be used to:

- Store the W register.
- Store the STATUS register.
- Execute the ISR code.
- Restore the Status (and Bank Select Bit register).
- Restore the W register.

**Note:** The PIC12F635/PIC16F636/639 normally does not require saving the PCLATH. However, if computed GOTO's are used in the ISR and the main code, the PCLATH must be saved and restored in the ISR.

### EXAMPLE 12-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF    W_TEMP          ;Copy W to TEMP register
SWAPF    STATUS,W        ;Swap status to be saved into W
                        ;Swaps are used because they do not affect the status bits
MOVWF    STATUS_TEMP     ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                ;Insert user code here
:
SWAPF    STATUS_TEMP,W   ;Swap STATUS_TEMP register into W
                        ;(sets bank to original state)
MOVWF    STATUS          ;Move W into STATUS register
SWAPF    W_TEMP,F        ;Swap W_TEMP
SWAPF    W_TEMP,W        ;Swap W_TEMP into W
```

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<b>MOVF</b>	<b>Move f</b>
Syntax:	[ <i>label</i> ] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) \rightarrow (\text{dest})$
Status Affected:	Z
Description:	The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
Example:	<pre>MOVF    FSR, 0</pre> <p>After Instruction</p> <p>W = value in FSR register Z = 1</p>

<b>MOVLW</b>	<b>Move literal to W</b>
Syntax:	[ <i>label</i> ] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k \rightarrow (W)$
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.
Words:	1
Cycles:	1
Example:	<pre>MOVLW    0x5A</pre> <p>After Instruction</p> <p>W = 0x5A</p>

<b>MOVWF</b>	<b>Move W to f</b>
Syntax:	[ <i>label</i> ] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
Example:	<pre>MOVWF    OPTION F</pre> <p>Before Instruction</p> <p>OPTION = 0xFF W = 0x4F</p> <p>After Instruction</p> <p>OPTION = 0x4F W = 0x4F</p>

<b>NOP</b>	<b>No Operation</b>
Syntax:	[ <i>label</i> ] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Words:	1
Cycles:	1
Example:	<pre>NOP</pre>



## 14.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C18 and MPLAB C30 C Compilers
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PICSTART® Plus Development Programmer
  - MPLAB PM3 Device Programmer
  - PICKit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

## 14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (assembly or C)
  - Mixed assembly and C
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

# PIC12F635/PIC16F636/639

## 15.1 DC Characteristics: PIC12F635/PIC16F636-I (Industrial) PIC12F635/PIC16F636-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001 D001A D001B D001C	VDD	Supply Voltage	2.0 2.0 3.0 4.5	— — — —	5.5 5.5 5.5 5.5	V V V V	FOSC ≤ 4 MHz FOSC ≤ 8 MHz, HFINTOSC, EC FOSC ≤ 10 MHz FOSC ≤ 20 MHz
D002	VDR	RAM Data Retention Voltage <sup>(1)</sup>	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See Section 12.3 “Power-on Reset” for details.
D004	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See Section 12.3 “Power-on Reset” for details.
D005	VBOD	Brown-out Reset	2.0	2.1	2.2	V	

\* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

# PIC12F635/PIC16F636/639

## 15.2 DC Characteristics: PIC12F635/PIC16F636-I (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Sym	Device Characteristics	Min	Typ†	Max	Units	Conditions	
							VDD	Note
D010	IDD	Supply Current <sup>(1,2)</sup>	—	11	16	μA	2.0	Fosc = 32.768 kHz LP Oscillator mode
			—	18	28	μA	3.0	
			—	35	54	μA	5.0	
D011			—	140	240	μA	2.0	Fosc = 1 MHz XT Oscillator mode
			—	220	380	μA	3.0	
			—	380	550	μA	5.0	
D012			—	260	360	μA	2.0	Fosc = 4 MHz XT Oscillator mode
			—	420	650	μA	3.0	
			—	0.8	1.1	mA	5.0	
D013			—	130	220	μA	2.0	Fosc = 1 MHz EC Oscillator mode
			—	215	360	μA	3.0	
			—	360	520	μA	5.0	
D014			—	220	340	μA	2.0	Fosc = 4 MHz EC Oscillator mode
			—	375	550	μA	3.0	
			—	0.65	1.0	mA	5.0	
D015			—	8	20	μA	2.0	Fosc = 31 kHz LFINTOSC mode
			—	16	40	μA	3.0	
			—	31	65	μA	5.0	
D016			—	340	450	μA	2.0	Fosc = 4 MHz HFINTOSC mode
			—	500	700	μA	3.0	
			—	0.8	1.2	mA	5.0	
D017			—	410	650	μA	2.0	Fosc = 8 MHz HFINTOSC mode
			—	700	950	μA	3.0	
			—	1.30	1.65	mA	5.0	
D018			—	230	400	μA	2.0	Fosc = 4 MHz EXTRC mode
			—	400	680	μA	3.0	
			—	0.63	1.1	mA	5.0	
D019			—	2.6	3.25	mA	4.5	Fosc = 20 MHz HS Oscillator mode
			—	2.6	3.25	mA	5.0	

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled. MCU only, Analog Front-End not included.
- 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. MCU only, Analog Front-End not included.
- 3:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.
- 4:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

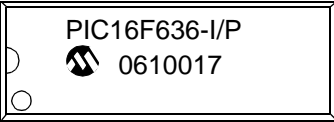
# PIC12F635/PIC16F636/639

## 17.1 Package Marking Information (Continued)

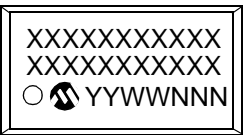
14-Lead PDIP



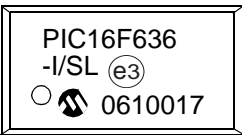
Example



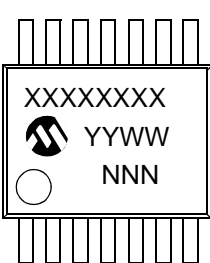
14-Lead SOIC



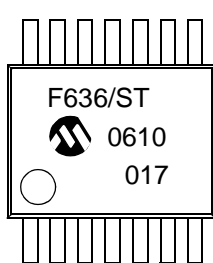
Example



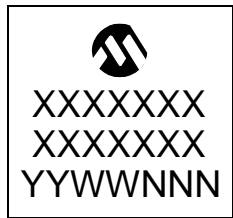
14-Lead TSSOP



Example



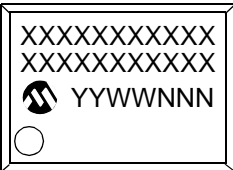
16-Lead QFN



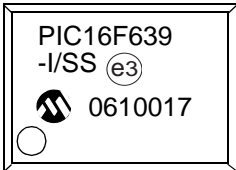
Example



20-Lead SSOP



Example



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