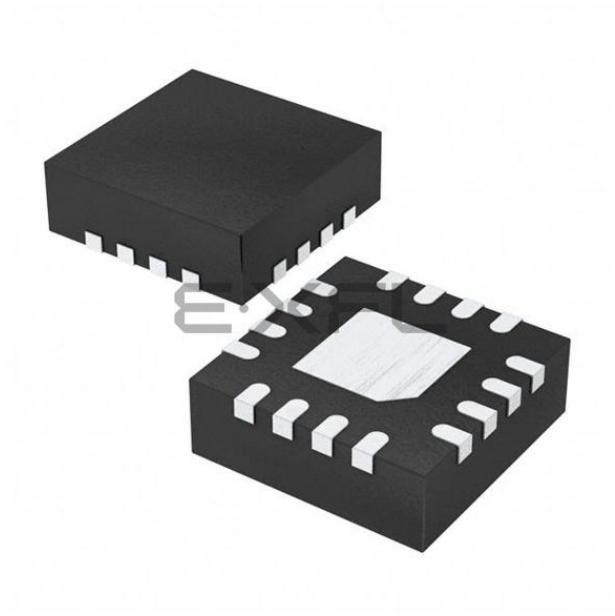

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f636-i-ml

NOTES:

TABLE 1-1: PIC12F635 PINOUT DESCRIPTIONS

Name	Function	Input Type	Output Type	Description
GP0/C1IN+/ICSPDAT/ULPWU	GP0	TTL	—	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down. Selectable Ultra Low-Power Wake-up pin.
	C1IN+	AN	—	Comparator 1 input – positive.
	ICSPDAT	TTL	CMOS	Serial programming data I/O.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
GP1/C1IN-/ICSPCLK	GP1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	C1IN-	AN	—	Comparator 1 input – negative.
	ICSPCLK	ST	—	Serial programming clock.
GP2/T0CKI/INT/C1OUT	GP2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T0CKI	ST	—	External clock for Timer0.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator 1 output.
GP3/$\overline{\text{MCLR}}$/VPP	GP3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear Reset. Pull-up enabled when configured as $\overline{\text{MCLR}}$.
	VPP	HV	—	Programming voltage.
GP4/$\overline{\text{T1G}}$/OSC2/CLKOUT	GP4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate.
	OSC2	—	XTAL	XTAL connection.
	CLKOUT	—	CMOS	TOSC/4 reference clock.
GP5/T1CKI/OSC1/CLKIN	GP5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T1CKI	ST	—	Timer1 clock.
	OSC1	XTAL	—	XTAL connection.
	CLKIN	ST	—	TOSC reference clock.
VDD	VDD	D	—	Power supply for microcontroller.
VSS	VSS	D	—	Ground reference for microcontroller.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; D = Direct
HV = High Voltage; ST = Schmitt Trigger input with CMOS levels
TTL = TTL compatible input; XTAL = Crystal

TABLE 2-4: PIC16F636/639 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR/ WUR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32,137
81h	OPTION_REG	$\overline{RAPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	63,137
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	32,137
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	26,137
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	32,137
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
86h	—	Unimplemented								—	—
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	32,137
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(3)	0000 000x	28,137
8Ch	PIE1	EEIE	LVDIE	CRIE	C2IE	C1IE	OSFIE	—	TMR1IE	0000 00-0	29,137
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	ULPWUE	SBOREN	$\overline{WUR}$	—	$\overline{POR}$	$\overline{BOR}$	--01 q-qq	--0u u-uu
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	-110 x000
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu
91h	—	Unimplemented								—	—
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -000	--00 -000
95h	WPUDA(2)	—	—	WPUDA5	WPUDA4	—	WPUDA2	WPUDA1	WPUDA0	--11 -111	--11 -111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
97h	WDA(2)	—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0	--11 -111	--11 -111
9Bh	—	Unimplemented								—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
9Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----
9Eh	—	Unimplemented								—	—
9Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: RA3 pull-up is enabled when pin is configured as $\overline{MCLR}$ in the Configuration Word register.

3: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset but will set again if the mismatch exists.

3.5.2.1 OSCTUNE Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-2).

The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

REGISTER 3-2: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

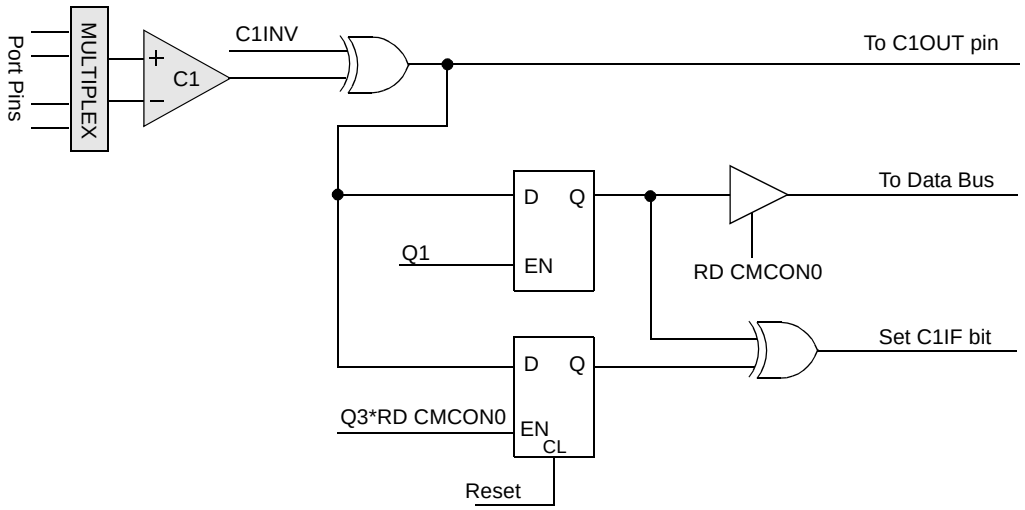
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Oscillator module is running at the calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

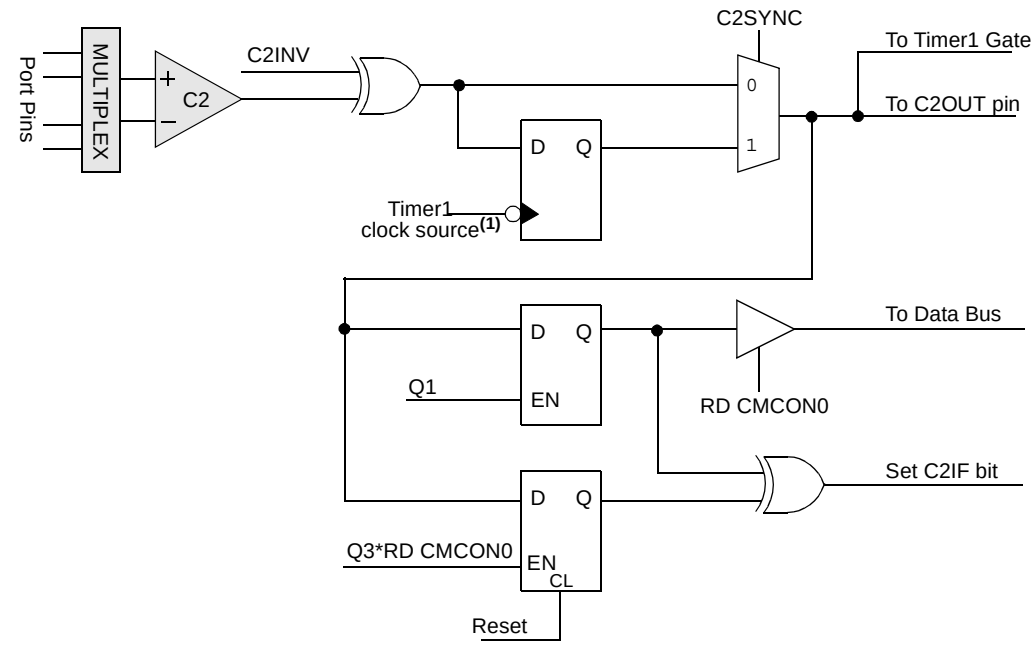
FIGURE 7-3: COMPARATOR C1 OUTPUT BLOCK DIAGRAM (PIC16F636/639)



Note 1: Q1 and Q3 are phases of the four-phase system clock (FOSC).

2: Q1 is held high during Sleep mode.

FIGURE 7-4: COMPARATOR C2 OUTPUT BLOCK DIAGRAM (PIC16F636/639)



Note 1: Comparator output is latched on falling edge of Timer1 clock source.

2: Q1 and Q3 are phases of the four-phase system clock (FOSC).

3: Q1 is held high during Sleep mode.

7.11 Comparator Voltage Reference

The Comparator Voltage Reference module provides an internally generated voltage reference for the comparators. The following features are available:

- Independent from Comparator operation
- Two 16-level voltage ranges
- Output clamped to VSS
- Ratiometric with VDD
- Fixed Voltage Reference

The VRCON register (Register 7-5) controls the Voltage Reference module shown in Figure 7-10.

7.11.1 INDEPENDENT OPERATION

The comparator voltage reference is independent of the comparator configuration. Setting the VREN bit of the VRCON register will enable the voltage reference.

7.11.2 OUTPUT VOLTAGE SELECTION

The CVREF voltage reference has 2 ranges with 16 voltage levels in each range. Range selection is controlled by the VRR bit of the VRCON register. The 16 levels are set with the VR<3:0> bits of the VRCON register.

The CVREF output voltage is determined by the following equations:

EQUATION 7-1: CVREF OUTPUT VOLTAGE (INTERNAL CVREF)

$$VRR = 1 \text{ (low range):}$$
$$CVREF = (VR<3:0>/24) \times VDD$$
$$VRR = 0 \text{ (high range):}$$
$$CVREF = (VDD/4) + (VR<3:0> \times VDD/32)$$

EQUATION 7-2: CVREF OUTPUT VOLTAGE (EXTERNAL CVREF)

$$VRR = 1 \text{ (low range):}$$
$$CVREF = (VR<3:0>/24) \times VLADDER$$
$$VRR = 0 \text{ (high range):}$$
$$CVREF = (VLADDER/4) + (VR<3:0> \times VLADDER/32)$$
$$VLADDER = VDD \text{ or } ([VREF+] - [VREF-]) \text{ or } VREF+$$

The full range of VSS to VDD cannot be realized due to the construction of the module. See Figure 7-10.

7.11.3 OUTPUT CLAMPED TO VSS

The CVREF output voltage can be set to Vss with no power consumption by configuring VRCON as follows:

- VREN = 0
- VRR = 1
- VR<3:0> = 0000

This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.

7.11.4 OUTPUT RATIOMETRIC TO VDD

The comparator voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 15.0 "Electrical Specifications"**.

TABLE 7-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CMCON0	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	---- --10
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIE1	EEIE	LVDIE	CRIE	—	C1IE	OSFIE	—	TMR1IE	000- 00-0	000- 00-0
PIR1	EEIF	LVDIF	CRIF	—	C1IF	OSFIF	—	TMR1IF	000- 00-0	000- 00-0
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for comparator.

NOTES:

11.20 Soft Reset

The AFE issues a Soft Reset in the following events:

a) After Power-on Reset (POR),
b) After Inactivity timer time-out,
c) If an “Abort” occurs,
d) After receiving SPI Soft Reset command.

The “Abort” occurs if there is no positive signal detected at the end of the AGC stabilization period (TAGC). The Soft Reset initializes internal circuits and brings the AFE into a low current Standby mode operation. The internal circuits that are initialized by the Soft Reset include:

- Output Enable Filter
- AGC circuits
- Demodulator
- 32 kHz Internal Oscillator

The Soft Reset has no effect on the Configuration register setup, except for some of the AFE Status Register 7 bits. (Register 11-8).

The circuit initialization takes one internal clock cycle (1/32 kHz = 31.25 μs). During the initialization, the modulation transistors between each input and LCCOM pins are turned-on to discharge any internal/external parasitic charges. The modulation transistors are turned-off immediately after the initialization time.

The Soft Reset is executed in Active mode only. It is not valid in Standby mode.

11.21 Minimum Modulation Depth Requirement for Input Signal

The AFE demodulates the modulated input signal if the modulation depth of the input signal is greater than the minimum requirement that is programmed in the AFE Configuration Register 5 (Register 11-6). Figure 11-7 shows the definition of the modulation depth and examples. MODMIN<6:5> of the Configuration Register 5 offer four options. They are 75%, 50%, 25% and 12%, with a default setting of 50%.

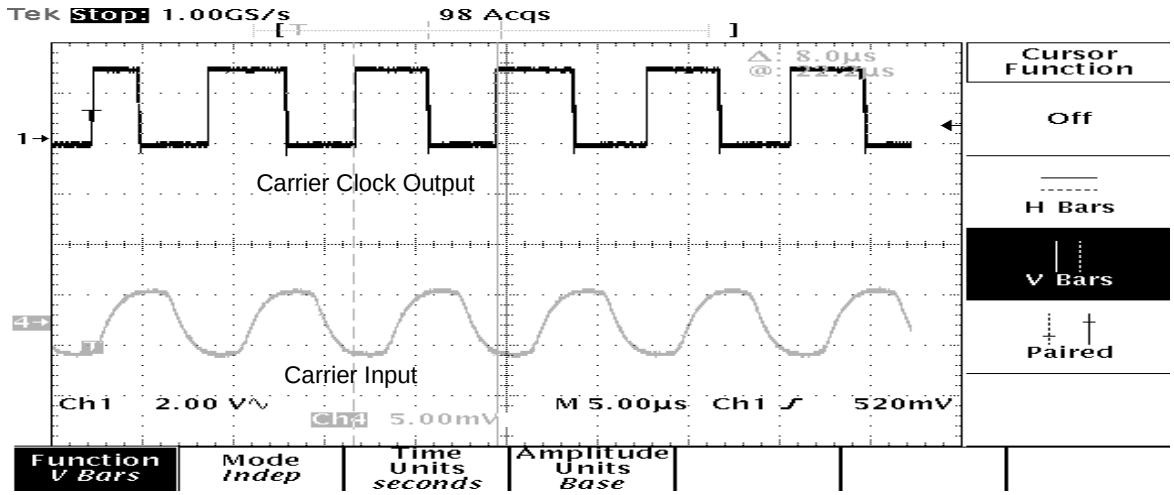
The purpose of this feature is to enhance the demodulation integrity of the input signal. The 12% setting is the best choice for the input signal with weak modulation depth, which is typically observed near the high-voltage base station antenna and also at far-distance from the base station antenna. It gives the best demodulation sensitivity, but is very susceptible to noise spikes that can result in a bit detection error. The 75% setting can reduce the bit errors caused by noise, but gives the least demodulation sensitivity. See Table 11-3 for minimum modulation depth requirement settings.

TABLE 11-3: SETTING FOR MINIMUM MODULATION DEPTH REQUIREMENT

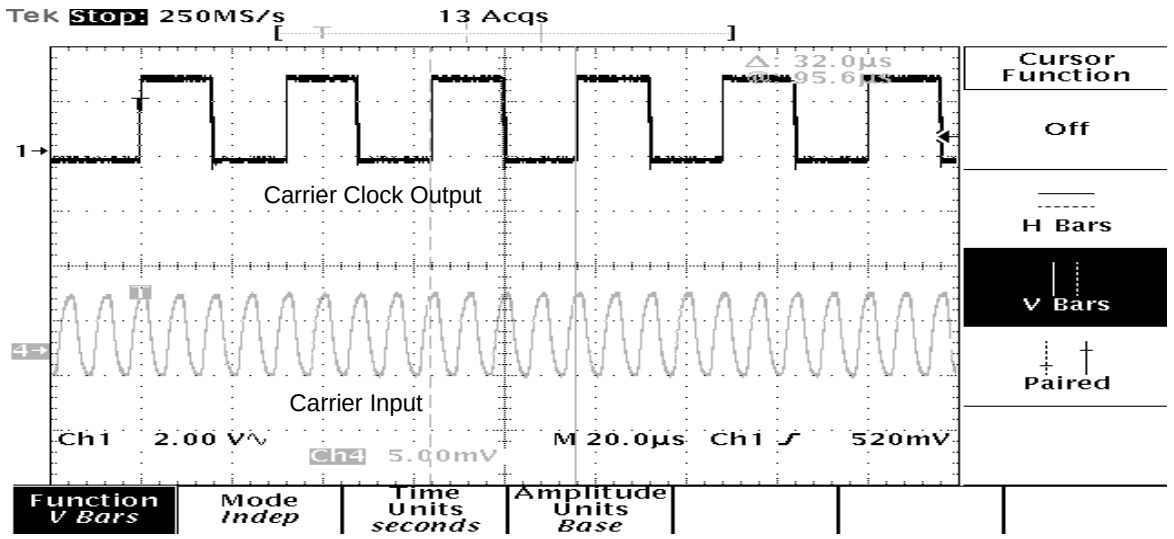
MODMIN Bits (Config. Register 5)		Modulation Depth
Bit 6	Bit 5	
0	0	50% (default)
0	1	75%
1	0	25%
1	1	12%

FIGURE 11-13: CARRIER CLOCK OUTPUT EXAMPLES

(A) CARRIER CLOCK OUTPUT WITH CARRIER/1 OPTION



(B) CARRIER CLOCK OUTPUT WITH CARRIER/4 OPTION



12.0 SPECIAL FEATURES OF THE CPU

The PIC12F635/PIC16F636/639 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset
  - Power-on Reset (POR)
  - Wake-up Reset (WUR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator selection
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming™

The PIC12F635/PIC16F636/639 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a nominal 64 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer Wake-up
- An Interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options (see Register 12-1).

12.1 Configuration Bits

The Configuration Word bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 12-1. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See *"*PIC12F6XX/16F6XX *Memory Programming Specification"* (DS41204) for more information.

12.2 Reset

The PIC12F635/PIC16F636/639 differentiates between various kinds of Reset:

a) Power-on Reset (POR)
b) Wake-up Reset (WUR)
c) WDT Reset during normal operation
d) WDT Reset during Sleep
e) $\overline{\text{MCLR}}$ Reset during normal operation
f) $\overline{\text{MCLR}}$ Reset during Sleep
g) Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

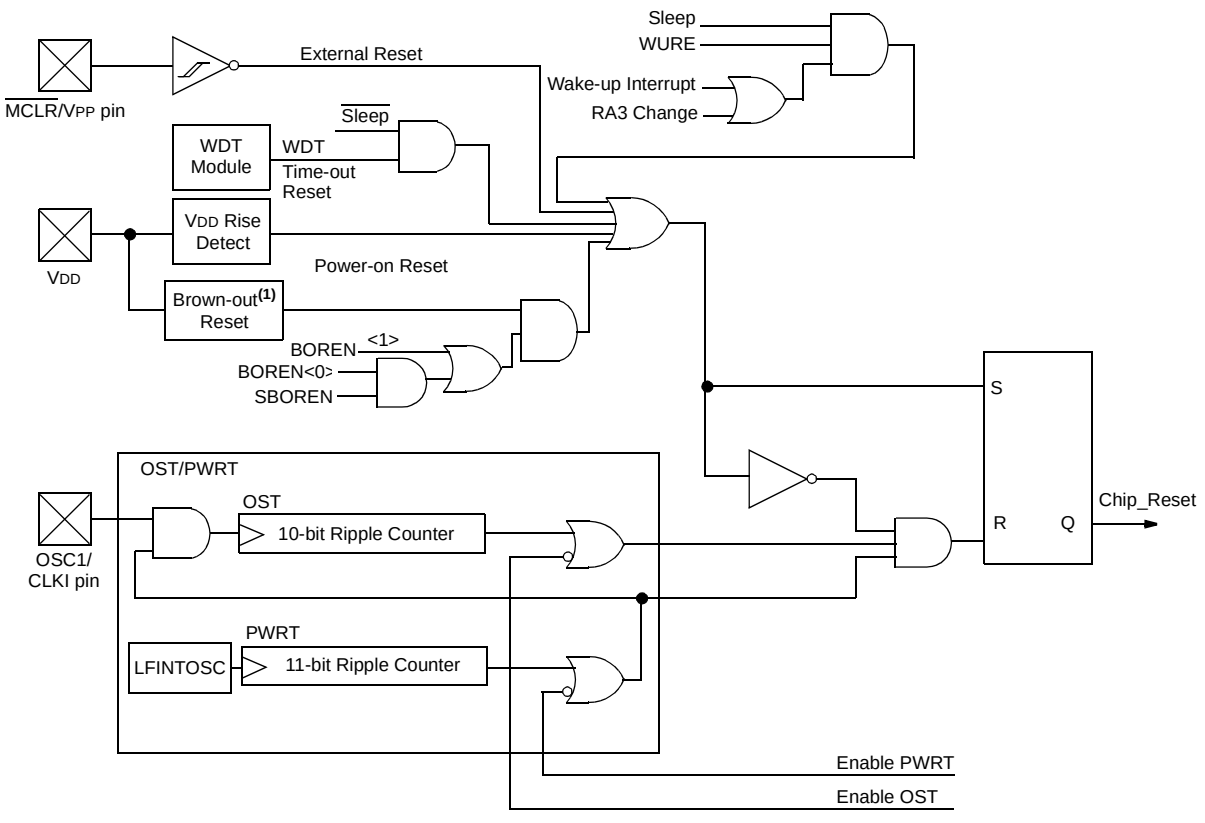
- Power-on Reset
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset

They are not affected by a WDT wake-up since this is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 12-3. These bits are used in software to determine the nature of the Reset. See Table 12-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 12-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 15.0 "Electrical Specifications"** for pulse width specifications.

FIGURE 12-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: Refer to the Configuration Word register (Register 12-1).

15.6 DC Characteristics: PIC16F639-I (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial Supply Voltage 2.0V ≤ VDD ≤ 3.6V					
Param No.	Sym	Device Characteristics	Min	Typ†	Max	Units	Conditions	
							VDD	Note
D010	IDD	**Supply Current(1,2,3)**	—	11	16	µA	2.0	FOSC = 32.768 kHz LP Oscillator mode
			—	18	28	µA	3.0	
D011			—	140	240	µA	2.0	FOSC = 1 MHz XT Oscillator mode
			—	220	380	µA	3.0	
D012			—	260	360	µA	2.0	FOSC = 4 MHz XT Oscillator mode
			—	420	650	µA	3.0	
D013			—	130	220	µA	2.0	FOSC = 1 MHz EC Oscillator mode
			—	215	360	µA	3.0	
D014			—	220	340	µA	2.0	FOSC = 4 MHz EC Oscillator mode
			—	375	550	µA	3.0	
D015			—	8	20	µA	2.0	FOSC = 31 kHz LFINTOSC mode
			—	16	40	µA	3.0	
D016			—	340	450	µA	2.0	FOSC = 4 MHz HFINTOSC mode
			—	500	700	µA	3.0	
D017			—	230	400	µA	2.0	FOSC = 4 MHz EXTRC mode
			—	400	680	µA	3.0	
D020	IPD	**Power-down Base Current(4)**	—	0.15	1.2	µA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled (excludes AFE)
			—	0.20	1.5	µA	3.0	
D021	IWDT		—	1.2	2.2	µA	2.0	WDT Current(1)
			—	2.0	4.0	µA	3.0	
D022A	IBOR		—	42	60	µA	3.0	BOR Current(1)
D022B	ILVD		—	22	28	µA	2.0	PLVD Current
			—	25	35	µA	3.0	
D023	ICMP		—	32	45	µA	2.0	Comparator Current(1)
			—	60	78	µA	3.0	
D024A	IVREFHS		—	30	36	µA	2.0	CVREF Current(1) (high-range)
			—	45	55	µA	3.0	
D024B	IVREFLS		—	39	47	µA	2.0	CVREF Current(1) (low-range)
			—	59	72	µA	3.0	
D025	IT1OSC		—	4.5	7.0	µA	2.0	T1OSC Current(1)
			—	5.0	8.0	µA	3.0	
D026	IACT	**Active Current** of AFE only (receiving signal) 1 LC Input Channel Signal 3 LC Input Channel Signals	 — —	 10 13	 — 18	 µA µA	 3.6 3.6	$\overline{CS}$ = VDD; Input = Continuous Wave (CW); Amplitude = 300 mVPP. All channels enabled.
D027	ISTDBY	**Standby Current** of AFE only (not receiving signal) 1 LC Input Channel Enabled 2 LC Input Channels Enabled 3 LC Input Channels Enabled	 — — —	 3 4 5	 5 6 7	 µA µA µA	 3.6 3.6 3.6	$\overline{CS}$ = VDD; $\overline{ALERT}$ = VDD
D028	ISLEEP	**Sleep Current** of AFE only	—	0.2	1	µA	3.6	$\overline{CS}$ = VDD; $\overline{ALERT}$ = VDD

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled. MCU only, Analog Front-End not included.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. MCU only, Analog Front-End not included.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

TABLE 15-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym**	**Characteristic**	**Freq Tolerance**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
OS06	TWARM	Internal Oscillator Switch when running(3)	—	—	—	2	TOSC	Slowest clock
OS07	TSC	Fail-Safe Sample Clock Period(1)	—	—	21	—	ms	LFINTOSC/64
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(2)	±1%	7.92	8.0	8.08	MHz	VDD = 3.5V, 25°C
			±2%	7.84	8.0	8.16	MHz	2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C
			±5%	7.60	8.0	8.40	MHz	2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.)
OS09*	LFOSC	Internal Uncalibrated LFINTOSC Frequency	—	15	31	45	kHz	
OS10*	TIOSCST	HFINTOSC Oscillator Wake-up from Sleep Start-up Time	—	5.5	12	24	µs	VDD = 2.0V, -40°C to +85°C
			—	3.5	7	14	µs	VDD = 3.0V, -40°C to +85°C
			—	3	6	11	µs	VDD = 5.0V, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

3: By design.

TABLE 15-6: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym**	**Characteristics**		**Min**	**Typ†**	**Max**	**Units**	**Comments**
CM01	VOS	Input Offset Voltage		—	± 5.0	± 10	mV	(VDD - 1.5)/2
CM02	VCM	Input Common Mode Voltage		0	—	VDD – 1.5	V	
CM03*	CMRR	Common Mode Rejection Ratio		+55	—	—	dB	
CM04*	TRT	Response Time	Falling	—	150	600	ns	**(NOTE 1)**
			Rising	—	200	1000	ns	
CM05*	TMC2COV	Comparator Mode Change to Output Valid		—	—	10	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Response time is measured with one comparator input at (VDD - 1.5)/2 - 100 mV to (VDD - 1.5)/2 + 20 mV.

TABLE 15-7: COMPARATOR VOLTAGE REFERENCE (CVREF) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ†**	**Max**	**Units**	**Comments**
CV01*	CLSB	Step Size(2)	— —	VDD/24 VDD/32	— —	V V	Low Range (VRR = 1) High Range (VRR = 0)
CV02*	CACC	Absolute Accuracy	— —	— —	± 1/2 ± 1/2	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV03*	CR	Unit Resistor Value (R)	—	2k	—	Ω	
CV04*	CST	Settling Time(1)	—	—	10	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

2: See **Section 7.11 "Comparator Voltage Reference"** for more information.

TABLE 15-8: PIC12F635/PIC16F636 PLVD CHARACTERISTICS:

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating Temperature -40°C ≤ TA ≤ +125°C Operating Voltage VDD Range 2.0V-5.5V				
Sym.	**Characteristic**		**Min**	**Typ†**	**Max**	**Units**	**Conditions**
VPLVD	PLVD Voltage	LVDL<2:0> = 001	1.900	2.0	2.125	V	
		LVDL<2:0> = 010	2.000	2.1	2.225	V	
		LVDL<2:0> = 011	2.100	2.2	2.325	V	
		LVDL<2:0> = 100	2.200	2.3	2.425	V	
		LVDL<2:0> = 101	3.825	4.0	4.200	V	
		LVDL<2:0> = 110	4.025	4.2	4.400	V	
		LVDL<2:0> = 111	4.325	4.5	4.700	V	
*TPLVDS	PLVD Settling time		—	50 25	—	µs	VDD = 5.0V VDD = 3.0V

* These parameters are characterized but not tested

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

15.11 AC Characteristics: Analog Front-End for PIC16F639 (Industrial)

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Supply Voltage 2.0V ≤ VDD ≤ 3.6V Operating temperature -40°C ≤ TAMB ≤ +85°C for industrial LC Signal Input Sinusoidal 300 mVPP Carrier Frequency 125 kHz LCCOM connected to VSS				
Param No.	**Sym.**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
AF01	VSENSE	LC Input Sensitivity	1	3.0	6	mVPP	VDD = 3.0V Output enable filter disabled AGCSIG = 0; MODMIN = 00 (33% modulation depth setting) Input = Continuous Wave (CW) Output = Logic level transition from low-to-high at sensitivity level for CW input.
AF02	VDE_Q	Coil de-Q'ing Voltage - RF Limiter (RFLM) must be active	3	—	5	V	VDD = 3.0V, Force IIN = 5 µA
AF03	RFLM	RF Limiter Turn-on Resistance (LCX, LCY, LCZ)	—	300	700	Ohm	VDD = 2.0V, VIN = 8 VDC
AF04	SADJ	Sensitivity Reduction	— —	0 -30	— —	dB dB	VDD = 3.0V No sensitivity reduction selected Max reduction selected Monotonic increment in attenuation value from setting = 0000 to 1111 by design
AF05	VIN_MOD	Minimum Modulation Depth 75% ± 12% 50% ± 12% 25% ± 12% 12% ± 12%	 63 38 13 0	 75 50 25 12	 87 62 37 24	 % % % %	VDD = 3.0V
AF06	CTUNX	LCX Tuning Capacitor	— 44	0 63	— 82	pF pF	VDD = 3.0V, Config. Reg. 1, bits <6:1> Setting = 000000 63 pF +/- 30% Config. Reg. 1, bits <6:1> Setting = 111111 63 steps, 1 pF/step Monotonic increment in capacitor value from setting = 000000 to 111111 by design
AF07	CTUNY	LCY Tuning Capacitor	— 44	0 63	— 82	pF pF	VDD = 3.0V, Config. Reg. 2, bits <6:1> Setting = 000000 63 pF +/- 30% Config. Reg. 2, bits <6:1> Setting = 111111 63 steps, 1 pF/step Monotonic increment in capacitor value from setting = 000000 to 111111 by design
AF08	CTUNZ	LCZ Tuning Capacitor	— 44	0 63	— 82	pF pF	VDD = 3.0V, Config. Reg. 3, bits<6:1> Setting = 000000 63 pF +/- 30% Config. Reg. 3, bits<6:1> Setting = 111111 63 steps, 1 pF/step Monotonic increment in capacitor value from setting = 000000 to 111111 by design
AF09	FCARRIER	Carrier frequency	—	125	—	kHz	Characterized at bench.
AF10	FMOD	Input modulation frequency	—	—	10	kHz	Input data rate, characterized at bench.
AF11	C_Q	Q of Trimming Capacitors	50*	—	—	pF	Characterized at bench test
AF12	TDR	Demodulator Charge Time (delay time of demodulated output to rise)	—	50	—	µs	VDD = 3.0V MOD depth setting = 50% Input conditions: Amplitude = 300 mVPP Modulation depth = 80%
AF13	TDF	Demodulator Discharge Time (delay time of demodulated output to fall)	—	50	—	µs	VDD = 3.0V MOD depth setting = 50% Input conditions: Amplitude = 300 mVPP Modulation depth = 80%

***** Parameter is characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

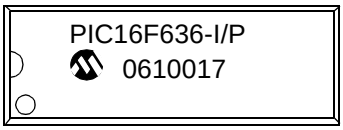
Note 1: Required output enable filter high time must account for input path analog delays (= **TOEH** - TDR + TDF).

2: Required output enable filter low time must account for input path analog delays (= **TOEL** + TDR - TDF).

17.1 Package Marking Information (Continued)

14-Lead PDIP

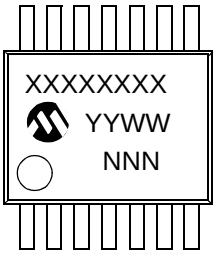
Example



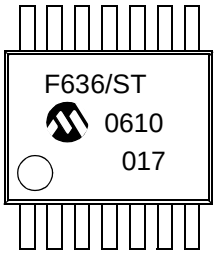
14-Lead SOIC

Example

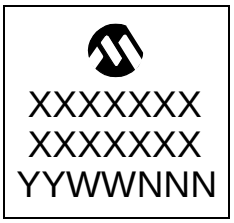
14-Lead TSSOP



Example

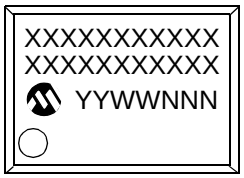


16-Lead QFN

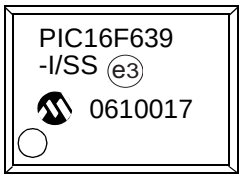


Example

20-Lead SSOP



Example

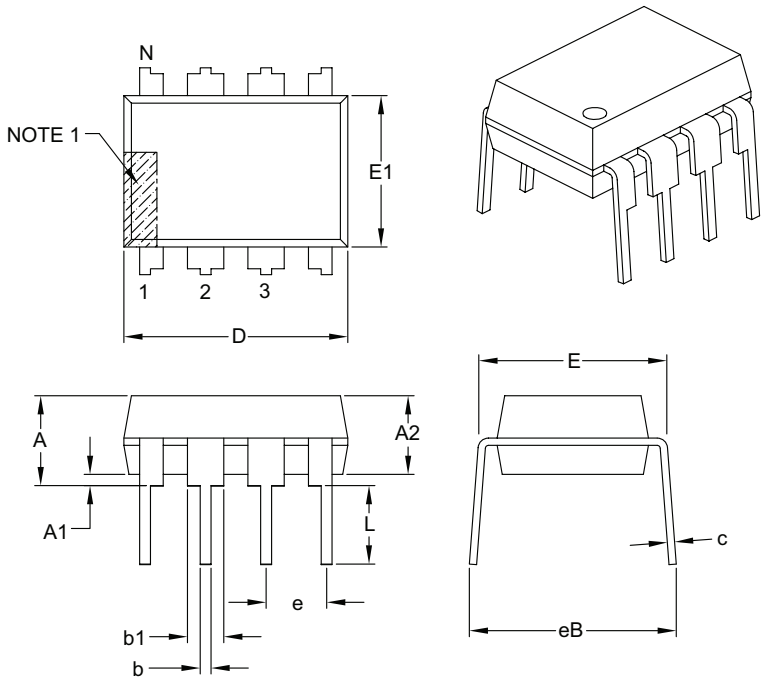


17.2 Package Details

The following sections give the technical details of the packages.

8-Lead Plastic Dual In-Line (P or PA) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

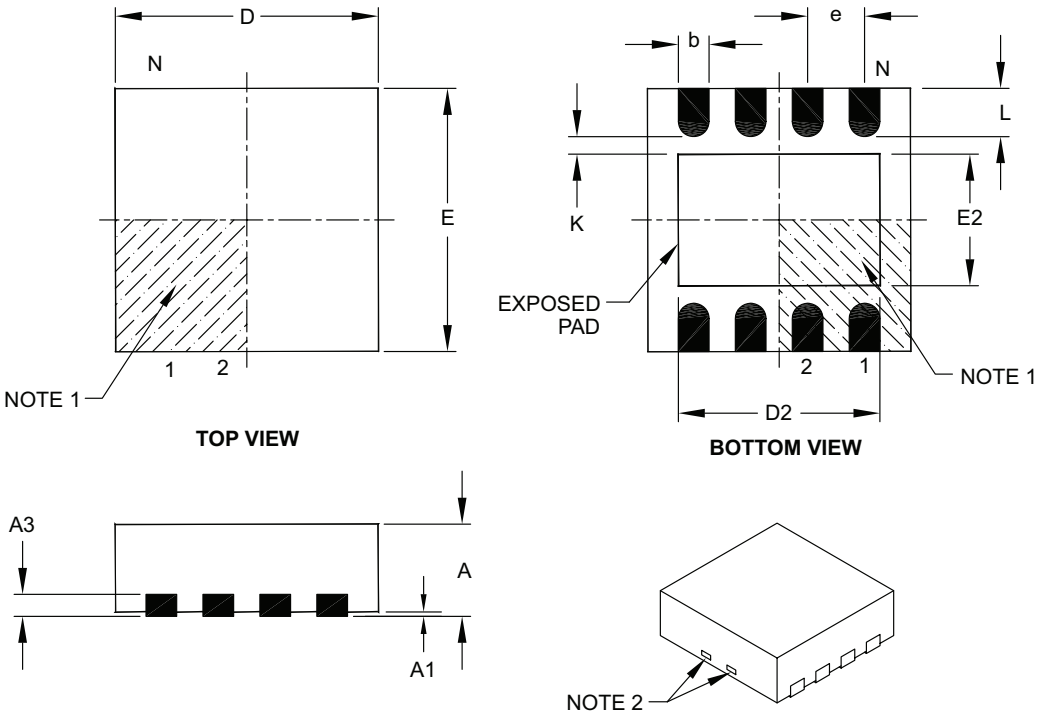
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.80 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Width	E2	0.00	2.20	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Length	D2	0.00	3.00	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.55	0.65
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

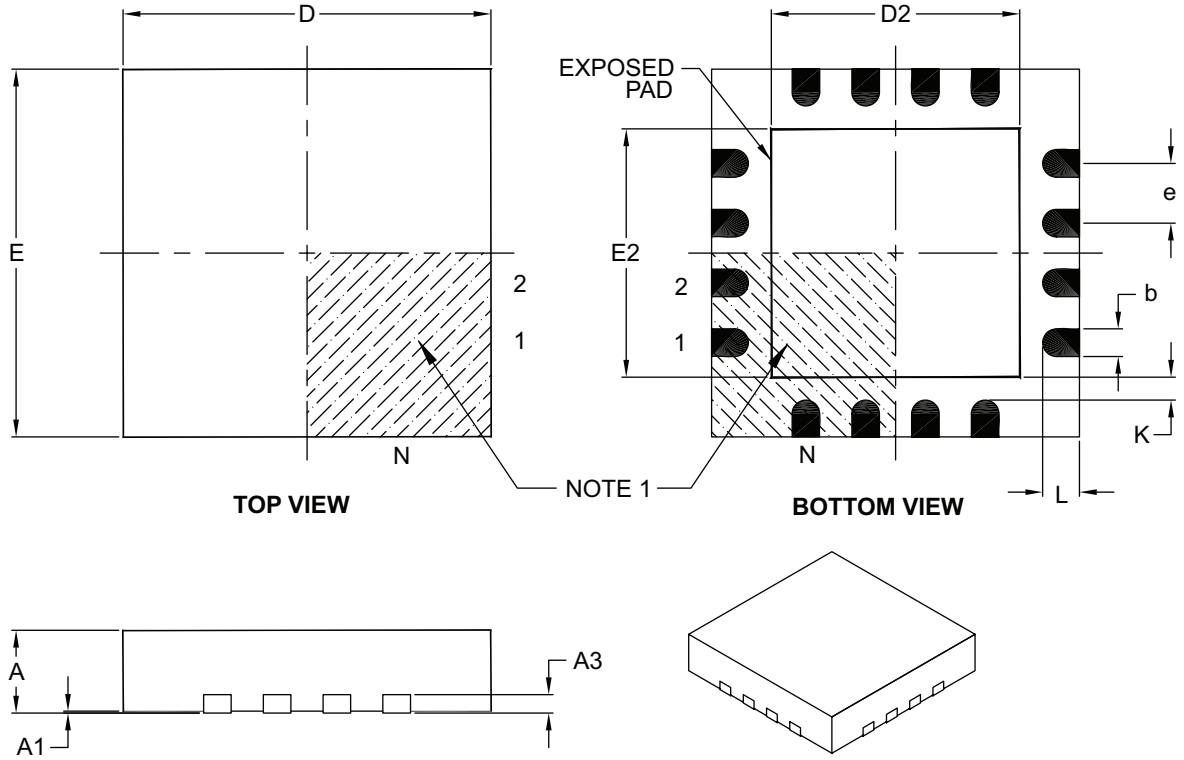
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131C

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B