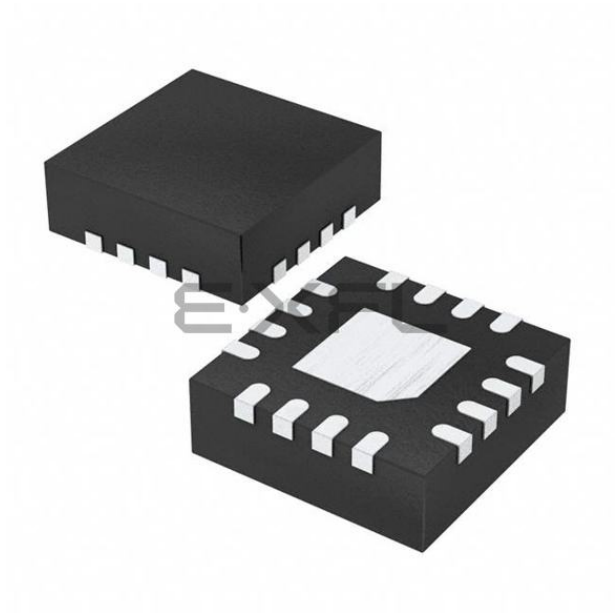

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f636t-i-ml

PIC12F635/PIC16F636/639

8/14-Pin Flash-Based, 8-Bit CMOS Microcontrollers With nanoWatt Technology

High-Performance RISC CPU:

- Only 35 instructions to learn:
  - All single-cycle instructions except branches
- Operating speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range of 8 MHz to 125 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - Crystal fail detect for critical applications
  - Clock mode switching during operation for power savings
- Clock mode switching for low-power operation
- Power-Saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and Extended Temperature range
- Power-on Reset (POR)
- Wake-up Reset (WUR)
- Independent weak pull-up/pull-down resistors
- Programmable Low-Voltage Detect (PLVD)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection (program and data independent)
- High-Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM Retention: > 40 years

Low-Power Features:

- Standby Current:
  - 1 nA @ 2.0V, typical
- Operating Current:
  - 8.5 μA @ 32 kHz, 2.0V, typical
  - 100 μA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical

Peripheral Features:

- 6/12 I/O pins with individual direction control:
  - High-current source/sink for direct LED drive
  - Interrupt-on-change pin
  - Individually programmable weak pull-ups/ pull-downs
  - Ultra Low-Power Wake-up
- Analog Comparator module with:
  - Up to two analog comparators
  - Programmable On-chip Voltage Reference (CV_{REF}) module (% of V_{DD})
  - Comparator inputs and outputs externally accessible
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Timer1 Gate (count enable)
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
- KEELOQ® compatible hardware Cryptographic module
- In-Circuit Serial Programming™ (ICSP™) via two pins

Low-Frequency Analog Front-End Features (PIC16F639 only):

- Three input pins for 125 kHz LF input signals
- High input detection sensitivity (3 mV_{PP}, typical)
- Demodulated data, Carrier clock or RSSI output selection
- Input carrier frequency: 125 kHz, typical
- Input modulation frequency: 4 kHz, maximum
- 8 internal Configuration registers
- Bidirectional transponder communication (LF talk back)
- Programmable antenna tuning capacitance (up to 63 pF, 1 pF/step)
- Low standby current: 5 μA (with 3 channels enabled), typical
- Low operating current: 15 μA (with 3 channels enabled), typical
- Serial Peripheral Interface (SPI) with internal MCU and external devices
- Supports Battery Back-up mode and batteryless operation with external circuits

FIGURE 1-2: PIC16F636 BLOCK DIAGRAM

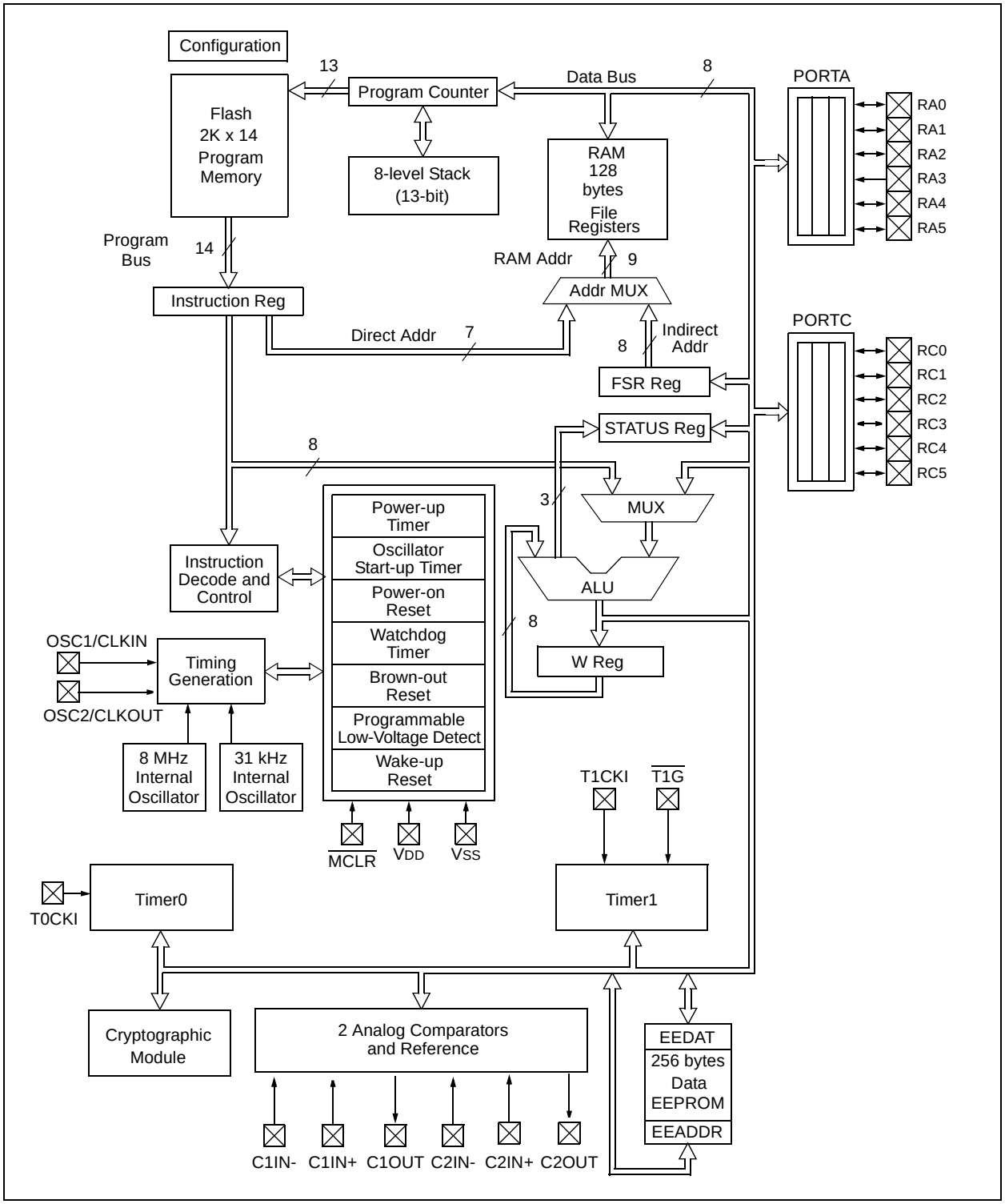


TABLE 2-2: PIC12F635 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR/ WUR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32,137
81h	OPTION_REG	$\overline{RAPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	63,137
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	32,137
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	26,137
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	32,137
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	32,137
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(3)	0000 000x	28,137
8Ch	PIE1	EEIE	LVDIE	CRIE	—	C1IE	OSFIE	—	TMR1IE	000- 00-0	29,137
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	ULPWUE	SBOREN	$\overline{WUR}$	—	$\overline{POR}$	$\overline{BOR}$	--01 q-qq	31,137
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	36,137
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	40,137
91h	—	Unimplemented								—	—
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -000	--00 -000
95h	WPUDA(2)	—	—	WPUDA5	WPUDA4	—	WPUDA2	WPUDA1	WPUDA0	--11 -111	--11 -111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
97h	WDA(2)	—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0	--11 -111	--11 -111
9Bh	—	Unimplemented								—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
9Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----
9Eh	—	Unimplemented								—	—
9Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

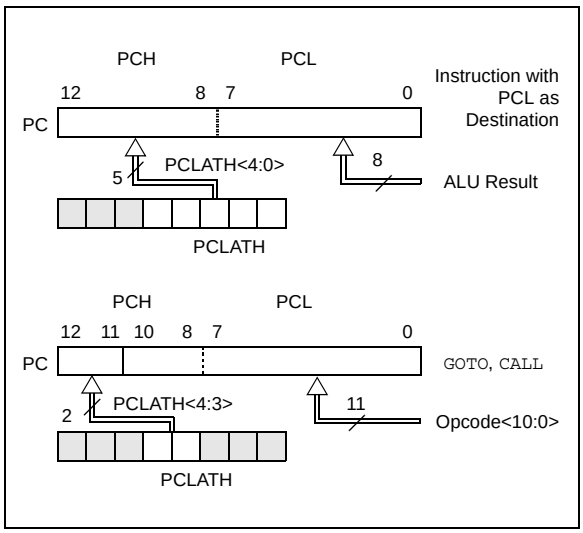
2: GP3 pull-up is enabled when pin is configured as $\overline{MCLR}$ in the Configuration Word register.

3: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset, but will set again if the mismatch exists.

2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-5 shows the two situations for the loading of the PC. The upper example in Figure 2-5 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-5 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-5: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper 5 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). Care should be exercised when jumping into a look-up table or program branch table (computed GOTO) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, "*Implementing a Table Read*" (DS00556).

2.3.2 STACK

The PIC12F635/PIC16F636/639 family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1:	There are no Status bits to indicate stack overflow or stack underflow conditions.
2:	There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit of the STATUS register, as shown in Figure 2-6.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
            MOVLW   0x20    ;initialize pointer
            MOVWF   FSR     ;to RAM
NEXT        CLRF    INDF    ;clear INDF register
            INCF    FSR     ;INC POINTER
            BTFSS   FSR,4   ;all done?
            GOTO    NEXT    ;no clear next
CONTINUE                    ;yes continue
```

NOTES:

REGISTER 8-1: LVDCON: LOW-VOLTAGE DETECT CONTROL REGISTER

U-0	U-0	R-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	—	IRVST(1)	LVDEN	—	LVDL2	LVDL1	LVDL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **IRVST:** Internal Reference Voltage Stable Status Flag bit(1)
1 = Indicates that the PLVD is stable and PLVD interrupt is reliable
0 = Indicates that the PLVD is not stable and PLVD interrupt must not be enabled

bit 4 **LVDEN:** Low-Voltage Detect Module Enable bit
1 = Enables PLVD Module, powers up PLVD circuit and supporting reference circuitry
0 = Disables PLVD Module, powers down PLVD circuit and supporting reference circuitry

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **LVDL<2:0>:** Low-Voltage Detection Level bits (nominal values)
111 = 4.5V
110 = 4.2V
101 = 4.0V
100 = 2.3V (default)
011 = 2.2V
010 = 2.1V
001 = 2.0V(2)
000 = Reserved

Note 1: The IRVST bit is usable only when the HFINTOSC is running.
2: Not tested and below minimum operating conditions.

TABLE 8-1: REGISTERS ASSOCIATED WITH PROGRAMMABLE LOW-VOLTAGE DETECT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIE1	OSFIE	C2IE	C1IE	LCDIE	—	LVDIE	—	CCP2IE	0000 -0-0	0000 -0-0
PIR1	OSFIF	C2IF	C1IF	LCDIF	—	LVDIF	—	CCP2IF	0000 -0-0	0000 -0-0
LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -100	--00 -100

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used by the PLVD module.

NOTES:

9.1 EECON1 AND EECON2 Registers

EECON1 is the control register with four low-order bits physically implemented. The upper four bits are non-implemented and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a $\overline{\text{MCLR}}$ Reset, or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit, clear it and rewrite the location. The data and address will be cleared. Therefore, the EEDAT and EEADR registers will need to be re-initialized.

Interrupt flag, EEIF bit of the PIR1 register, is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence.

Note:	The EECON1, EEDAT and EEADR registers should not be modified during a data EEPROM write (WR bit = 1).

REGISTER 9-3: EECON1: EEPROM CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD
bit 7							bit 0

Legend:			
S = Bit can only be set			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **WRERR:** EEPROM Error Flag bit
- 1 = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ Reset, any WDT Reset during normal operation or BOR Reset)
- 0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit
- 1 = Allows write cycles
- 0 = Inhibits write to the data EEPROM

bit 1 **WR:** Write Control bit
- 1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)
- 0 = Write cycle to the data EEPROM is complete

bit 0 **RD:** Read Control bit
- 1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.)
- 0 = Does not initiate an EEPROM read

TABLE 11-1: TYPICAL OUTPUT ENABLE FILTER TIMING

OEH <1:0>	OEL <1:0>	TOEH (ms)	TOEL (ms)	TOET (ms)
01	00	1	1	3
01	01	1	1	3
01	10	1	2	4
01	11	1	4	6
10	00	2	1	4
10	01	2	1	4
10	10	2	2	5
10	11	2	4	8
11	00	4	1	6
11	01	4	1	6
11	10	4	2	8
11	11	4	4	10
00	xx	Filter Disabled		

Note 1: Typical at room temperature and VDD = 3.0V, 32 kHz oscillator.

TOEH is measured from the rising edge of the demodulator output to the first falling edge. The pulse width must fall within TOEH ≤ *t* ≤ TOET.

TOEL is measured from the falling edge of the demodulator output to the rising edge of the next pulse. The pulse width must fall within TOEL ≤ *t* ≤ TOET.

TOET is measured from rising edge to the next rising edge (i.e., the sum of TOEH and TOEL). The pulse width must be *t* ≤ TOET. If the Configuration Register 0 (Register 11-1), OEL<8:7> is set to '00', then TOEH must not exceed TOET and TOEL must not exceed TINACT.

The filter will reset, requiring a complete new successive high and low period to enable LFDATA, under the following conditions.

- The received high is not greater than the configured minimum TOEH value.
- During TOEH, a loss of signal > 56 µs. A loss of signal < 56 µs may or may not cause a filter Reset.
- The received low is not greater than the configured minimum TOEL value.
- The received sequence exceeds the maximum TOET value:
  - TOEH + TOEL > TOET
  - or TOEH > TOET
  - or TOEL > TOET
- A Soft Reset SPI command is received.

If the filter resets due to a long high (TOEH > TOET), the high-pulse timer will not begin timing again until after a gap of TE and another low-to-high transition occurs on the demodulator output.

Disabling the output enable filter disables the TOEH and TOEL requirement and the AFE passes all received LF data. See Figure 11-10, Figure 11-11 and Figure 11-12 for examples.

When viewed from an application perspective, from the pin input, the actual output enable filter timing must factor in the analog delays in the input path (such as demodulator charge and discharge times).

- **TOEH** - TDR + TDF
- **TOEL** + TDR - TDF

The output enable filter starts immediately after TGAP, the gap after AGC stabilization period.

11.16 Input Sensitivity Control

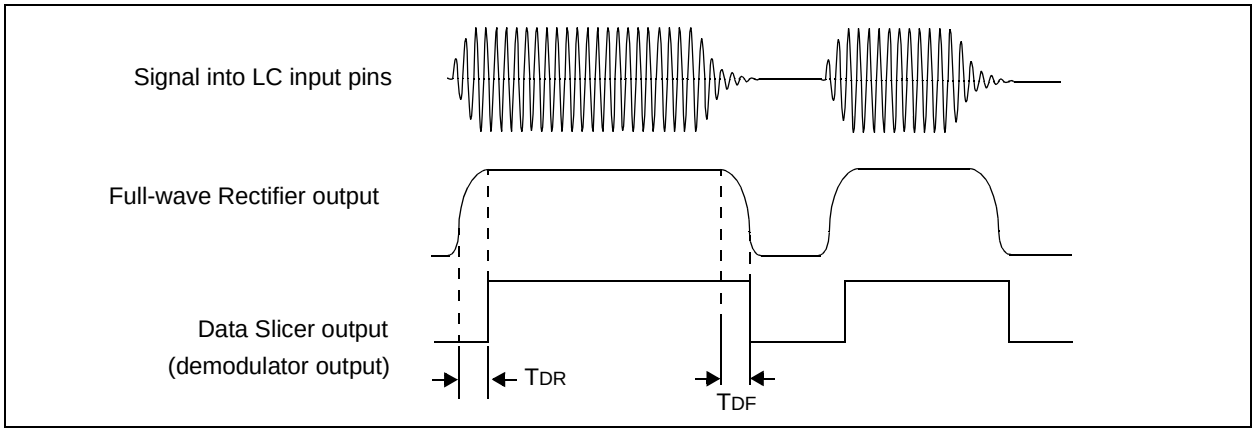
The AFE is designed to have typical input sensitivity of 3 mVPP. This means any input signal with amplitude greater than 3 mVPP can be detected. The AFE's internal AGC loop regulates the detecting signal amplitude when the input level is greater than approximately 20 mVPP. This signal amplitude is called "AGC-active level". The AGC loop regulates the input voltage so that the input signal amplitude range will be kept within the linear range of the detection circuits without saturation. The AGC Active Status bit AGCACT<5>, in the AFE Status Register 7 (Register 11-8) is set if the AGC loop regulates the input voltage.

Table 11-2 shows the input sensitivity comparison when the AGCSIG option is used. When AGCSIG option bit is set, the demodulated output is available only when the AGC loop is active (see Table 11-1). The AFE has also input sensitivity reduction options per each channel. The Configuration Register 3 (Register 11-4), Configuration Register 4 (Register 11-5) and Configuration Register 5 (Register 11-6) have the option to reduce the channel gains from 0 dB to approximately -30 dB.

11.29 Demodulator

The demodulator recovers the modulation data from the received signal, containing carrier plus data, by appropriate envelope detection. The demodulator has a fast rise (charge) time (T_{DR}) and a fall time (T_{DF}) appropriate to an envelope of input signal (see **Section 15.0 "Electrical Specifications"** for T_{DR} and T_{DF} specifications). The demodulator contains the full-wave rectifier, low-pass filter, peak detector and data slicer.

FIGURE 11-9: DEMODULATOR CHARGE AND DISCHARGE



11.30 Power-On Reset

This circuit remains in a Reset state until a sufficient supply voltage is applied to the AFE. The Reset releases when the supply is sufficient for correct AFE operation, nominally V_{POR} of AFE.

The Configuration registers are all cleared on a Power-on Reset. As the Configuration registers are protected by odd row and column parity, the $\overline{ALERT}$ pin will be pulled down – indicating to the microcontroller section that the AFE configuration memory is cleared and requires loading.

11.31 LFDATA Output Selection

The LFDATA output can be configured to pass the Demodulator output, Received Signal Strength Indicator (RSSI) output, or Carrier Clock. See Configuration Register 1 (Register 11-2) for more details.

11.31.1 DEMODULATOR OUTPUT

The demodulator output is the default configuration of the output selection. This is the output of an envelope detection circuit. See Figure 11-9 for the demodulator output.

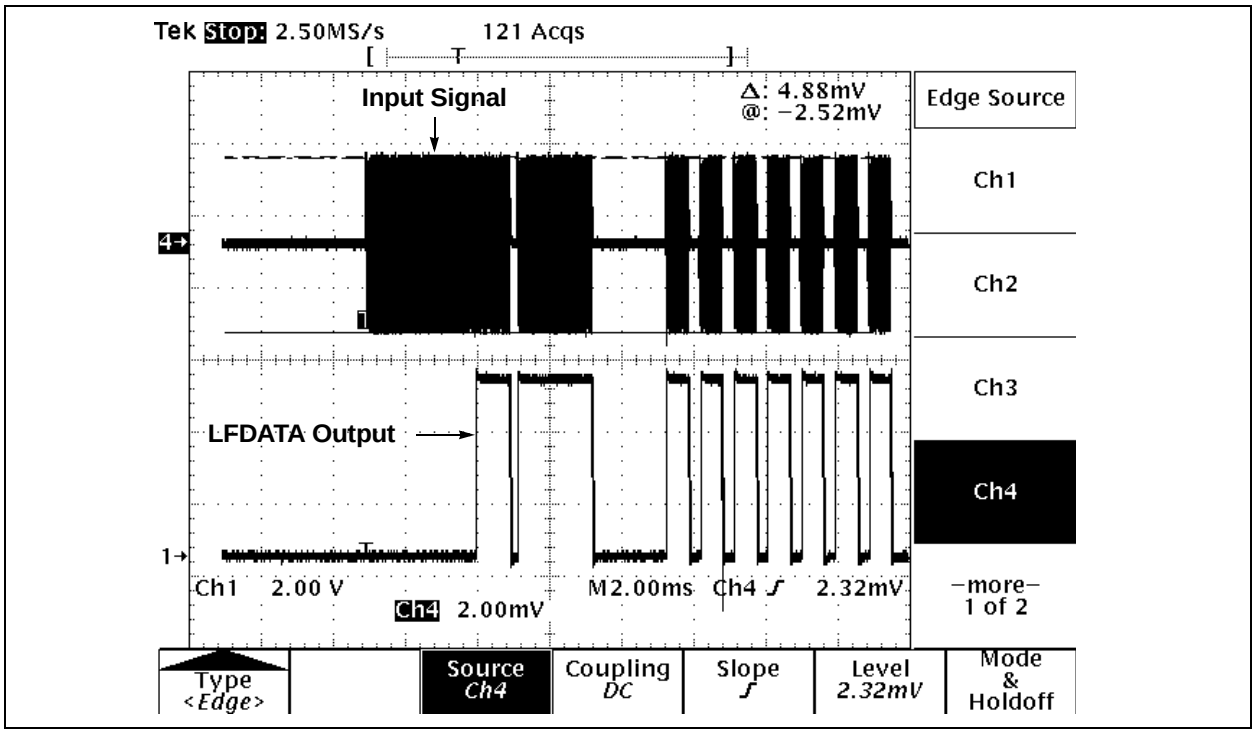
For a clean data output or to save operating power, the input channels can be individually enabled or disabled. If more than one channel is enabled, the output is the sum of each output of all enabled channels. There will be no valid output if all three channels are disabled. When the demodulated output is selected, the output is available in two different conditions depending on how the options of Configuration Register 0 (Register 11-1) are set: Output Enable Filter is disabled or enabled.

Related Configuration register bits:

- Configuration Register 1 (Register 11-2), DATOUT <8:7>:
  - bit 8 bit 7
    - 0 0: Demodulator Output
    - 0 1: Carrier Clock Output
    - 1 0: RSSI Output
    - 0 1: RSSI Output
- Configuration Register 0 (Register 11-1): all bits

Case I. When Output Enable Filter is disabled: Demodulated output is available immediately after the AGC stabilization time (TAGC). Figure 11-10 shows an example of demodulated output when the Output Enable Filter is disabled.

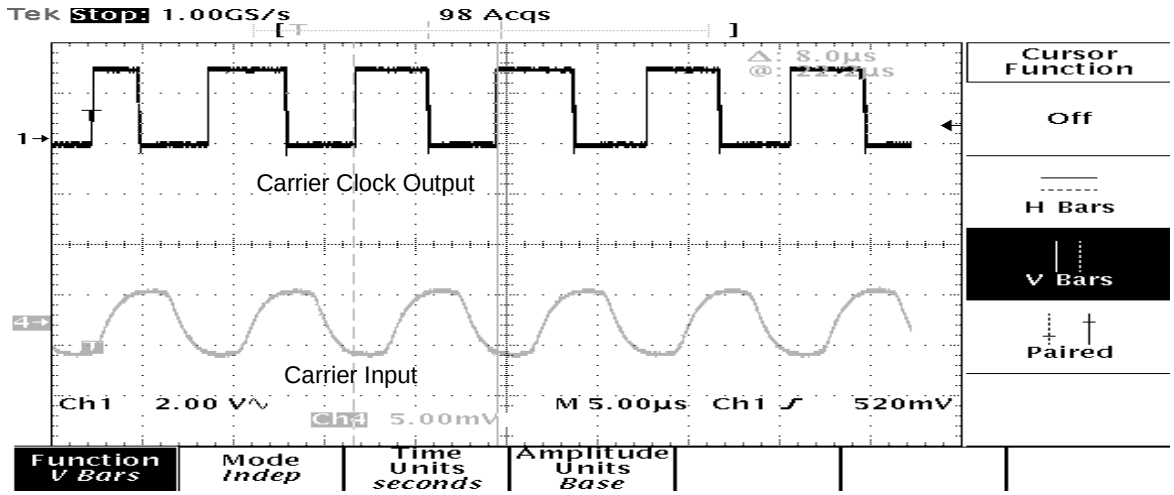
FIGURE 11-10: INPUT SIGNAL AND DEMODULATOR OUTPUT WHEN THE OUTPUT ENABLE FILTER IS DISABLED



Case II. When Output Enable Filter is enabled: Demodulated output is available only if the incoming signal meets the enable filter timing criteria that is defined in the Configuration Register 0 (Register 11-1). If the criteria is met, the output is available after the low timing (TOEL) of the Enable Filter. Figure 11-11 and Figure 11-12 shows examples of demodulated output when the Output Enable Filter is enabled.

FIGURE 11-13: CARRIER CLOCK OUTPUT EXAMPLES

(A) CARRIER CLOCK OUTPUT WITH CARRIER/1 OPTION



(B) CARRIER CLOCK OUTPUT WITH CARRIER/4 OPTION

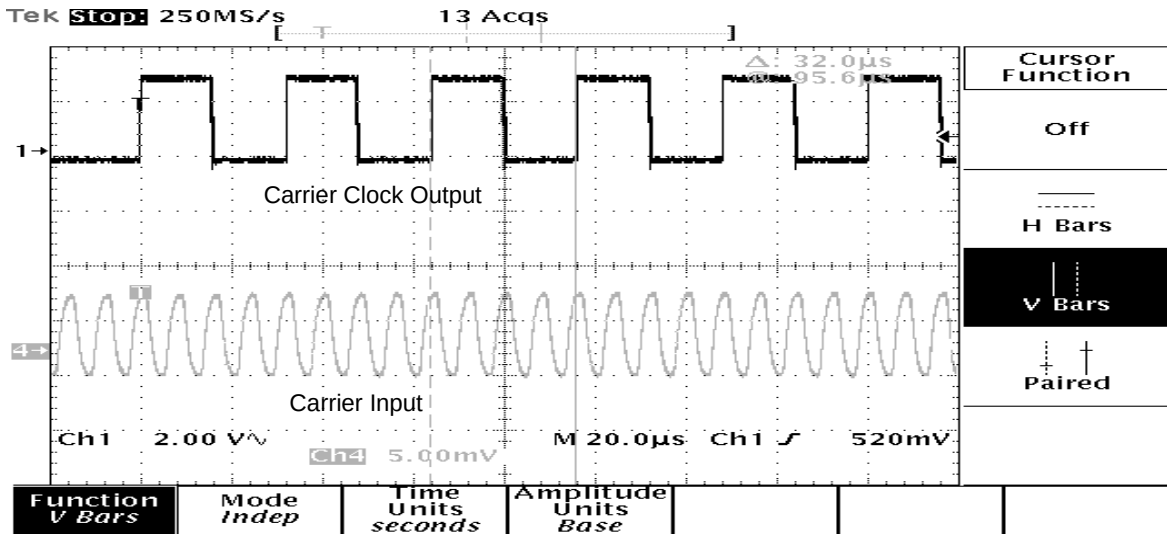
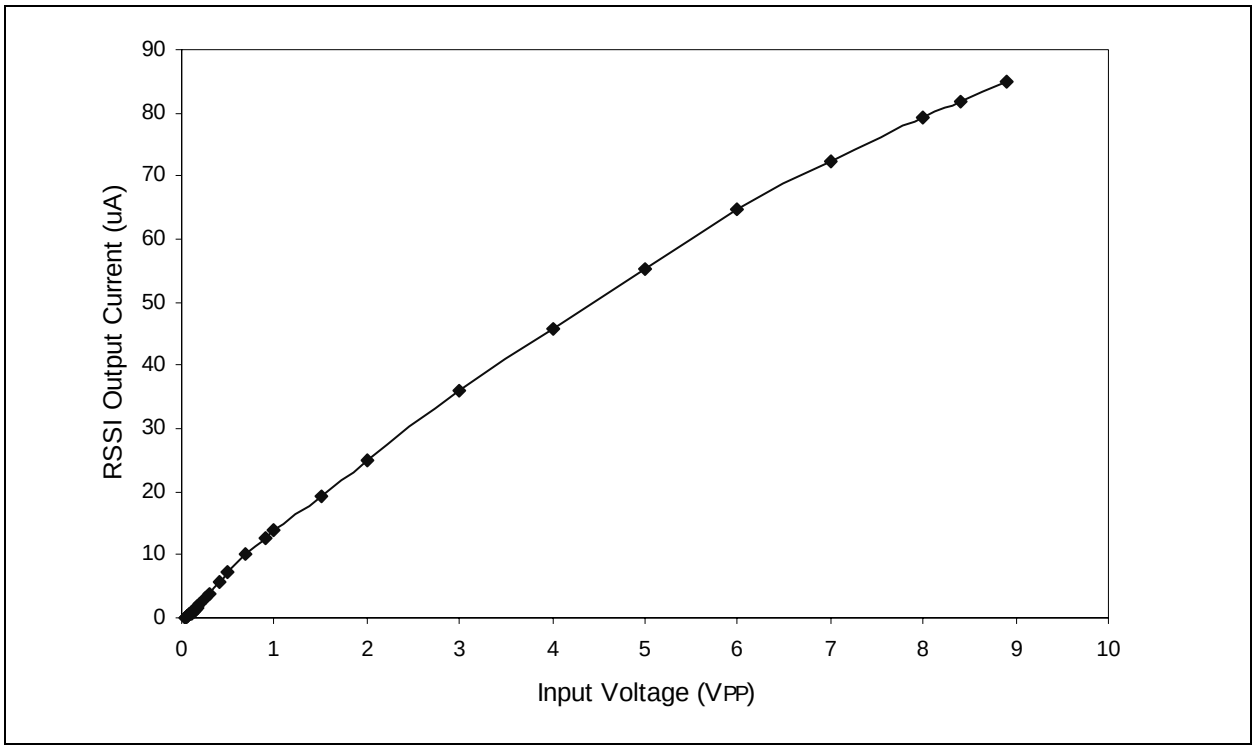


FIGURE 11-15: RSSI OUTPUT CURRENT VS. INPUT SIGNAL LEVEL EXAMPLE



12.6 Brown-out Reset (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register select one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = 01, the SBOREN bit of the PCON register enables/disables the BOR allowing it to be controlled in software. By selecting BOREN<1:0>, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 12-1 for the Configuration Word definition.

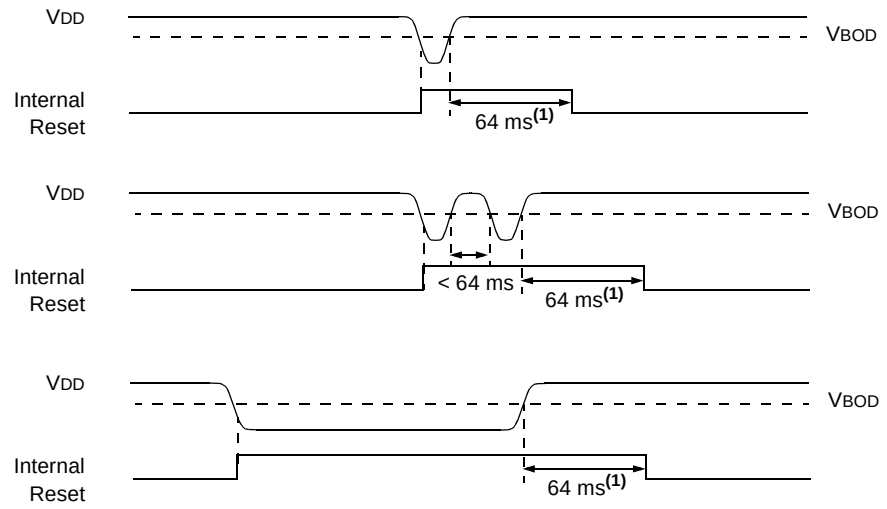
If VDD falls below VBOD for greater than parameter (TBOD) (see **Section 15.0 "Electrical Specifications"**), the Brown-out situation will reset the device. This will occur regardless of VDD slew rate. A Reset is not ensured to occur if VDD falls below VBOD for less than parameter (TBOD).

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOD (see Figure 12-3). The Power-up Timer will now be invoked, if enabled and will keep the chip in Reset an additional nominal 64 ms.

Note:	The Power-up Timer is enabled by the $\overline{\text{PWRTE}}$ bit in the Configuration Word register.

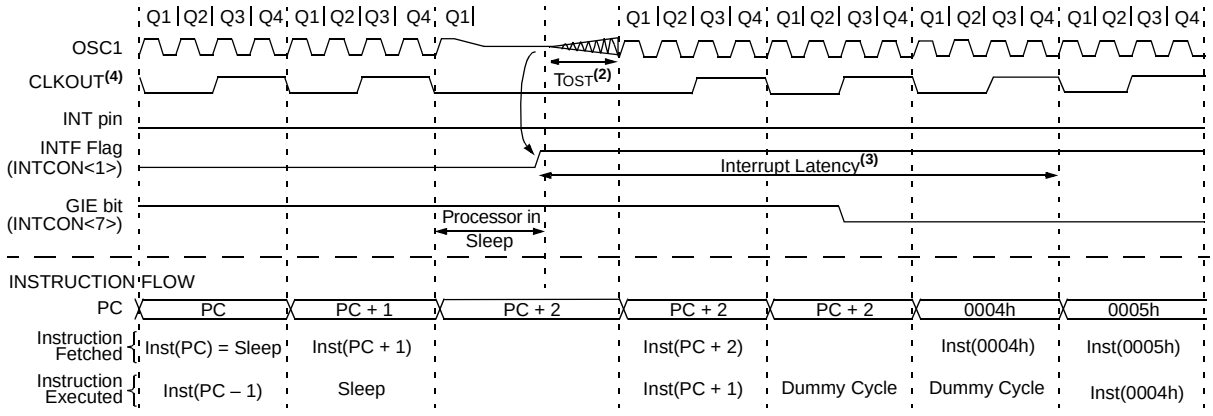
If VDD drops below VBOD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOD, the Power-up Timer will execute a 64 ms Reset.

FIGURE 12-3: BROWN-OUT RESET SITUATIONS



Note 1: Nominal 64 ms delay only if $\overline{\text{PWRTE}}$ bit is programmed to '0'.

FIGURE 12-10: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP Oscillator mode assumed.

2: TOST = 1024 TOSC (drawing not to scale). This delay does not apply to EC and RC Oscillator modes.

3: GIE = 1 assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = 0, execution will continue in-line.

4: CLKOUT is not available in XT, HS, LP or EC Oscillator modes, but shown here for timing reference.

12.13 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP for verification purposes.

Note:	The entire data EEPROM and Flash program memory will be erased when the code protection is turned off. See the *"*PIC12F6XX/16F6XX *Memory Programming Specification"* (DS41204) for more information.

12.14 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.

12.15 In-Circuit Serial Programming

The PIC12F635/PIC16F636/639 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for:

- Power
- Ground
- Programming Voltage

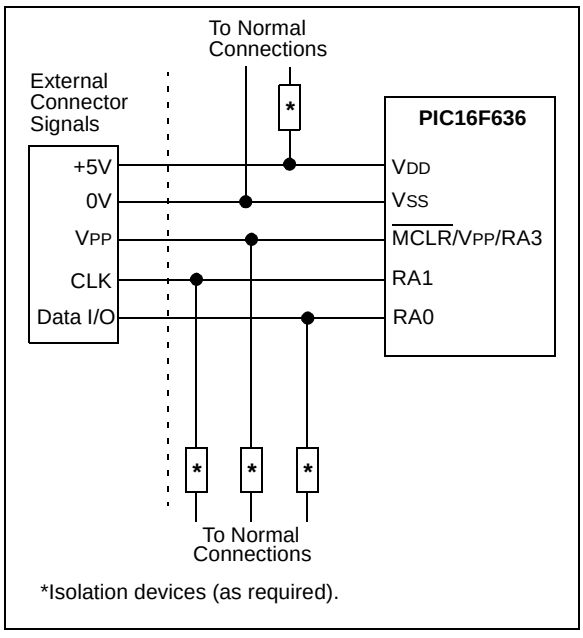
This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the RA0 and RA1 pins low, while raising the MCLR (V_{PP}) pin from V_{IL} to V_{IHH}. See the *"PIC12F6XX/16F6XX Memory Programming Specification"* (DS41204) for more information. RA0 becomes the programming data and RA1 becomes the programming clock. Both RA0 and RA1 are Schmitt Trigger inputs in this mode.

After Reset, to place the device into Program/Verify mode, the Program Counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the *"PIC12F6XX/16F6XX Memory Programming Specification"* (DS41204).

A typical In-Circuit Serial Programming connection is shown in Figure 12-11.

FIGURE 12-11: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



12.16 In-Circuit Debugger

Since in-circuit debugging requires the loss of clock, data and MCLR pins, MPLAB® ICD 2 development with a 14-pin device is not practical. A special 20-pin PIC16F636 ICD device is used with MPLAB ICD 2 to provide separate clock, data and MCLR pins and frees all normally available pins to the user.

Use of the ICD device requires the purchase of a special header. On the top of the header is an MPLAB ICD 2 connector. On the bottom of the header is a 14-pin socket that plugs into the user's target via the 14-pin stand-off connector.

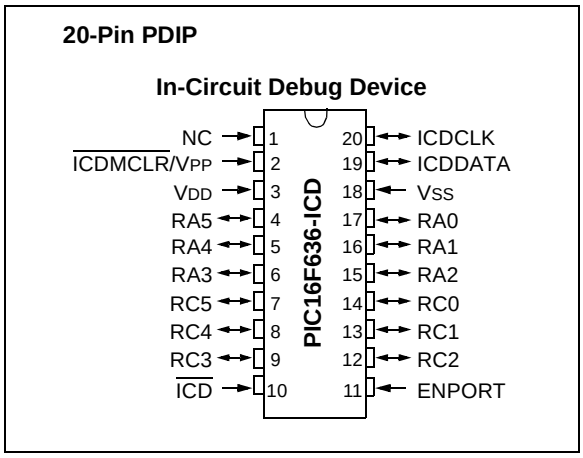
When the ICD pin on the PIC16F636 ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 12-9 shows which features are consumed by the background debugger:

TABLE 12-9: DEBUGGER RESOURCES

Resource	Description
I/O pins	ICDCLK, ICDDATA
Stack	1 level
Program Memory	Address 0h must be `NOP` 700h-7FFh

For more information, see the "*MPLAB® ICD 2 In-Circuit Debugger User's Guide*" (DS51331), available on Microchip's web site (www.microchip.com).

FIGURE 12-12: 20-PIN ICD PINOUT



MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Description: The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:
```
MOVF    FSR, 0
```
After Instruction
W = value in FSR register
Z = 1

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \le f \le 127$

Operation: (W) → (f)

Status Affected: None

Description: Move data from W register to register 'f'.

Words: 1

Cycles: 1

Example:
```
MOVW    OPTION
F
```
Before Instruction
OPTION = 0xFF
W = 0x4F
After Instruction
OPTION = 0x4F
W = 0x4F

MOVLW **Move literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (W)

Status Affected: None

Description: The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Description: No operation.

Words: 1

Cycles: 1

Example:
```
NOP
```

15.8 Thermal Considerations

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C						
Param No.	**Sym**	**Characteristic**		**Typ**	**Units**	**Conditions**
TH01	θJA	Thermal Resistance Junction to Ambient	PIC12F635	84.6	°C/W	8-pin PDIP package
				163.0	°C/W	8-pin SOIC package
				52.4	°C/W	8-pin DFN 4x4x0.9 mm package
				52.4	°C/W	8-pin DFN-S 6x5 mm package
			PIC16F636	69.8	°C/W	14-pin PDIP package
				85.0	°C/W	14-pin SOIC package
				100.4	°C/W	14-pin TSSOP package
				46.3	°C/W	16-pin QFN 4x0.9mm package
			PIC16F639	108.1	°C/W	20-pin SSOP package
TH02	θJC	Thermal Resistance Junction to Case	PIC12F635	41.2	°C/W	8-pin PDIP package
				38.8	°C/W	8-pin SOIC package
				3.0	°C/W	8-pin DFN 4x4x0.9 mm package
				3.0	°C/W	8-pin DFN-S 6x5 mm package
			PIC16F636	32.5	°C/W	14-pin PDIP package
				31.0	°C/W	14-pin SOIC package
				31.7	°C/W	14-pin TSSOP package
				2.6	°C/W	16-pin QFN 4x0.9mm package
			PIC16F639	32.2	°C/W	20-pin SSOP package
TH03	TJ	Junction Temperature		150	°C	For derated power calculations
TH04	PD	Power Dissipation		—	W	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation		—	W	PINTERNAL = IDD x VDD **(NOTE 1)**
TH06	PI/O	I/O Power Dissipation		—	W	PI/O = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH))
TH07	PDER	Derated Power		—	W	PDER = (TJ - TA)/θJA **(NOTE 2, 3)**

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature.

3: Maximum allowable power dissipation is the lower value of either the absolute maximum total power dissipation or derated power (PDER).

TABLE 15-9: PIC16F639 PLVD CHARACTERISTICS:

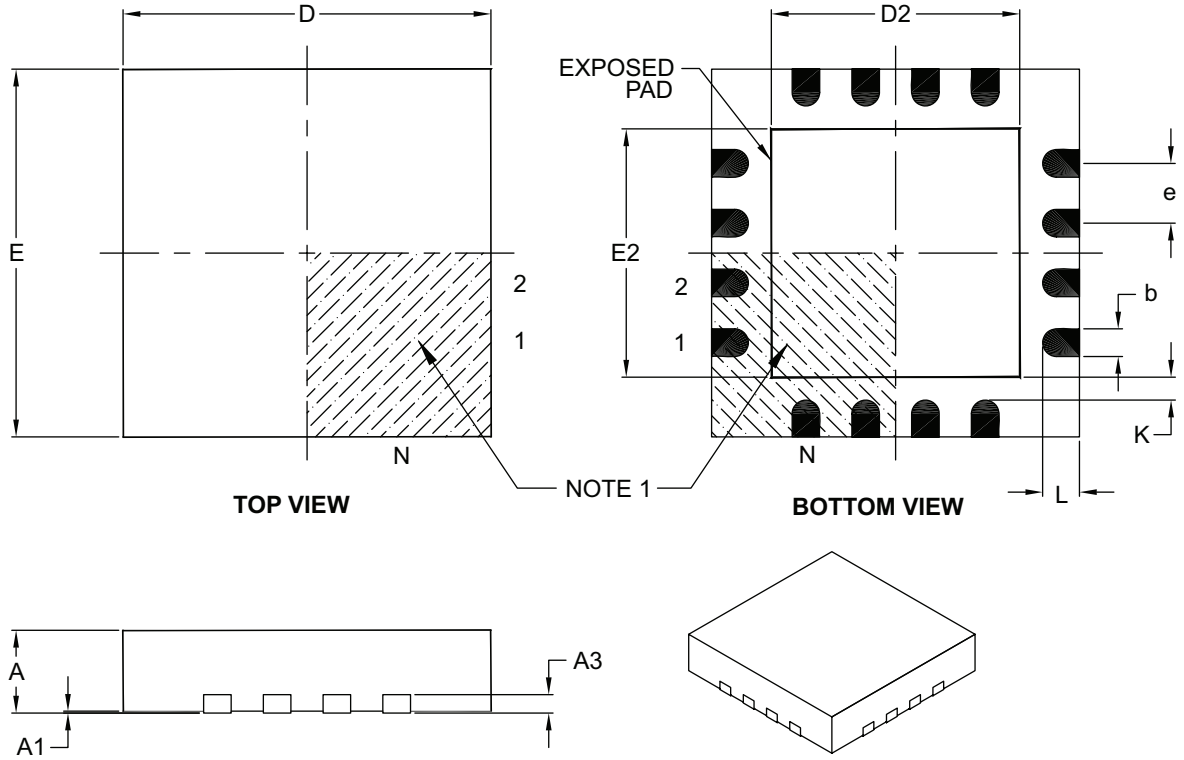
DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +85°C Operating Voltage VDD Range 2.0V-5.5V				
Sym.	**Characteristic**		**Min**	**Typ†**	**Max**	**Units**	**Conditions**
VPLVD	PLVD Voltage	LVDL<2:0> = 001	1.900	2.0	2.100	V	
		LVDL<2:0> = 010	2.000	2.1	2.200	V	
		LVDL<2:0> = 011	2.100	2.2	2.300	V	
		LVDL<2:0> = 100	2.200	2.3	2.400	V	
		LVDL<2:0> = 101	3.825	4.0	4.175	V	
		LVDL<2:0> = 110	4.025	4.2	4.375	V	
		LVDL<2:0> = 111	4.325	4.5	4.675	V	
*TPLVDS	PLVD Settling time		—	50 25	—	µs	VDD = 5.0V VDD = 3.0V

* These parameters are characterized but not tested

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B