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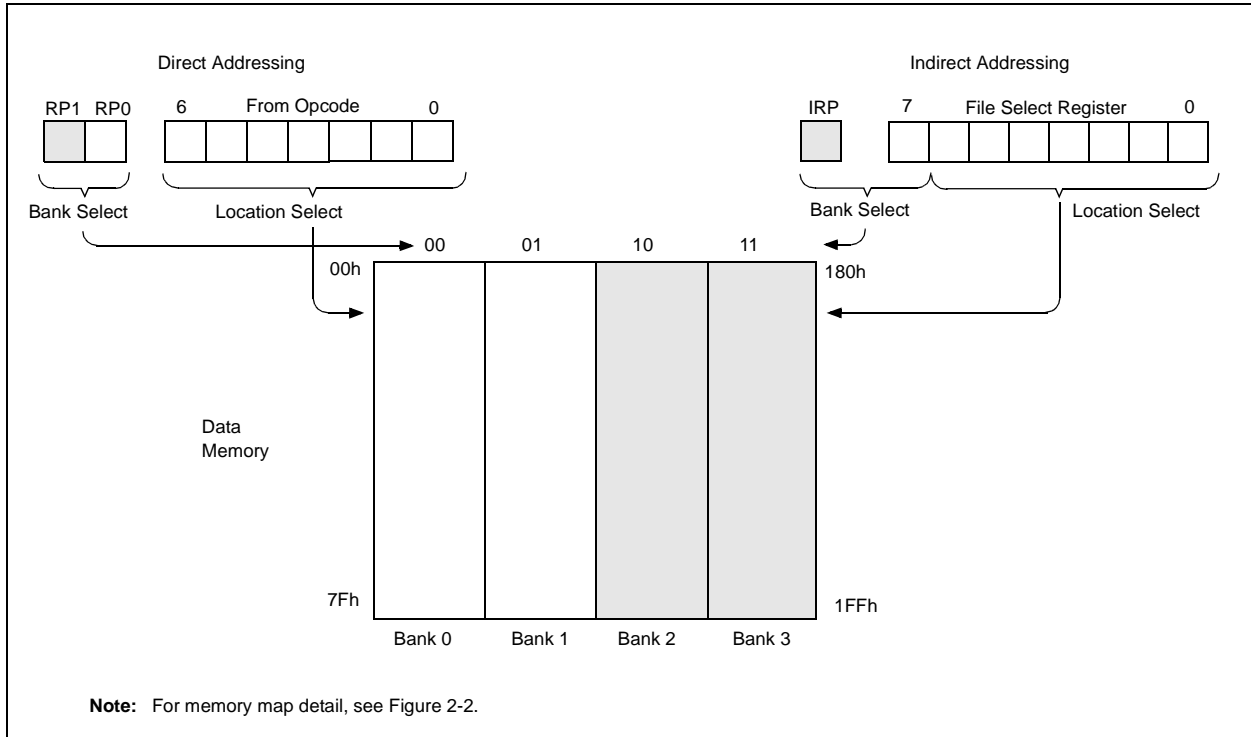
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f636t-i-sl

PIC12F635/PIC16F636/639

FIGURE 2-6: DIRECT/INDIRECT ADDRESSING PIC12F635/PIC16F636/639



3.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

3.1 Overview

The Oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 3-1 illustrates a block diagram of the Oscillator module.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured from one of two internal oscillators, with a choice of speeds selectable via software. Additional clock features include:

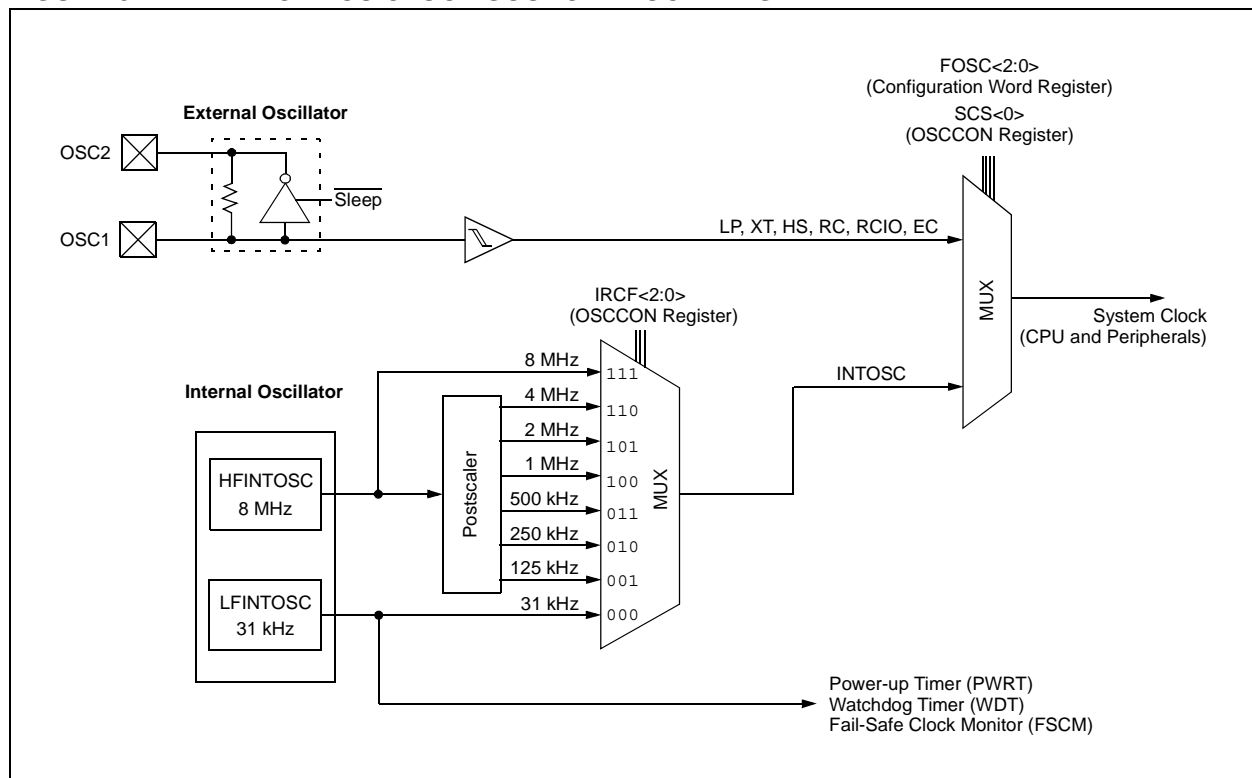
- Selectable system clock source between external or internal via software.
- Two-Speed Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch automatically to the internal oscillator.

The Oscillator module can be configured in one of eight clock modes.

1. EC – External clock with I/O on OSC2/CLKOUT.
2. LP – 32 kHz Low-Power Crystal mode.
3. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
4. HS – High Gain Crystal or Ceramic Resonator mode.
5. RC – External Resistor-Capacitor (RC) with Fosc/4 output on OSC2/CLKOUT.
6. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
7. INTOSC – Internal oscillator with Fosc/4 output on OSC2 and I/O on OSC1/CLKIN.
8. INTOSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.

Clock Source modes are configured by the FOSC<2:0> bits in the Configuration Word register (CONFIG). The internal clock can be generated from two internal oscillators. The HFINTOSC is a calibrated high-frequency oscillator. The LFINTOSC is an uncalibrated low-frequency oscillator.

FIGURE 3-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



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REGISTER 4-1: PORTA: PORTA REGISTER

U-0	U-0	R/W-x	R/W-x	R-x	R/W-x	R/W-x	R/W-x
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RA<5:0>:** PORTA I/O Pin bit

1 = Port pin is > VIH

0 = Port pin is < VIL

REGISTER 4-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bits

1 = PORTA pin configured as an input (tri-stated)

0 = PORTA pin configured as an output

Note 1: TRISA<3> always reads '1'.

Note 2: TRISA<5:4> always reads '1' in XT, HS and LP Oscillator modes.

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TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR, WUR	Value on all other Resets
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xx00	--uu uu00
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
CMCON1	—	—	—	—	—	—	T1GSS	CxSYNC	---- --10	---- --10
CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
OPTION_REG	RAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
WPUDA	—	—	WPUDA5	WPUDA4	—	WPUDA2	WPUDA1	WPUDA0	--11 -111	--11 -111
IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
WDA	—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0	--11 -111	--11 -111

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

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TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	00-- --10
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIE1	EEIE	LVDIE	CRIE	C2IE ⁽¹⁾	C1IE	OSFIE	—	TMR1IE	000- 00-0	000- 00-0
PIR1	EEIF	LVDIF	CRIF	C2IF ⁽¹⁾	C1IF	OSFIF	—	TMR1IF	000- 00-0	000- 00-0
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYN \overline{C}	TMR1CS	TMR1ON	0000 0000	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: PIC16F636/639 only.

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7.4 Comparator Control

The CMCON0 register (Register 7-1) provides access to the following comparator features:

- Mode selection
- Output state
- Output polarity
- Input switch

7.4.1 COMPARATOR OUTPUT STATE

Each comparator state can always be read internally via the CxOUT bit of the CMCON0 register. The comparator state may also be directed to the CxOUT pin in the following modes:

PIC12F635

- CM<2:0> = 001
- CM<2:0> = 011
- CM<2:0> = 101

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- CM<2:0> = 110

When one of the above modes is selected, the associated TRIS bit of the CxOUT pin must be cleared.

7.4.2 COMPARATOR OUTPUT POLARITY

Inverting the output of a comparator is functionally equivalent to swapping the comparator inputs. The polarity of a comparator output can be inverted by setting the CxINV bit of the CMCON0 register. Clearing CxINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 7-1.

TABLE 7-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	CxINV	CxOUT
VIN- > VIN+	0	0
VIN- < VIN+	0	1
VIN- > VIN+	1	1
VIN- < VIN+	1	0

Note: CxOUT refers to both the register bit and output pin.

7.4.3 COMPARATOR INPUT SWITCH

The inverting input of the comparators may be switched between two analog pins in the following modes:

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- CM<2:0> = 101
- CM<2:0> = 110

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- CM<2:0> = 001 (Comparator C1 only)
- CM<2:0> = 010 (Comparators C1 and C2)

In the above modes, both pins remain in Analog mode regardless of which pin is selected as the input. The CIS bit of the CMCON0 register controls the comparator input switch.

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TABLE 7-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CMCON0	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	---- --10
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIE1	EEIE	LVDIE	CRIE	—	C1IE	OSFIE	—	TMR1IE	000- 00-0	000- 00-0
PIR1	EEIF	LVDIF	CRIF	—	C1IF	OSFIF	—	TMR1IF	000- 00-0	000- 00-0
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for comparator.

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9.1 EECON1 AND EECON2 Registers

EECON1 is the control register with four low-order bits physically implemented. The upper four bits are non-implemented and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR Reset, or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit, clear it and rewrite the location. The data and address will be cleared. Therefore, the EEDAT and EEADR registers will need to be re-initialized.

Interrupt flag, EEIF bit of the PIR1 register, is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence.

Note: The EECON1, EEDAT and EEADR registers should not be modified during a data EEPROM write (WR bit = 1).

REGISTER 9-3: EECON1: EEPROM CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD
bit 7				bit 0			

Legend:

S = Bit can only be set

R = Readable bit

-n = Value at POR

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **WRERR:** EEPROM Error Flag bit

1 = A write operation is prematurely terminated (any MCLR Reset, any WDT Reset during normal operation or BOR Reset)

0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit

1 = Allows write cycles

0 = Inhibits write to the data EEPROM

bit 1 **WR:** Write Control bit

1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)

0 = Write cycle to the data EEPROM is complete

bit 0 **RD:** Read Control bit

1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.)

0 = Does not initiate an EEPROM read

11.14.2 INACTIVITY TIMER

The Inactivity Timer is used to automatically return the AFE to Standby mode, if there is no input signal. The time-out period is approximately 16 ms (T_{INACT}), based on the 32 kHz internal clock.

The purpose of the Inactivity Timer is to minimize AFE current draw by automatically returning the AFE to the lower current Standby mode, if there is no input signal for approximately 16 ms.

The timer is reset when:

- An amplitude change in LF input signal, either high-to-low or low-to-high
- $\overline{\text{CS}}$ pin is low (any SPI command)
- Timer-related Soft Reset

The timer starts when:

- AFE receives any LF signal

The timer causes an AFE Soft Reset when:

- A previously received LF signal does not change either high-to-low or low-to-high for T_{INACT}

The Soft Reset returns the AFE to Standby mode where most of the analog circuits, such as the AGC, demodulator and RC oscillator, are powered down. This returns the AFE to the lower Standby Current mode.

11.14.3 ALARM TIMER

The Alarm Timer is used to notify the MCU that the AFE is receiving LF signal that does not pass the output enable filter requirement. The time-out period is approximately 32 ms (T_{ALARM}) in the presence of continuing noise.

The Alarm Timer time-out occurs if there is an input signal for longer than 32 ms that does not meet the output enable filter requirements. The Alarm Timer time-out causes:

- a) The $\overline{\text{ALERT}}$ pin to go low.
- b) The ALARM bit to set in the AFE Status Configuration 7 register (Register 11-8).

The MCU is informed of the Alarm timer time-out by monitoring the $\overline{\text{ALERT}}$ pin. If the Alarm timer time-out occurs, the MCU can take appropriate actions such as lowering channel sensitivity or disabling channels. If the noise source is ignored, the AFE can return to a lower standby current draw state.

The timer is reset when the:

- $\overline{\text{CS}}$ pin is low (any SPI command).
- Output enable filter is disabled.
- LFDATA pin is enabled (signal passed output enable filter).

The timer starts when:

- Receiving a LF signal.

The timer causes a low output on the $\overline{\text{ALERT}}$ pin when:

- Output enable filter is enabled and modulated input signal is present for T_{ALARM}, but does not pass the output enable filter requirement.

Note: The Alarm timer is disabled if the output enable filter is disabled.

11.14.4 PULSE WIDTH TIMER

The Pulse Width Timer is used to verify that the received output enable sequence meets both the minimum TOEH and minimum TOEL requirements.

11.14.5 PERIOD TIMER

The Period Timer is used to verify that the received output enable sequence meets the maximum TOET requirement.

11.14.6 AGC SETTling TIMER (TAGC)

This timer is used to keep the output enable filter in Reset while the AGC settles on the input signal. The time-out period is approximately 3.5 ms. At end of this time (TAGC), the input should remain high (TPAGC), otherwise the counting is aborted and a Soft Reset is issued. See Figure 11-6 for details.

Note 1: The AFE needs continuous and uninterrupted high input signal during AGC settling time (TAGC). Any absence of signal during this time may reset the timer and a new input signal is needed for AGC settling time, or may result in improper AGC gain settings which will produce invalid output.
--

2: The rest of the AFE section wakes up if any of these input channels receive the AGC settling time correctly. AFE Status Register 7 bits <4:2> (Register 11-8) indicate which input channels have waken up the AFE first. Valid input signal on multiple input pins can cause more than one channel's indicator bit to be set.

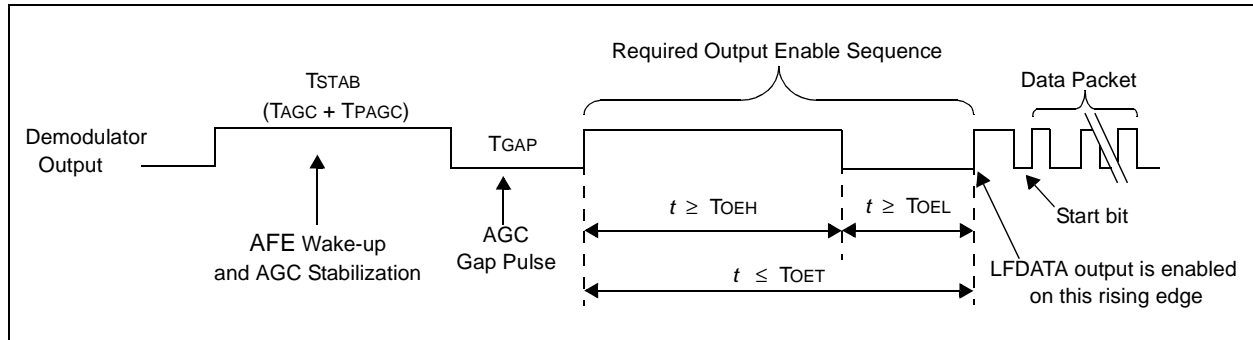
11.15 Configurable Output Enable Filter

The purpose of this filter is to enable the LFDATA output and wake the microcontroller only after receiving a specific sequence of pulses on the LC input pins. Therefore, it prevents the AFE from waking up the microcontroller due to noise or unwanted input signals. The circuit compares the timing of the demodulated header waveform with a pre-defined value, and enables the demodulated LFDATA output when a match occurs.

The output enable filter consists of a high (TOEH) and low duration (TOEL) of a pulse immediately after the AGC settling gap time. The selection of high and low times further implies a max period time. The output enable high and low times are determined by SPI interface programming. Figure 11-5 and Figure 11-6 show the output enable filter waveforms.

There should be no missing cycles during TOEH. Missing cycles may result in failing the output enable condition.

FIGURE 11-5: OUTPUT ENABLE FILTER TIMING



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TABLE 11-2: INPUT SENSITIVITY VS. MODULATED SIGNAL STRENGTH SETTING (AGCSIG <7>)

AGCSIG<7> (Config. Register 5)	Description	Input Sensitivity (Typical)
0	Disabled – the AFE passes signal of any amplitude level it is capable of detecting (demodulated data and carrier clock).	3.0 mVPP
1	Enabled – No output until AGC Status = 1 (i.e., $V_{PEAK} \approx 20$ mVPP) (demodulated data and carrier clock). <ul style="list-style-type: none">Provides the best signal to noise ratio.	20 mVPP

11.17 Input Channels (Enable/Disable)

Each channel can be individually enabled or disabled by programming bits in Configuration Register 0<3:1> (Register 11-1).

The purpose of having an option to disable a particular channel is to minimize current draw by powering down as much circuitry as possible, if the channel is not needed for operation. The exact circuits disabled when an input is disabled are amplifiers, detector, full-wave rectifier, data slicer, and modulation FET. However, the RF input limiter remains active to protect the silicon from excessive antenna input voltages.

11.18 AGC Amplifier

The circuit automatically amplifies input signal voltage levels to an acceptable level for the data slicer. Fast attack and slow release by nature, the AGC tracks the carrier signal level and not the modulated data bits.

The AGC inherently tracks the strongest of the three antenna input signals. The AGC requires an AGC stabilization time (TAGC).

The AGC will attempt to regulate a channel's peak signal voltage into the data slicer to a desired regulated AGC voltage – reducing the input path's gain as the signal level attempts to increase above regulated AGC voltage, and allowing full amplification on signal levels below the regulated AGC voltage.

The AGC has two modes of operation:

1. During the AGC settling time (TAGC), the AGC time constant is fast, allowing a reasonably short acquisition time of the continuous input signal.
2. After TAGC, the AGC switches to a slower time constant for data slicing.

Also, the AGC is frozen when the input signal envelope is low. The AGC tracks only high envelope levels.

11.19 AGC Preserve

The AGC preserve feature allows the AFE to preserve the AGC value during the AGC settling time (TAGC) and apply the value to the data slicing circuit for the following data streams instead of using a new tracking value. This feature is useful to demodulate the input signal correctly when the input has random amplitude variations at a given time period. This feature is enabled when the AFE receives an AGC Preserve On command and disabled if it receives an AGC Preserve Off command. Once the AGC Preserve On command is received, the AFE acquires a new AGC value during each AGC settling time and preserves the value until a Soft Reset or an AGC Preserve Off command is issued. Therefore, it does not need to issue another AGC Preserve On command. An AGC Preserve Off command is needed to disable the AGC preserve feature (see **Section 11.32.2.5 “AGC Preserve On Command”** and **Section 11.32.2.6 “AGC Preserve Off Command”** for AGC Preserve commands).

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11.31.3 RECEIVED SIGNAL STRENGTH INDICATOR (RSSI) OUTPUT

An analog current is available at the LFDATA pin when the Received Signal Strength Indicator (RSSI) output is selected for the AFE's Configuration register. The analog current is linearly proportional to the input signal strength (see Figure 11-15).

All timers in the circuit, such as inactivity timer, alarm timer, and AGC settling time, are disabled during the RSSI mode. Therefore, the RSSI output is not affected by the AGC settling time, and available immediately when the RSSI option is selected. The AFE enters Active mode immediately when the RSSI output is selected. The MCU I/O pin (RC3) connected to the LFDATA pin, must be set to high-impedance state during the RSSI Output mode.

When the AFE receives an SPI command during the RSSI output, the RSSI mode is temporary disabled until the SPI interface communication is completed. It returns to the RSSI mode again after the SPI interface communication is completed. The AFE holds the RSSI mode until another output type is selected (\overline{CS} low turns off the RSSI signal). To obtain the RSSI output for a particular input channel, or to save operating power, the input channel can be individually enabled or disabled. If more than one channel is enabled, the RSSI output is from the strongest signal channel. There will be no valid output if all three channels are disabled.

Related AFE Configuration register bits:

- Configuration Register 1 (Register 11-2), DATOUT<8:7>:

bit 8	bit 7
0	0: Demodulated Output
0	1: Carrier Clock Output
1	0: RSSI Output
1	1: RSSI Output

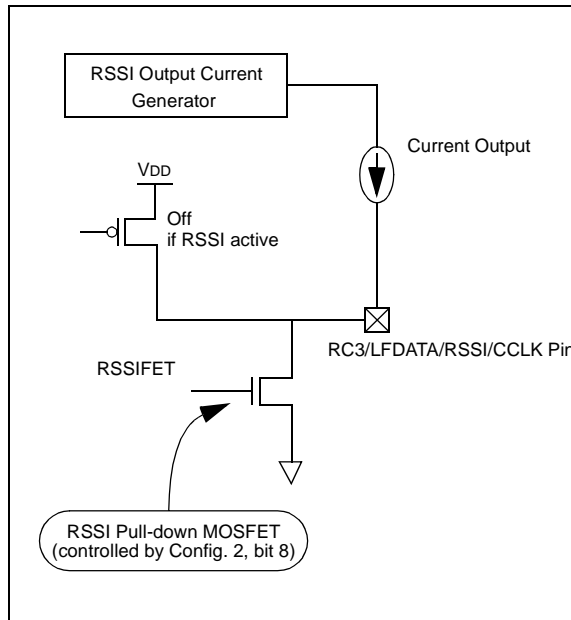
- Configuration Register 2 (Register 11-3), RSSIFET<8>:

0: Pull-Down MOSFET off
1: Pull-Down MOSFET on.

Note: The pull-down MOSFET option is valid only when the RSSI output is selected. The MOSFET is not controllable by users when Demodulated or Carrier Clock output option is selected.

- Configuration Register 0 (Register 11-1): all bits are affected.

FIGURE 11-14: RSSI OUTPUT PATH



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11.31.3.1 ANALOG-TO-DIGITAL DATA CONVERSION OF RSSI SIGNAL

The AFE's RSSI output is an analog current. It needs an external Analog-to-Digital (ADC) data conversion device for digitized output. The ADC data conversion can be accomplished by using a stand-alone external ADC device or by firmware utilizing MCU's internal comparator along with a few external resistors and a capacitor. For slope ADC implementations, the external capacitor at the LFDATA pad needs to be discharged before data sampling. For this purpose, the internal pull-down MOSFET on the LFDATA pad can be utilized. The MOSFET can be turned on or off with bit `RSSIFET<8>` of the Configuration Register 2 (Register 11-3). When it is turned on, the internal MOSFET provides a discharge path for the external capacitor. This MOSFET option is valid only if RSSI output is selected and not controllable by users for demodulated or carrier clock output options.

See separate application notes for various external ADC implementation methods for this device.

11.32 AFE Configuration

11.32.1 SPI COMMUNICATION

The AFE SPI interface communication is used to read or write the AFE's Configuration registers and to send command only messages. For the SPI interface, the device has three pads; \overline{CS} , $SCLK/ALERT$, and $LFDATA/RSSI/CCLK/SDIO$. Figure 11-15,

Figure 11-14, Figure 11-16 and Figure 11-17 shows examples of the SPI communication sequences.

When the device powers up, these pins will be high-impedance inputs until firmware modifies them appropriately. The AFE pins connected to the MCU pins will be as follows.

\overline{CS}

- Pin is permanently an input with an internal pull-up.

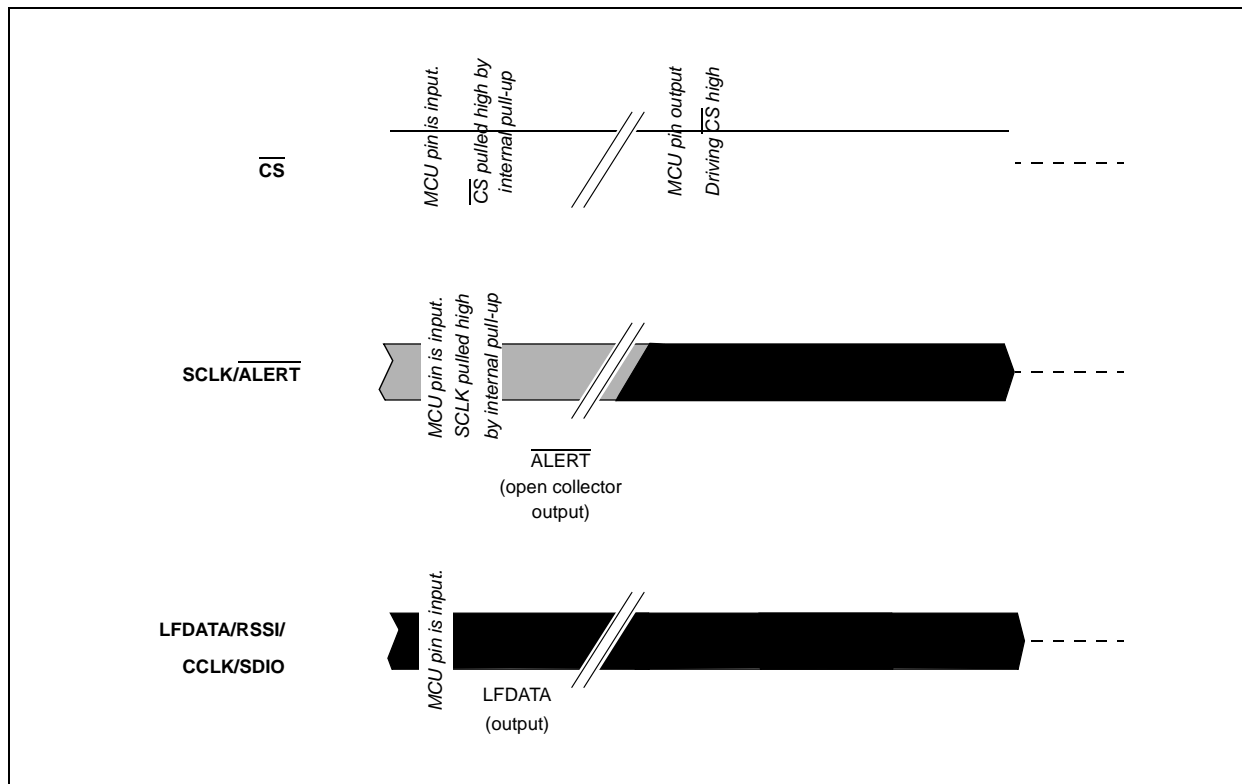
$SCLK/ALERT$

- Pin is an open collector output when \overline{CS} is high. An internal pull-up resistor exists internal to the AFE to ensure no spurious SPI communication between powering and the MCU configuring its pins. This pin becomes the SPI clock input when \overline{CS} is low.

$LFDATA/RSSI/CCLK/SDIO$

- Pin is a digital output ($LFDATA$) so long as \overline{CS} is high. During SPI communication, the pin is the SPI data input (SDI) unless performing a register Read, where it will be the SPI data output (SDO).

FIGURE 11-16: POWER-UP SEQUENCE



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FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$)

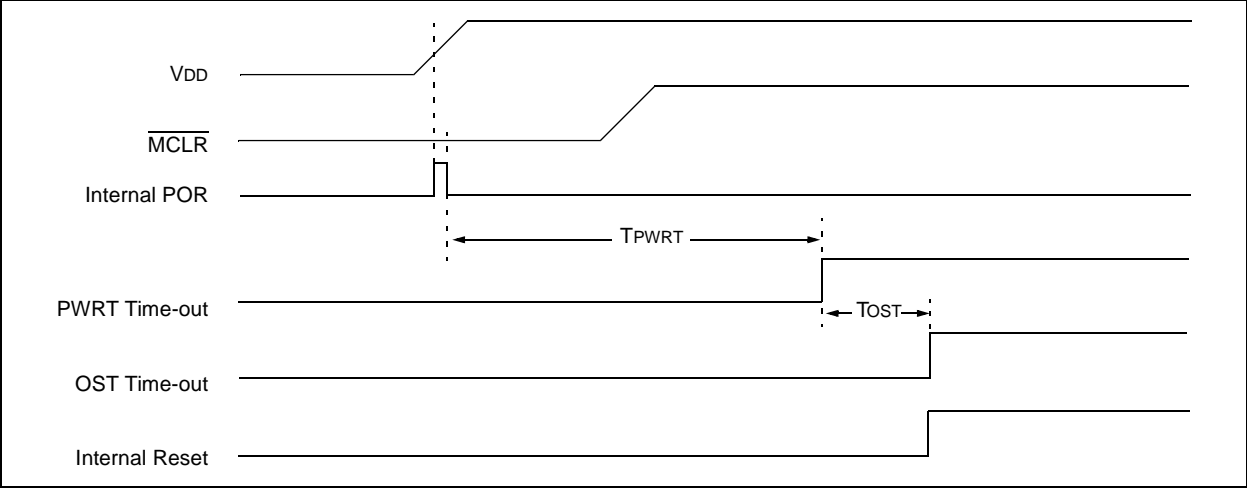


FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$)

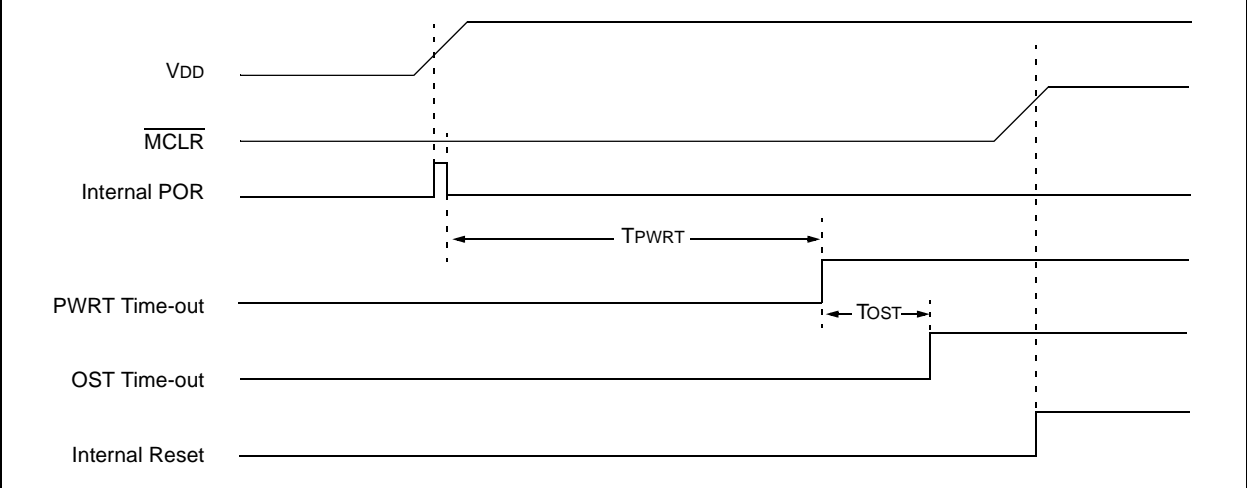
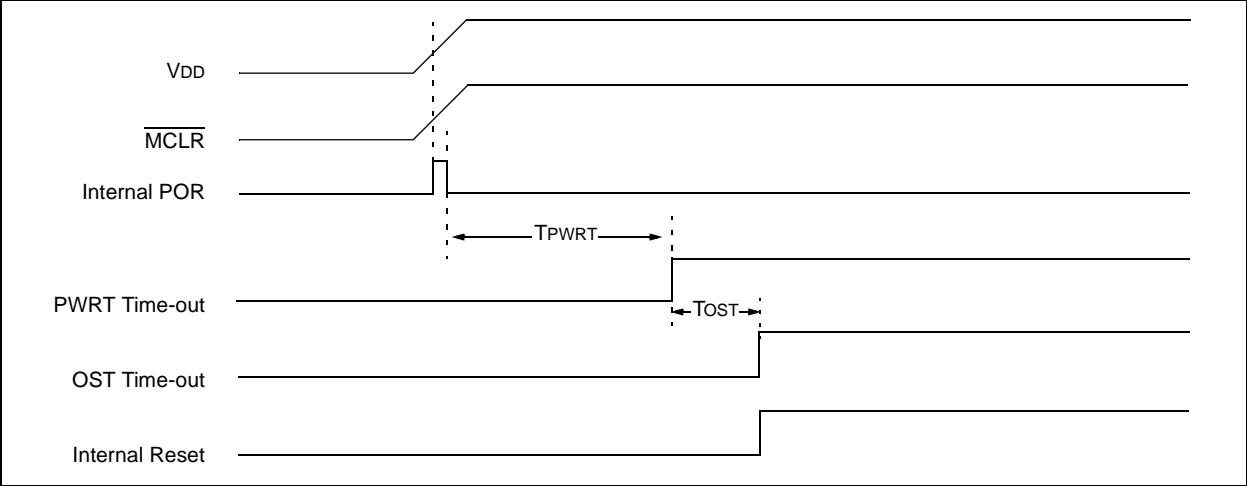


FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ WITH V_{DD})



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NOTES:

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14.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

14.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

14.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

14.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

14.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

PIC12F635/PIC16F636/639

FIGURE 15-9: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

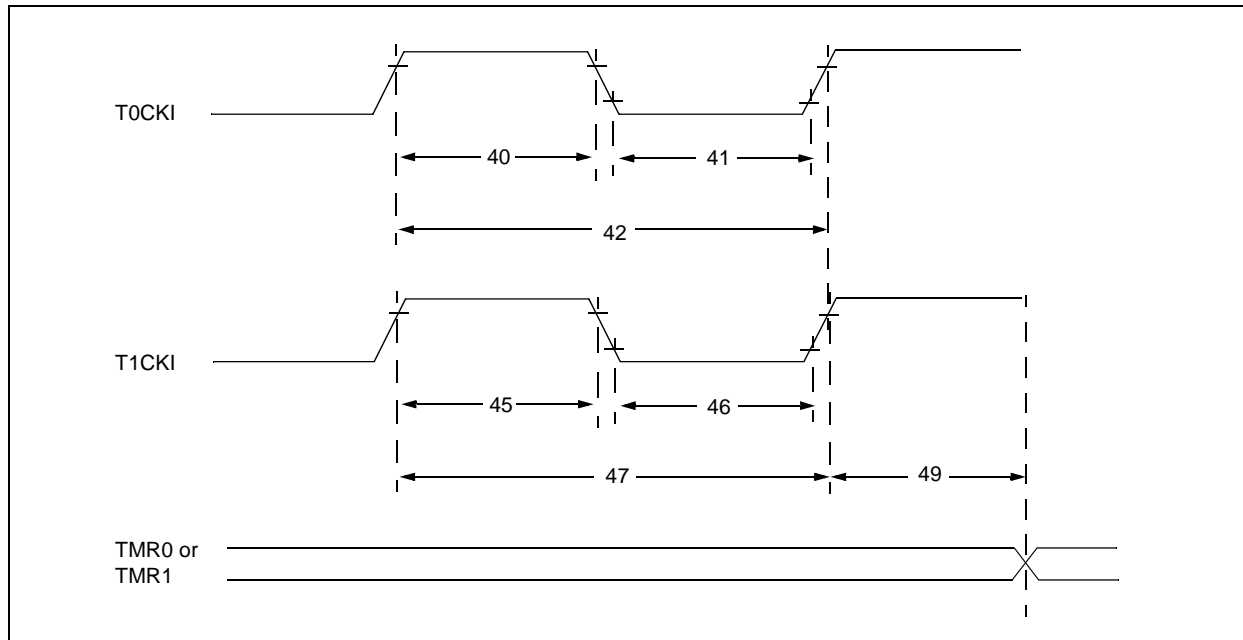


TABLE 15-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$								
Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period		Greater of: 20 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	Tt1P	T1CKI Input Period	Synchronous	Greater of: 30 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	Ft1	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)		—	32.768	—	kHz	
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment		$2 T_{OSC}$	—	$7 T_{OSC}$	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 16-28: SCHMITT TRIGGER INPUT THRESHOLD V_{IN} vs. V_{DD} OVER TEMPERATURE

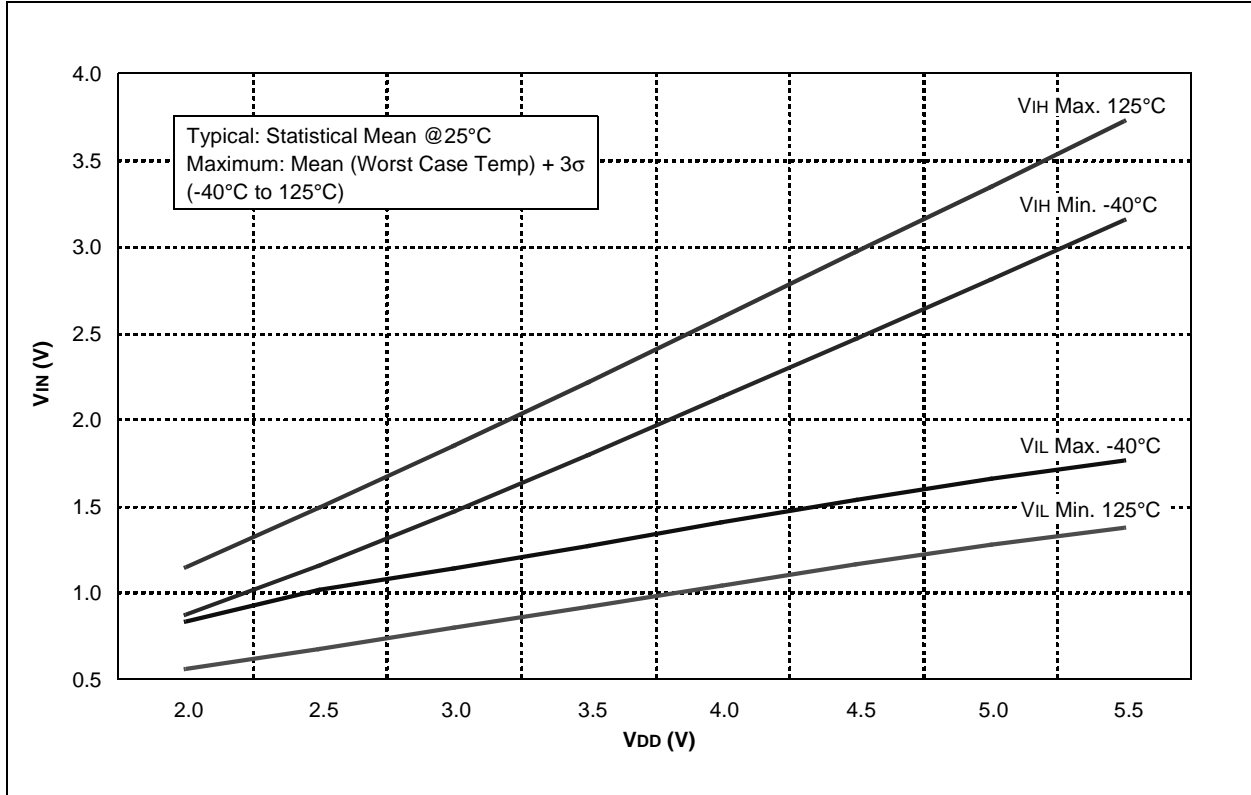
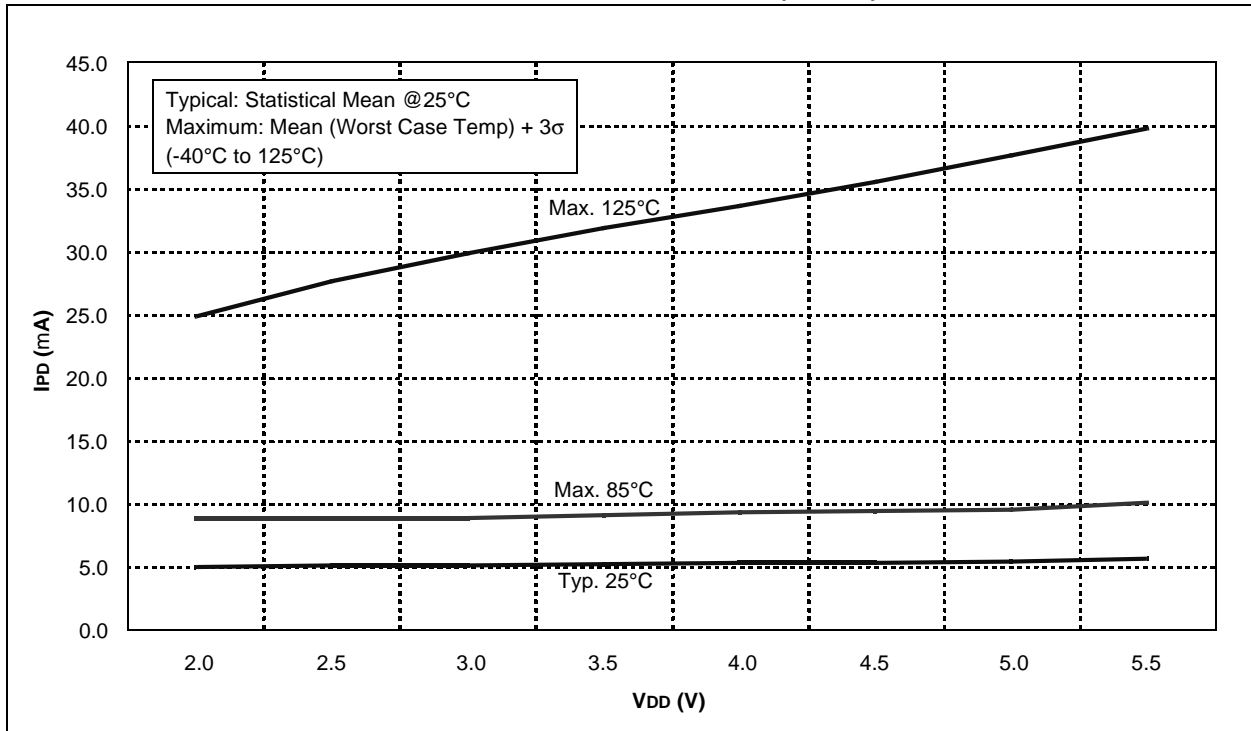


FIGURE 16-29: T1OSC IPD vs. V_{DD} OVER TEMPERATURE (32 kHz)



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FIGURE 16-34: MAXIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

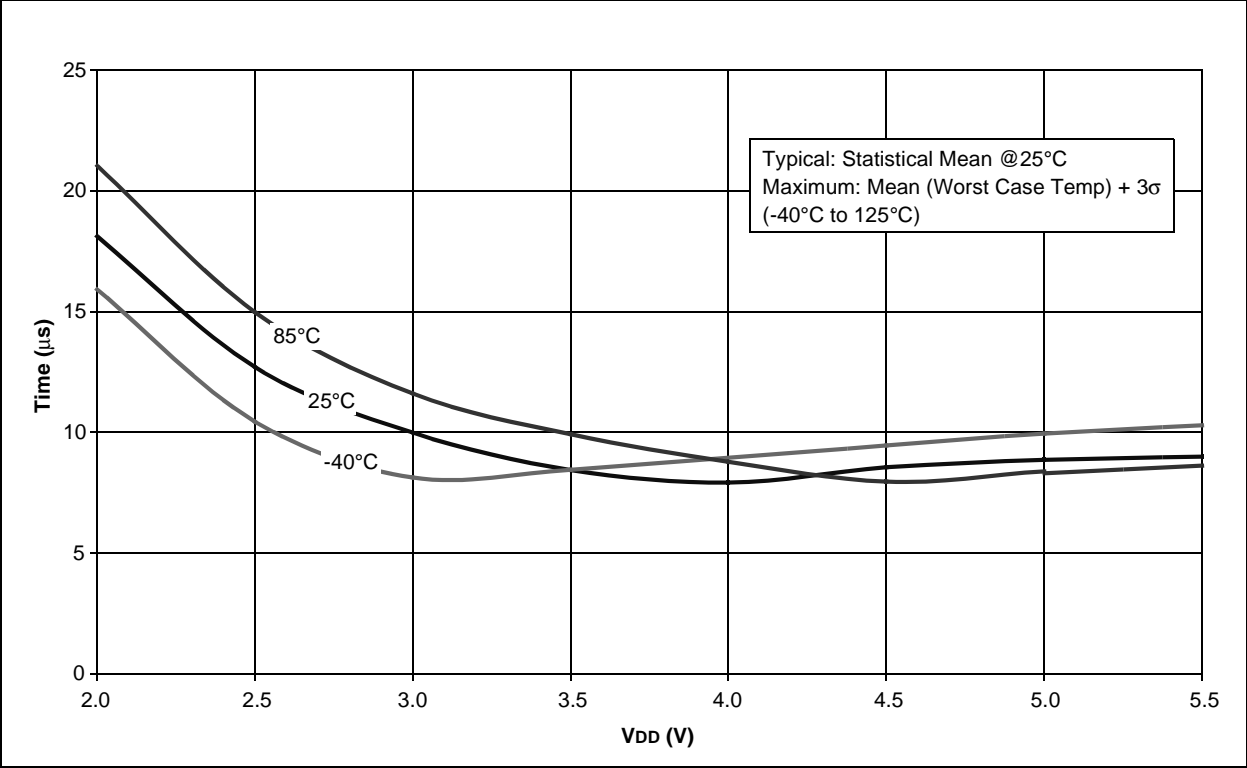
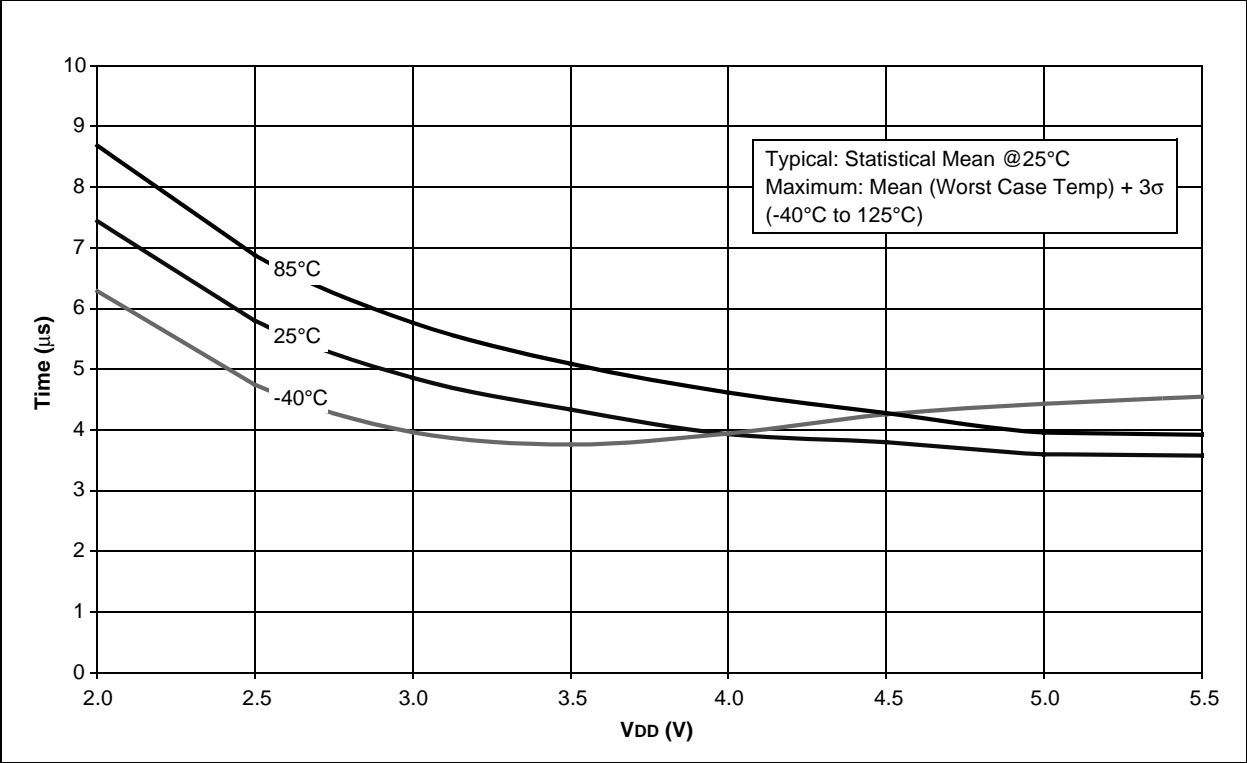


FIGURE 16-35: MINIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE





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