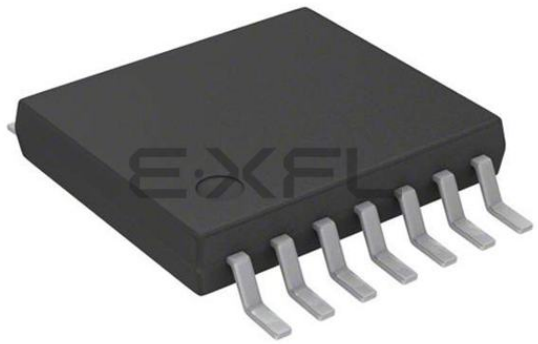

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f636t-i-st

3.5.2.1 OSCTUNE Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-2).

The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

REGISTER 3-2: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

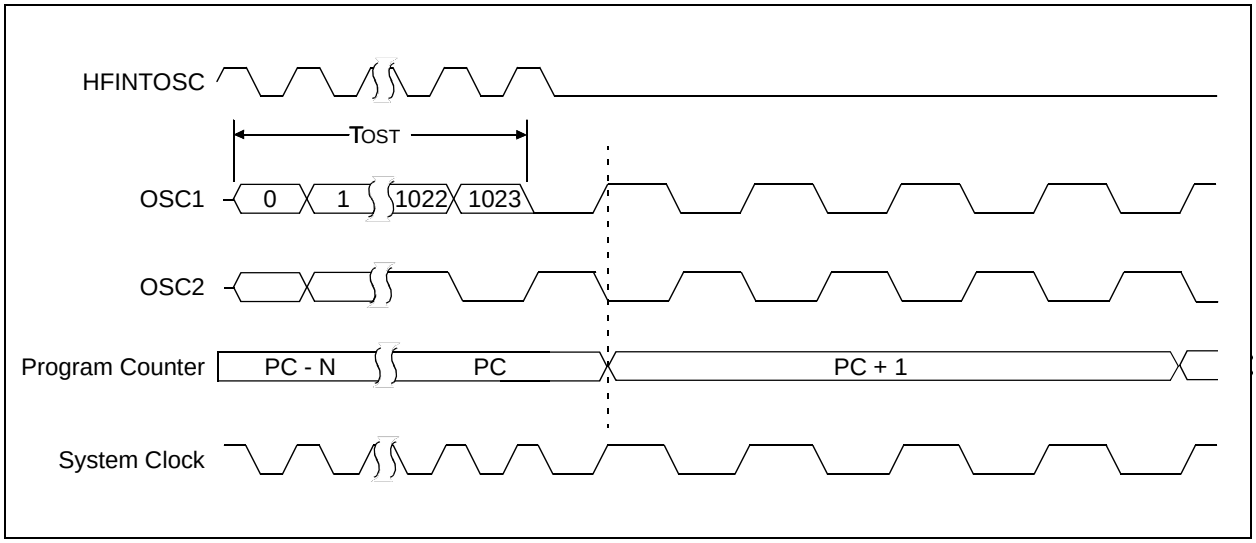
bit 4-0 **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Oscillator module is running at the calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

3.7.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCCON register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or the internal oscillator.

FIGURE 3-7: TWO-SPEED START-UP



REGISTER 4-1: PORTA: PORTA REGISTER

U-0	U-0	R/W-x	R/W-x	R-x	R/W-x	R/W-x	R/W-x
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **RA<5:0>**: PORTA I/O Pin bit
1 = Port pin is > V_{IH}
0 = Port pin is < V_{IL}

REGISTER 4-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bits
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

Note 1: TRISA<3> always reads '1'.
2: TRISA<5:4> always reads '1' in XT, HS and LP Oscillator modes.

4.3 PORTC

PORTC is a general purpose I/O port consisting of 6 bidirectional pins. The pins can be configured for either digital I/O or analog input to comparator. For specific information about individual functions, refer to the appropriate section in this data sheet.

Note:	The CMCON0 register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 4-3: INITIALIZING PORTC

```
BANKSEL PORTC          ;
CLRF    PORTC          ;Init PORTC
MOVLW   07h            ;Set RC<4,1:0> to
MOVWF   CMCON0         ;digital I/O
BANKSEL TRISC          ;
MOVLW   0Ch            ;Set RC<3:2> as inputs
MOVWF   TRISC          ;and set RC<5:4,1:0>
                       ;as outputs
```

REGISTER 4-6: PORTC: PORTC REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-0	R/W-0
—	—	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **RC<5:0>:** PORTC General Purpose I/O Pin bits
1 = Port pin is > V_{IH}
0 = Port pin is < V_{IL}

REGISTER 4-7: TRISC: PORTC TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **TRISC<5:0>:** PORTC Tri-State Control bits
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	00-- --10
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIE1	EEIE	LVDIE	CRIE	C2IE(1)	C1IE	OSFIE	—	TMR1IE	000- 00-0	000- 00-0
PIR1	EEIF	LVDIF	CRIF	C2IF(1)	C1IF	OSFIF	—	TMR1IF	000- 00-0	000- 00-0
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.
Note 1: PIC16F636/639 only.

7.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The comparators are very useful mixed signal building blocks because they provide analog functionality independent of the program execution. The Analog Comparator module includes the following features:

- Dual comparators (PIC16F636/639 only)
- Multiple comparator configurations
- Comparator(s) output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Timer1 gate (count enable)
- Output synchronization to Timer1 clock input
- Programmable voltage reference

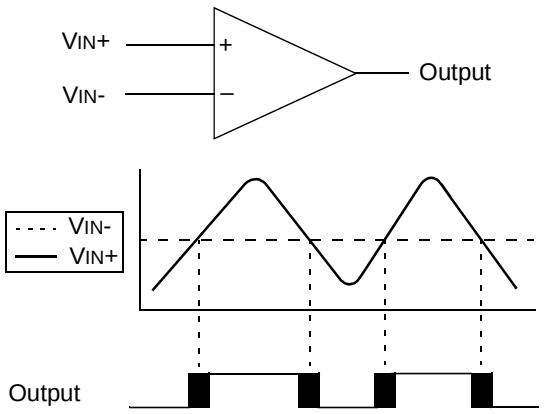
7.1 Comparator Overview

A comparator is shown in Figure 7-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The PIC12F635 contains a single comparator as shown in Figure 7-2.

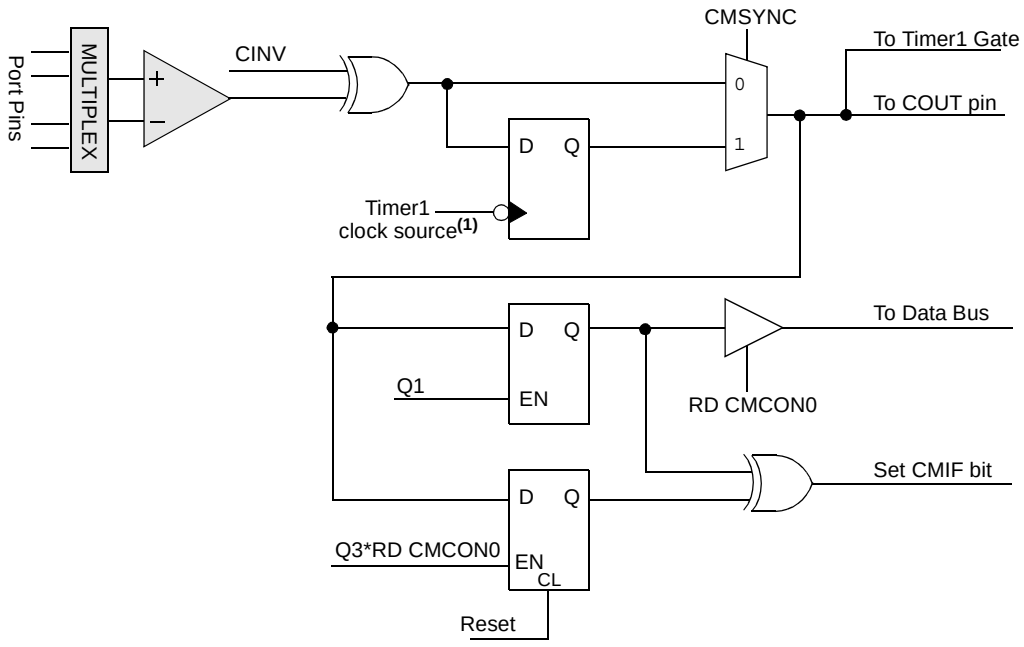
The PIC16F636/639 devices contains two comparators as shown in Figure 7-3 and Figure 7-4. The comparators are not independently configurable.

FIGURE 7-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

FIGURE 7-2: COMPARATOR OUTPUT BLOCK DIAGRAM (PIC12F635)



Note 1: Comparator output is latched on falling edge of Timer1 clock source.

2: Q1 and Q3 are phases of the four-phase system clock (FOSC).

3: Q1 is held high during Sleep mode.

7.9 Comparator Gating Timer1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CMCON1 register will enable Timer1 to increment based on the output of the comparator (or Comparator C2 for PIC16F636/639). This requires that Timer1 is on and gating is enabled. See **Section 6.0 "Timer1 Module with Gate Control"** for details.

It is recommended to synchronize the comparator with Timer1 by setting the CxSYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

Note:	References to the comparator in this section specifically are referring to Comparator C2 on the PIC16F636/639.

7.10 Synchronizing Comparator Output to Timer1

The comparator (or Comparator C2 for PIC16F636/639) output can be synchronized with Timer1 by setting the CxSYNC bit of the CMCON1 register. When enabled, the comparator output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 7-2) and the Timer1 Block Diagram (Figure 6-1) for more information.

Note:	References to the comparator in this section specifically are referring to Comparator C2 on the PIC16F636/639.

REGISTER 7-3: CMCON1: COMPARATOR CONFIGURATION REGISTER (PIC12F635)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
—	—	—	—	—	—	T1GSS	CMSYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **T1GSS:** Timer1 Gate Source Select bit(1)
- 1 = Timer1 Gate Source is $\overline{T1G}$ pin (pin should be configured as digital input)
- 0 = Timer1 Gate Source is comparator output

bit 0 **CMSYNC:** Comparator Output Synchronization bit(2)
- 1 = Output is synchronized with falling edge of Timer1 clock
- 0 = Output is asynchronous

Note 1: Refer to **Section 6.6 "Timer1 Gate"**.
2: Refer to Figure 7-2.

REGISTER 7-4: CMCON1: COMPARATOR CONFIGURATION REGISTER (PIC16F636/639)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
—	—	—	—	—	—	T1GSS	C2SYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **T1GSS:** Timer1 Gate Source Select bit(1)
- 1 = Timer1 gate source is $\overline{T1G}$ pin (pin should be configured as digital input)
- 0 = Timer1 gate source is Comparator C2 output

bit 0 **C2SYNC:** Comparator C2 Output Synchronization bit(2)
- 1 = Output is synchronized with falling edge of Timer1 clock
- 0 = Output is asynchronous

Note 1: Refer to **Section 6.6 "Timer1 Gate"**.
2: Refer to Figure 7-4.

8.0 PROGRAMMABLE LOW-VOLTAGE DETECT (PLVD) MODULE

The Programmable Low-Voltage Detect (PLVD) module is a power supply detector which monitors the internal power supply. This module is typically used in key fobs and other devices, where certain actions need to be taken as a result of a falling battery voltage.

The PLVD module includes the following capabilities:

- Eight programmable trip points
- Interrupt on falling VDD
- Stable reference indication
- Operation during Sleep

A Block diagram of the PLVD module is shown in Figure 8-1.

FIGURE 8-1: PLVD BLOCK DIAGRAM

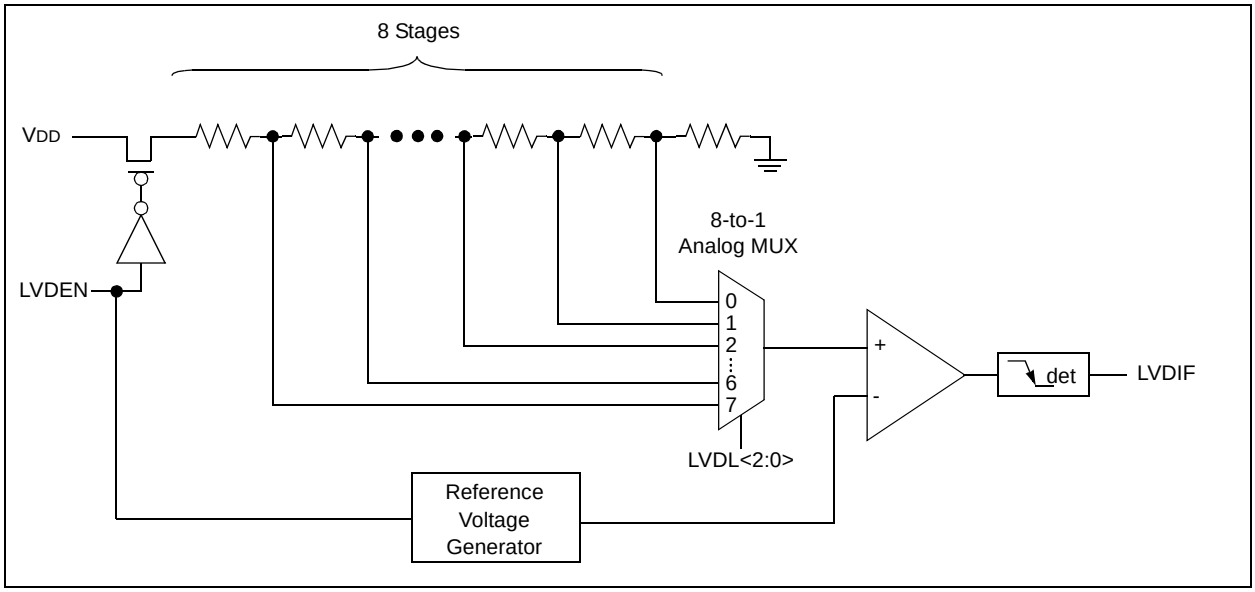
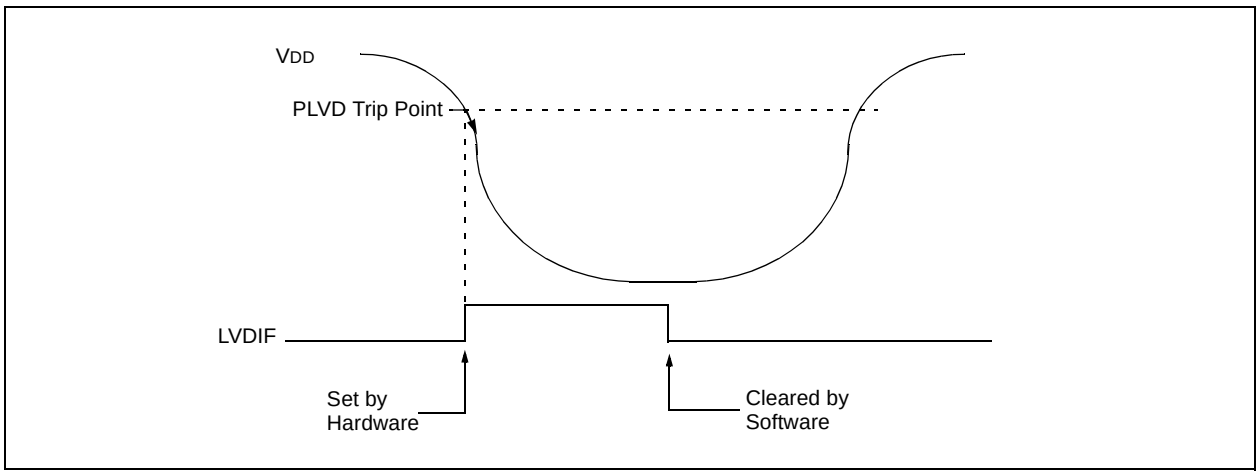


FIGURE 8-2: PLVD OPERATION



11.15 Configurable Output Enable Filter

The purpose of this filter is to enable the LFDATA output and wake the microcontroller only after receiving a specific sequence of pulses on the LC input pins. Therefore, it prevents the AFE from waking up the microcontroller due to noise or unwanted input signals. The circuit compares the timing of the demodulated header waveform with a pre-defined value, and enables the demodulated LFDATA output when a match occurs.

The output enable filter consists of a high (TOEH) and low duration (TOEL) of a pulse immediately after the AGC settling gap time. The selection of high and low times further implies a max period time. The output enable high and low times are determined by SPI interface programming. Figure 11-5 and Figure 11-6 show the output enable filter waveforms.

There should be no missing cycles during TOEH. Missing cycles may result in failing the output enable condition.

FIGURE 11-5: OUTPUT ENABLE FILTER TIMING

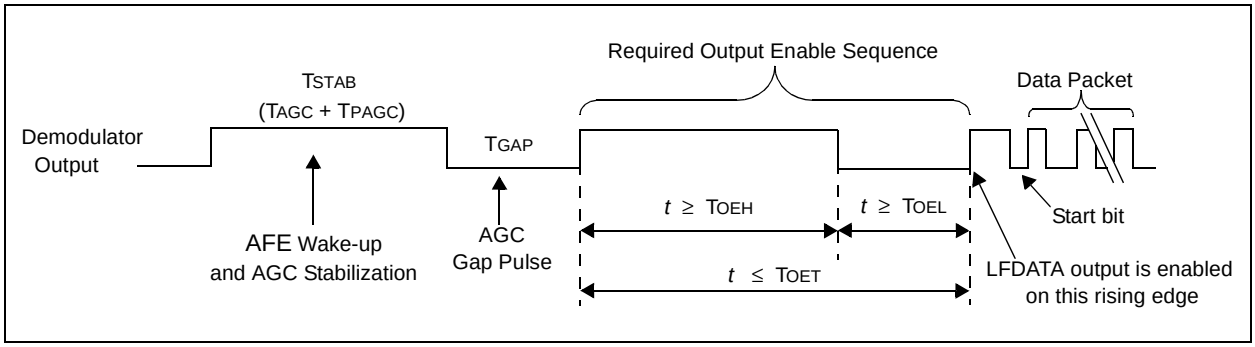
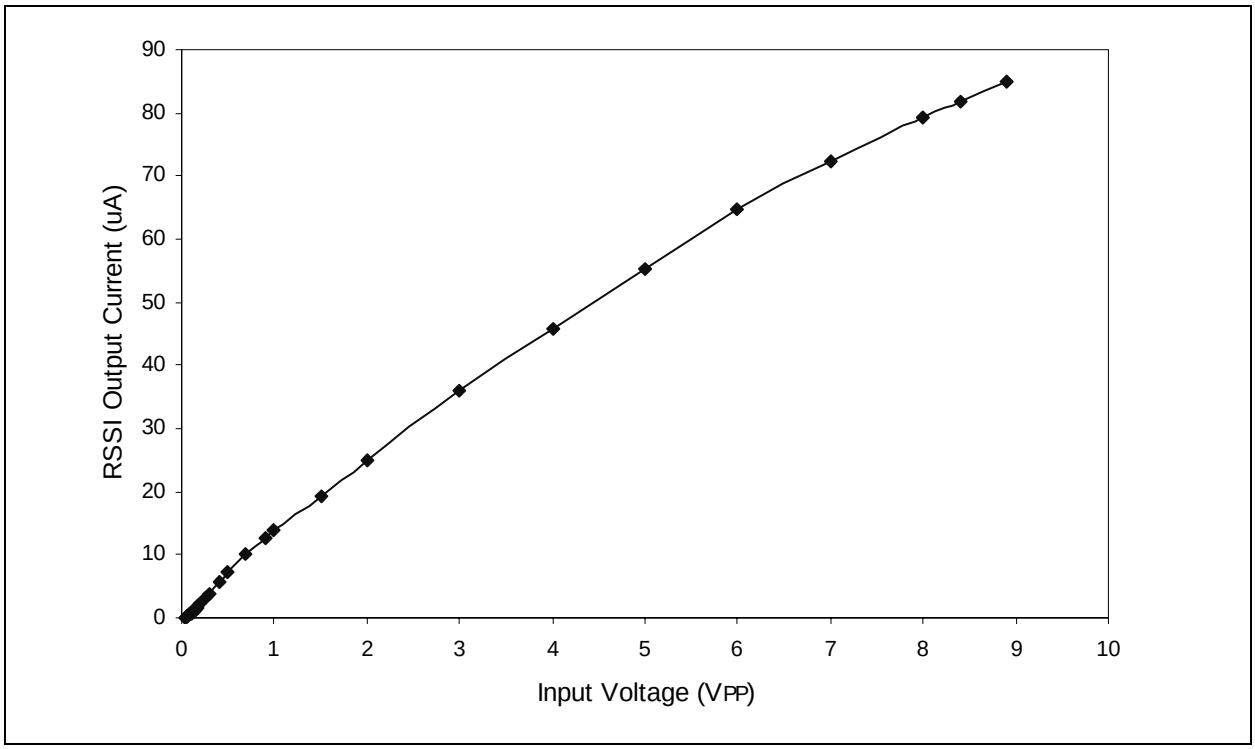


FIGURE 11-15: RSSI OUTPUT CURRENT VS. INPUT SIGNAL LEVEL EXAMPLE



REGISTER 12-2: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-1 **WDTPS<3:0>:** Watchdog Timer Period Select bits

Bit Value = Prescale Rate

0000 = 1:32
0001 = 1:64
0010 = 1:128
0011 = 1:256
0100 = 1:512 (Reset value)
0101 = 1:1024
0110 = 1:2048
0111 = 1:4096
1000 = 1:8192
1001 = 1:16384
1010 = 1:32768
1011 = 1:65536
1100 = Reserved
1101 = Reserved
1110 = Reserved
1111 = Reserved

bit 0 **SWDTEN:** Software Enable or Disable the Watchdog Timer bit(1)

1 = WDT is turned on
0 = WDT is turned off (Reset value)

Note 1: If WDTE Configuration bit = 1, then WDT is always enabled, irrespective of this control bit. If WDTE Configuration bit = 0, then it is possible to turn WDT on/off with this control bit.

TABLE 12-8: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
WDTCON	—	—	—	WDTPS3	WDTPS2	WSTPS1	WDTPS0	SWDTEN	---0 1000	---0 1000
OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
CONFIG	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—

Legend: Shaded cells are not used by the Watchdog Timer.
Note 1: See Register 12-1 for operation of all Configuration Word register bits.

14.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

14.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

14.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart® battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest *"Product Selector Guide"* (DS00148) for the complete list of demonstration, development and evaluation kits.

15.7 DC Characteristics: PIC16F639-I (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial Supply Voltage 2.0V ≤ VDD ≤ 3.6V				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports:					
D030A		with TTL buffer	VSS	—	0.15 VDD	V	
D031		with Schmitt Trigger buffer	VSS	—	0.2 VDD	V	
D032		$\overline{MCLR}$, OSC1 (RC mode)	VSS	—	0.2 VDD	V	
D033		OSC1 (XT and LP modes)(1)	VSS	—	0.3	V	
D033A		OSC1 (HS mode)(1)	VSS	—	0.3 VDD	V	
D034		**Digital Input Low Voltage**	VSS	—	0.3 VDD	V	Analog Front-End section
	VIH	**Input High Voltage**					
		I/O ports:					
D040		with TTL buffer					
D040A			(0.25 VDD + 0.8)	—	VDD	V	
D041		with Schmitt Trigger buffer	0.8 VDD	—	VDD	V	
D042		$\overline{MCLR}$	0.8 VDD	—	VDD	V	
D043		OSC1 (XT and LP modes)	1.6	—	VDD	V	**(Note 1)**
D043A		OSC1 (HS mode)	0.7 VDD	—	VDD	V	**(Note 1)**
D043B		OSC1 (RC mode)	0.9 VDD	—	VDD	V	
		Digital Input High Voltage					Analog Front-End section
D044		SCLK, $\overline{CS}$, SDIO for Analog Front-End (AFE)	0.8 VDD	—	VDD	V	
	IIL	**Input Leakage Current(2)**					
D060		I/O ports	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D060A		Analog inputs	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD
D060B		VREF	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD
D061		$\overline{MCLR}$(3)	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration
		Digital Input Leakage Current(2)					VDD = 3.6V, Analog Front-End section
D064		SDI for Analog Front-End (AFE)	—	—	± 1	µA	VSS ≤ VPIN ≤ VDD
D064A		SCLK, $\overline{CS}$ for Analog Front-End (AFE)	—	—	± 1	µA	VPIN ≤ VDD
D070	IPUR	**PORTA Weak Pull-up Current**	50*	250	400	µA	VDD = 3.6V, VPIN = VSS
D071	IPDR	**PORTA Weak Pull-down Current**	50	250	400	µA	VDD = 3.6V, VPIN = VDD
	VOL	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 3.6V (Ind.)
D083		OSC2/CLKOUT (RC mode)	—	—	0.6	V	IOL = 1.6 mA, VDD = 3.6V (Ind.) IOL = 1.2 mA, VDD = 3.6V (Ext.)
		Digital Output Low Voltage					Analog Front-End section
D084		$\overline{ALERT}$, LFDATA/SDIO for Analog Front-End (AFE)	—	—	VSS + 0.4	V	IOL = 1.0 mA, VDD = 2.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 9.4.1 "Using the Data EEPROM"** for additional information

15.7 DC Characteristics: PIC16F639-I (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial Supply Voltage 2.0V ≤ VDD ≤ 3.6V				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VOH	**Output High Voltage**					
D090		I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 3.6V (Ind.)
D092		OSC2/CLKOUT (RC mode)	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 3.6V (Ind.) IOH = -1.0 mA, VDD = 3.6V (Ext.)
		Digital Output High Voltage					Analog Front-End (AFE) section
D093		LFDATA/SDIO for Analog Front-End (AFE)	VDD – 0.5	—	—	V	IOH = -400 µA, VDD = 2.0V
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	—	50*	pF	
D102	IULP	**Ultra Low-power Wake-up Current**	—	200	—	nA	
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh(1)	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

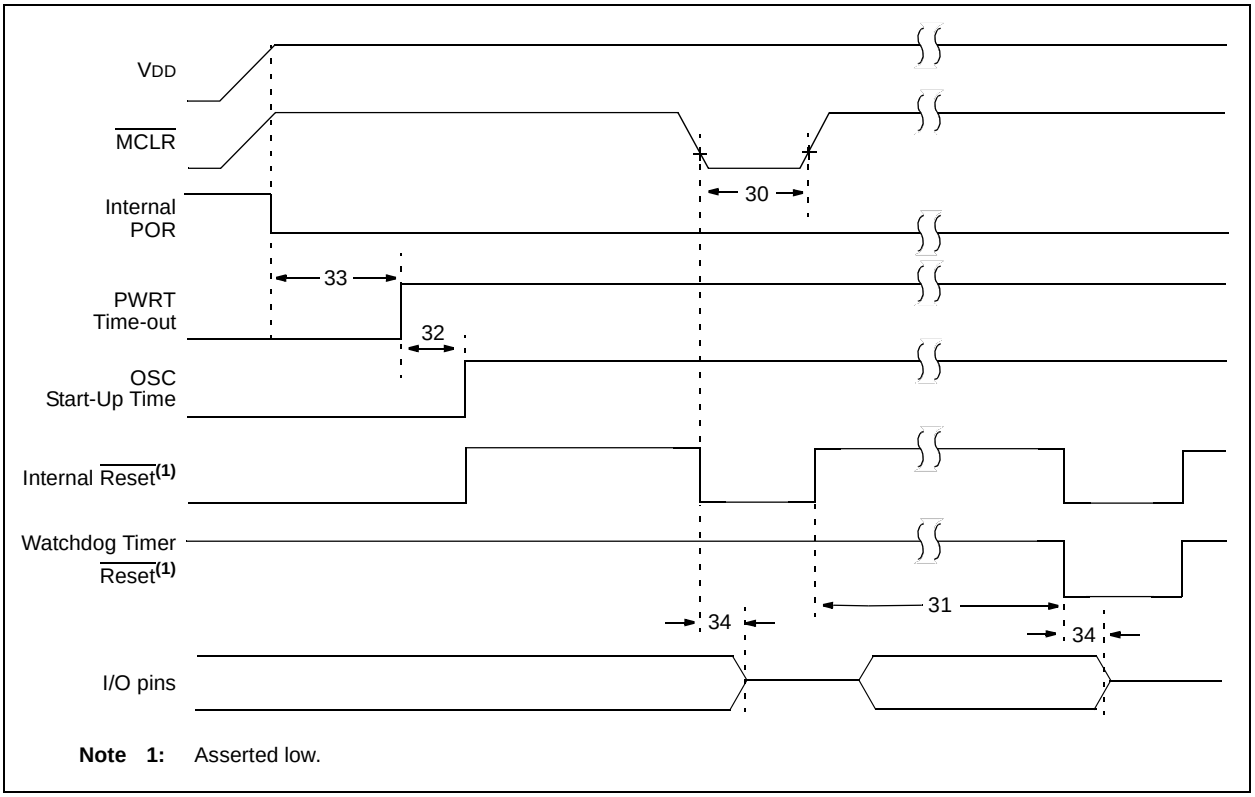
Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

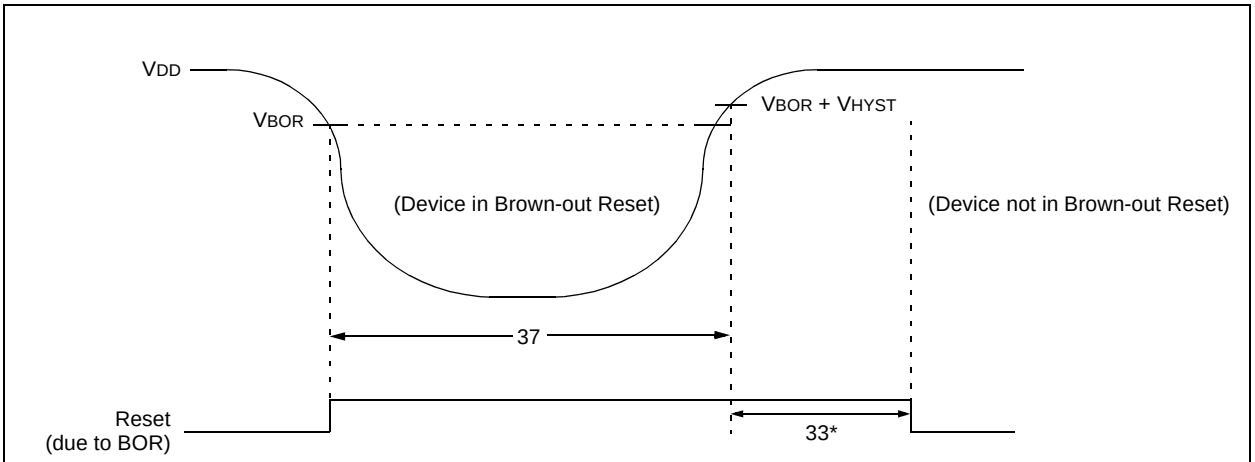
4: See **Section 9.4.1 "Using the Data EEPROM"** for additional information

FIGURE 15-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note 1: Asserted low.

FIGURE 15-8: BROWN-OUT RESET TIMING AND CHARACTERISTICS



* 64 ms delay only if $\overline{\text{PWRTE}}$ bit in the Configuration Word register is programmed to '0'.

TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
30	TMCL	$\overline{\text{MCLR}}$ Pulse Width (low)	2 5	— —	— —	µs µs	VDD = 5V, -40°C to +85°C VDD = 5V
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	10 10	16 16	29 31	ms ms	VDD = 5V, -40°C to +85°C VDD = 5V
32	TOST	Oscillation Start-up Timer Period**(1, 2)**	—	1024	—	TOSC	**(NOTE 3)**
33*	TPWRT	Power-up Timer Period	40	65	140	ms	
34*	TIOZ	I/O High-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	—	2.0	µs	
35	VBOR	Brown-out Reset Voltage	2.0	—	2.2	V	**(NOTE 4)**
36*	VHYST	Brown-out Reset Hysteresis	—	50	—	mV	
37*	TBOR	Brown-out Reset Minimum Detection Period	100	—	—	µs	VDD ≤ VBOR

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

2: By design.

3: Period of the slower clock.

4: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

15.11 AC Characteristics: Analog Front-End for PIC16F639 (Industrial) (Continued)

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Supply Voltage 2.0V ≤ VDD ≤ 3.6V Operating temperature -40°C ≤ TAMB ≤ +85°C for industrial LC Signal Input Sinusoidal 300 mVPP Carrier Frequency 125 kHz LCCOM connected to VSS				
Param No.	**Sym.**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
AF14	TLFDATAR	Rise time of LFDATA	—	0.5	—	µs	VDD = 3.0V Time is measured from 10% to 90% of amplitude
AF15	TLFDATAF	Fall time of LFDATA	—	0.5	—	µs	VDD = 3.0V Time is measured from 10% to 90% of amplitude
AF16	TAGC	AGC initialization time	—	3.5*	—	ms	Time required for AGC stabilization
AF17	TPAGC	High time after AGC settling time	—	62.5	—	µs	Equivalent to two Internal clock cycle (FOSC)
AF18	TSTAB	AGC stabilization time plus high time (after AGC settling time) (TAGC + TPAGC)	4	—	—	ms	AGC stabilization time
AF19	TGAP	Gap time after AGC settling time	200	—	—	µs	Typically 1 TE
AF20	TRDY	Time from exiting Sleep or POR to being ready to receive signal	—	—	50*	ms	
AF21	TPRES	Minimum time AGC level must be held after receiving AGC Preserve command	5*	—	—	ms	AGC level must not change more than 10% during TPRES.
AF22	FOSC	Internal RC oscillator frequency (±10%)	28.8	32	35.2	kHz	Internal clock trimmed at 32 kHz during test
AF23	TINACT	Inactivity timer time-out	14.4	16	17.6	ms	512 cycles of RC oscillator @ FOSC
AF24	TALARM	Alarm timer time-out	28.8	32	35.2	ms	1024 cycles of RC oscillator @ FOSC
AF25	RLC	**LC Pin Input Impedance** LCX, LCY, LCZ	—	1*	—	MOhm	Device in Standby mode
AF26	CIN	**LC Pin Input Capacitance** LCX, LCY, LCZ	—	24	—	pF	LCCOM grounded. Vdd = 3.0V, FCARRIER = 125 kHz
AF27	TE	Time element of pulse	100	—	—	µs	
AF28	TOEH	Minimum output enable filter high time **OEH (Bits Config0<7:6>)** 01 = 1 ms 10 = 2 ms 11 = 4 ms 00 = Filter Disabled	 32 (~1ms) 64 (~2ms) 128 (~4ms) —	 — — — —	 — — — —	 clock count	RC oscillator = FOSC Viewed from the pin input: **(Note 1)**
AF29	TOEL	Minimum output enable filter low time **OEL (Bits Config0<5:4>)** 00 = 1 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms	 32 (~1ms) 32 (~1ms) 64 (~2ms) 128 (~4ms)	 — — — —	 — — — —	 clock count	RC oscillator = FOSC Viewed from the pin input: **(Note 2)**

* Parameter is characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Required output enable filter high time must account for input path analog delays (= **TOEH** - TDR + TDF).

2: Required output enable filter low time must account for input path analog delays (= **TOEL** + TDR - TDF).

FIGURE 16-28: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

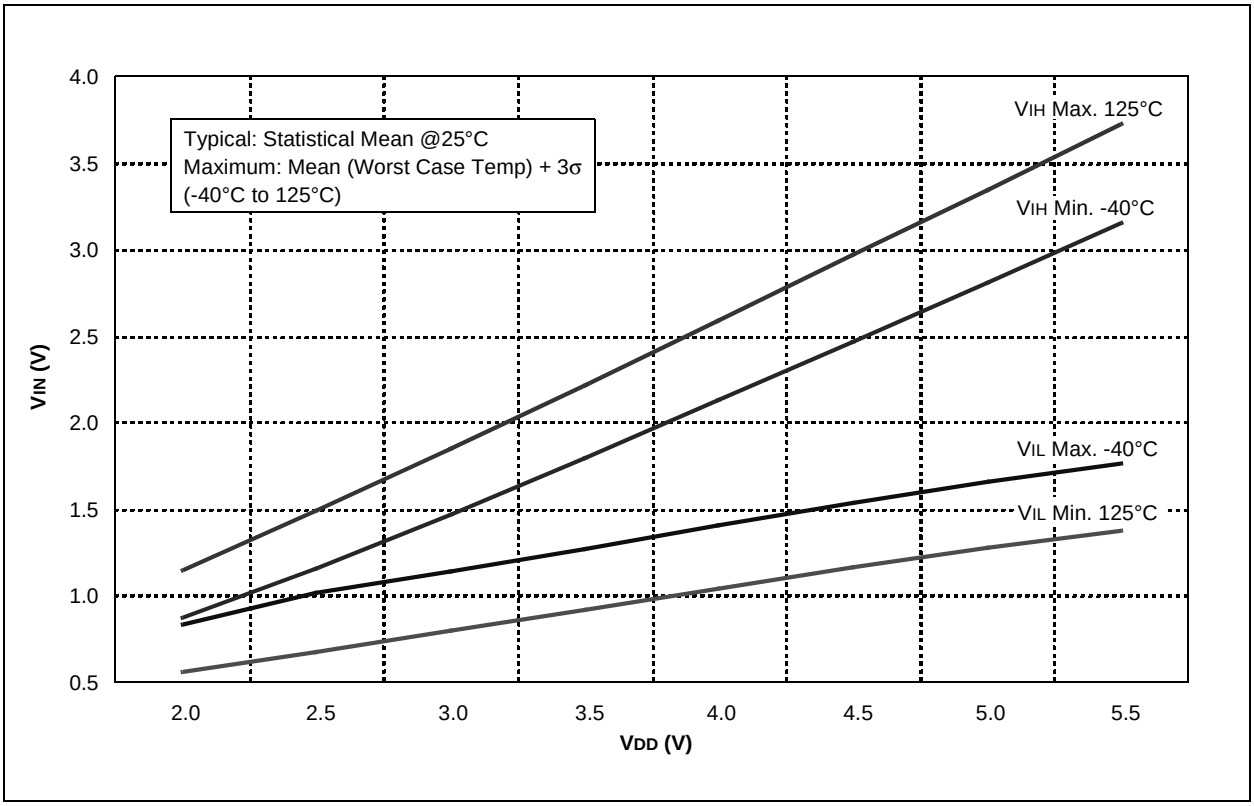
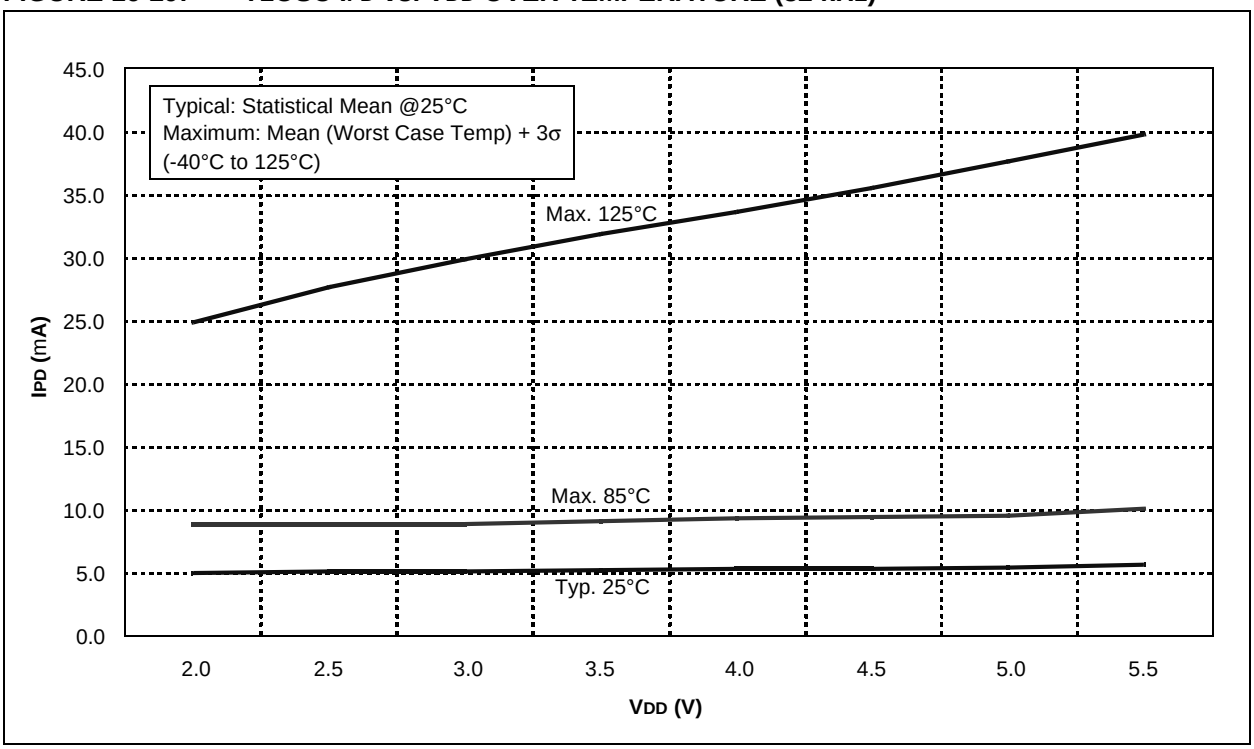
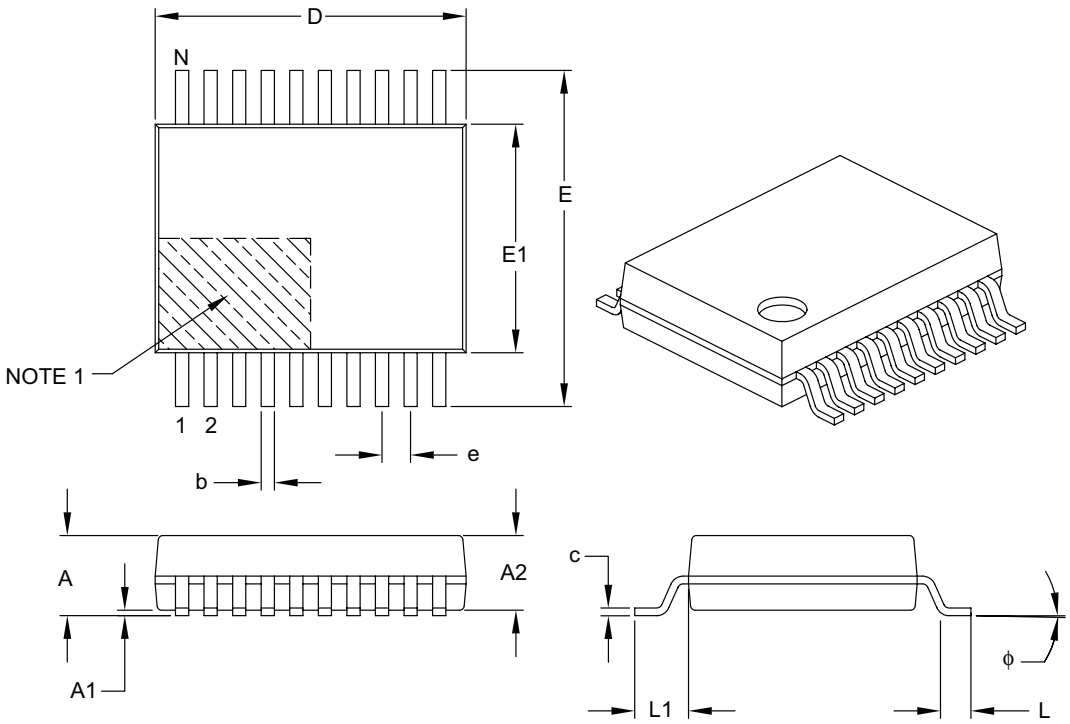


FIGURE 16-29: T1OSC IPD vs. VDD OVER TEMPERATURE (32 kHz)



20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B