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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f639-i-p

TABLE 2-2: PIC12F635 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR/ WUR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32,137
81h	OPTION_REG	$\overline{RAPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	63,137
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	32,137
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	26,137
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	32,137
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	32,137
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(3)	0000 000x	28,137
8Ch	PIE1	EEIE	LVDIE	CRIE	—	C1IE	OSFIE	—	TMR1IE	000- 00-0	29,137
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	ULPWUE	SBOREN	$\overline{WUR}$	—	$\overline{POR}$	$\overline{BOR}$	--01 q-qq	31,137
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	36,137
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	40,137
91h	—	Unimplemented								—	—
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -000	--00 -000
95h	WPUDA(2)	—	—	WPUDA5	WPUDA4	—	WPUDA2	WPUDA1	WPUDA0	--11 -111	--11 -111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
97h	WDA(2)	—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0	--11 -111	--11 -111
9Bh	—	Unimplemented								—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
9Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----
9Eh	—	Unimplemented								—	—
9Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: GP3 pull-up is enabled when pin is configured as $\overline{MCLR}$ in the Configuration Word register.

3: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset, but will set again if the mismatch exists.

2.2.2.4 PIE1 Register

The PIE1 register contains the interrupt enable bits, as shown in Register 2-4.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
EEIE	LVDIE	CRIE	C2IE(1)	C1IE	OSFIE	—	TMR1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EEIE**: EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 6 **LVDIE**: Low-Voltage Detect Interrupt Enable bit
1 = Enables the LVD interrupt
0 = Disables the LVD interrupt

bit 5 **CRIE**: Cryptographic Interrupt Enable bit
1 = Enables the cryptographic interrupt
0 = Disables the cryptographic interrupt

bit 4 **C2IE**: Comparator 2 Interrupt Enable bit(1)
1 = Enables the Comparator 2 interrupt
0 = Disables the Comparator 2 interrupt

bit 3 **C1IE**: Comparator 1 Interrupt Enable bit
1 = Enables the Comparator 1 interrupt
0 = Disables the Comparator 1 interrupt

bit 2 **OSFIE**: Oscillator Fail Interrupt Enable bit
1 = Enables the oscillator fail interrupt
0 = Disables the oscillator fail interrupt

bit 1 **Unimplemented**: Read as '0'

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

Note 1: PIC16F636/639 only.

REGISTER 4-3: WDA: WEAK PULL-UP/PULL-DOWN DIRECTION REGISTER

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-4 **WDA<5:4>**: Pull-up/Pull-down Selection bits
1 = Pull-up selected
0 = Pull-down selected

bit 3 **Unimplemented**: Read as '0'

bit 2-0 **WDA<2:0>**: Pull-up/Pull-down Selection bits
1 = Pull-up selected
0 = Pull-down selected

Note 1: The weak pull-up/pull-down device is enabled only when the global $\overline{\text{RAPU}}$ bit is enabled, the pin is in Input mode (TRIS = 1), the individual WDA bit is enabled (WDA = 1) and the pin is not configured as an analog input or clock function.

2: RA3 pull-up is enabled when the pin is configured as $\overline{\text{MCLR}}$ in the Configuration Word register and the device is not in Programming mode.

REGISTER 4-4: WPUDA: WEAK PULL-UP/PULL-DOWN ENABLE REGISTER

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPUDA5(3)	WPUDA4(3)	—	WPUDA2	WPUDA1	WPUDA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-4 **WPUDA<5:4>**: Pull-up/Pull-down Direction Selection bits(3)
1 = Pull-up/pull-down enabled
0 = Pull-up/pull-down disabled

bit 3 **Unimplemented**: Read as '0'

bit 2-0 **WPUDA<2:0>**: Pull-up/Pull-down Direction Selection bits
1 = Pull-up/pull-down enabled
0 = Pull-up/pull-down disabled

Note 1: The weak pull-up/pull-down direction device is enabled only when the global $\overline{\text{RAPU}}$ bit is enabled, the pin is in Input mode (TRIS = 1), the individual WPUDA bit is enabled (WPUDA = 1) and the pin is not configured as an analog input or clock function.

2: RA3 pull-up is enabled when the pin is configured as $\overline{\text{MCLR}}$ in the Configuration Word register and the device is not in Programming mode.

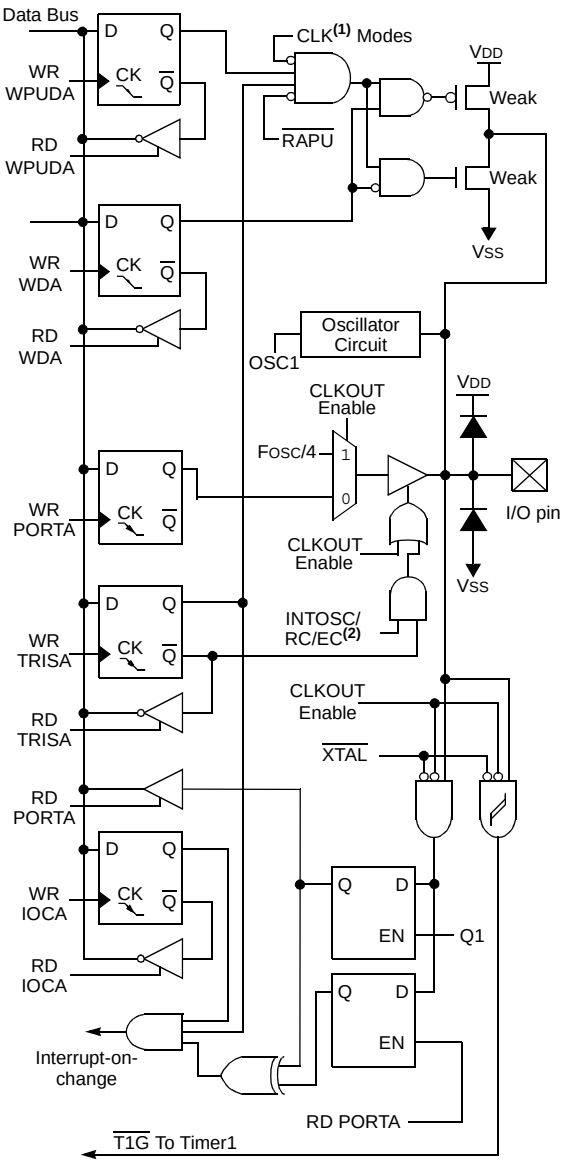
3: WPUDA5 bit can be written if INTOSC is enabled and T1OSC is disabled; otherwise, the bit can not be written and reads as '1'. WPUDA4 bit can be written if not configured as OSC2; otherwise, the bit can not be written and reads as '1'

4.2.4.5 RA4/$\overline{T1G}$/OSC2/CLKOUT

Figure 4-5 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 gate input
- a crystal/resonator connection
- a clock output

FIGURE 4-5: BLOCK DIAGRAM OF RA4



Note 1: Oscillator modes are XT, HS, LP, LPTMR1 and CLKOUT Enable.

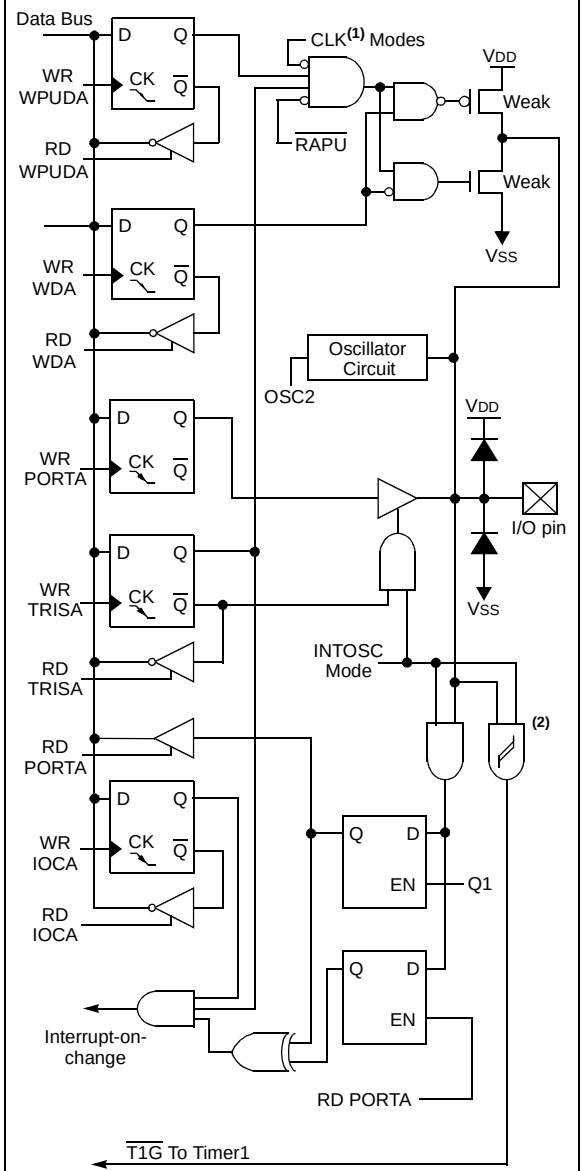
2: With CLKOUT option.

4.2.4.6 RA5/T1CKI/OSC1/CLKIN

Figure 4-6 shows the diagram for this pin. The RA5 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 clock input
- a crystal/resonator connection
- a clock input

FIGURE 4-6: BLOCK DIAGRAM OF RA5



Note 1: Oscillator modes are XT, HS, LP and LPTMR1.

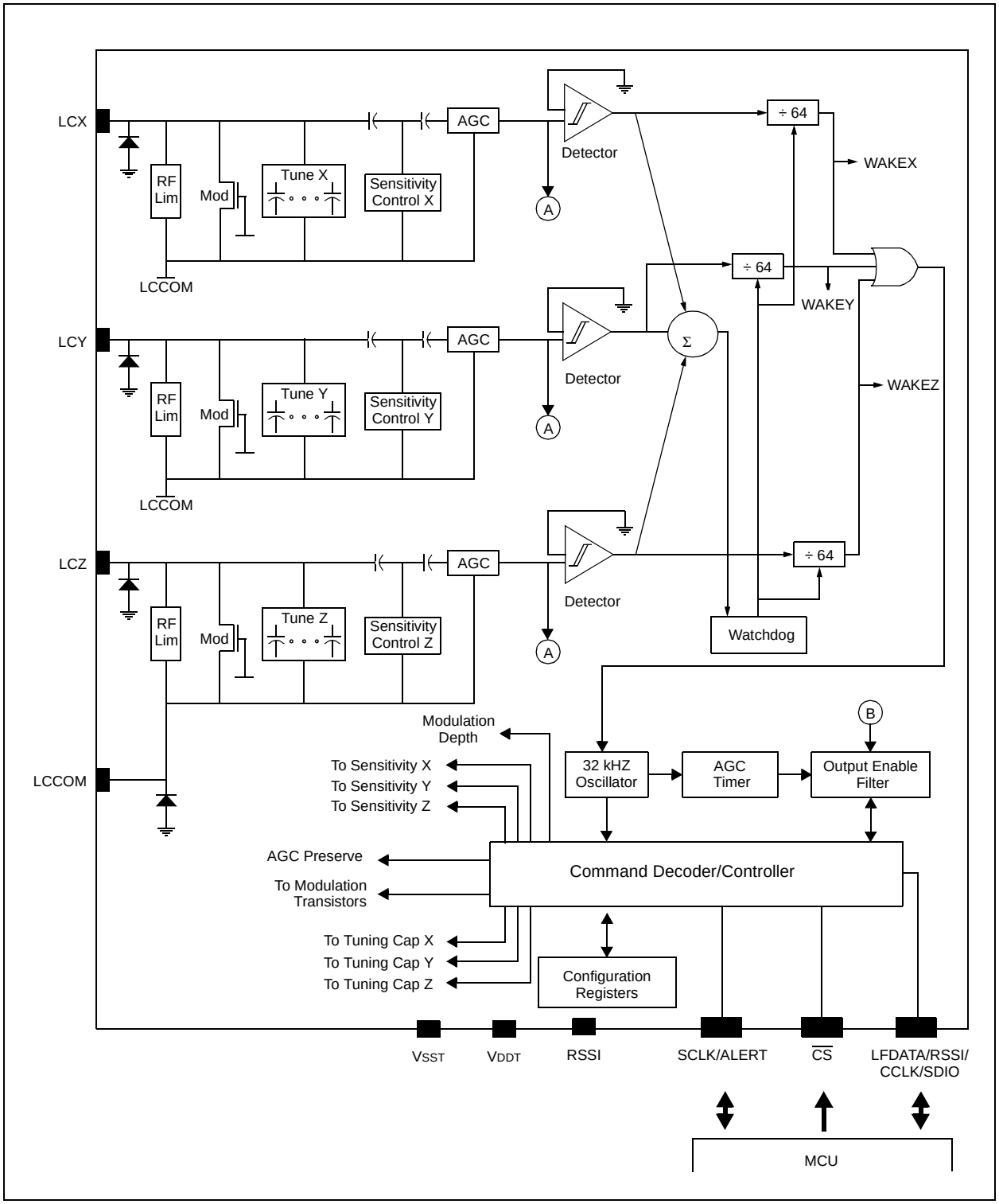
2: When using Timer1 with LP oscillator, the Schmitt Trigger is bypassed.

TABLE 7-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CMCON0	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	---- --10
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIE1	EEIE	LVDIE	CRIE	—	C1IE	OSFIE	—	TMR1IE	000- 00-0	000- 00-0
PIR1	EEIF	LVDIF	CRIF	—	C1IF	OSFIF	—	TMR1IF	000- 00-0	000- 00-0
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for comparator.

FIGURE 11-1: FUNCTIONAL BLOCK DIAGRAM – ANALOG FRONT-END



11.26 Factory Calibration

Microchip calibrates the AFE to reduce the device-to-device variation in standby current, internal timing and sensitivity, as well as channel-to-channel sensitivity variation.

11.27 De-Q'ing of Antenna Circuit

When the transponder is close to the base station, the transponder coil may develop coil voltage higher than V_{DE_Q}. This condition is called "near field". The AFE detects the strong near field signal through the AGC control, and de-Q'ing the antenna circuit to reduce the input signal amplitude.

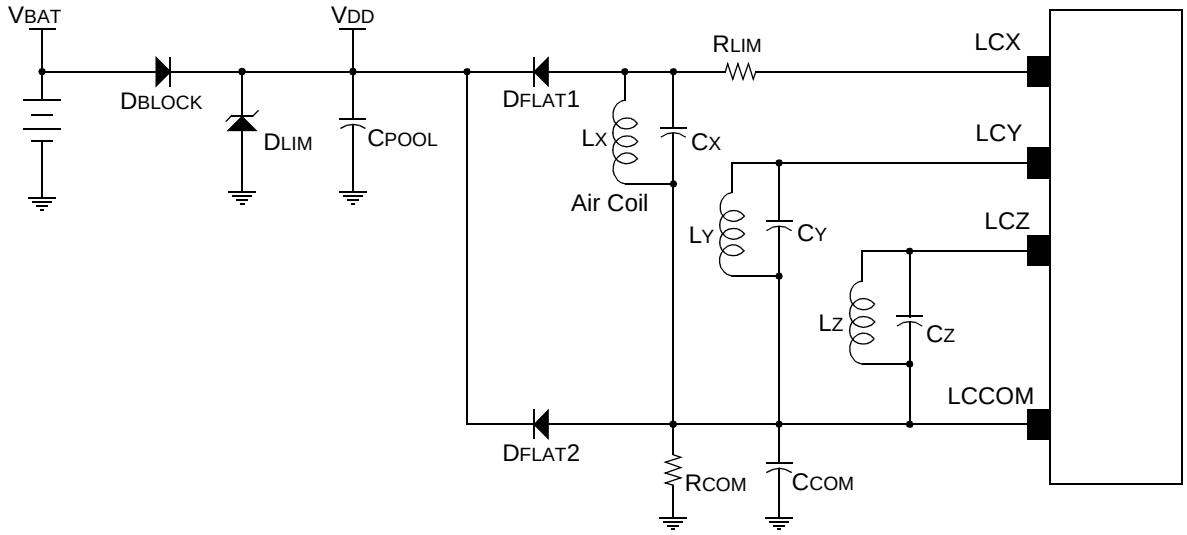
11.28 Battery Back-up and Batteryless Operation

The device supports both battery back-up and batteryless operation by the addition of external components, allowing the device to be partially or completely powered from the field.

Figure 11-8 shows an example of the external circuit for the battery back-up.

Note:	Voltage on LCCOM combined with coil input voltage must not exceed the maximum LC input voltage.

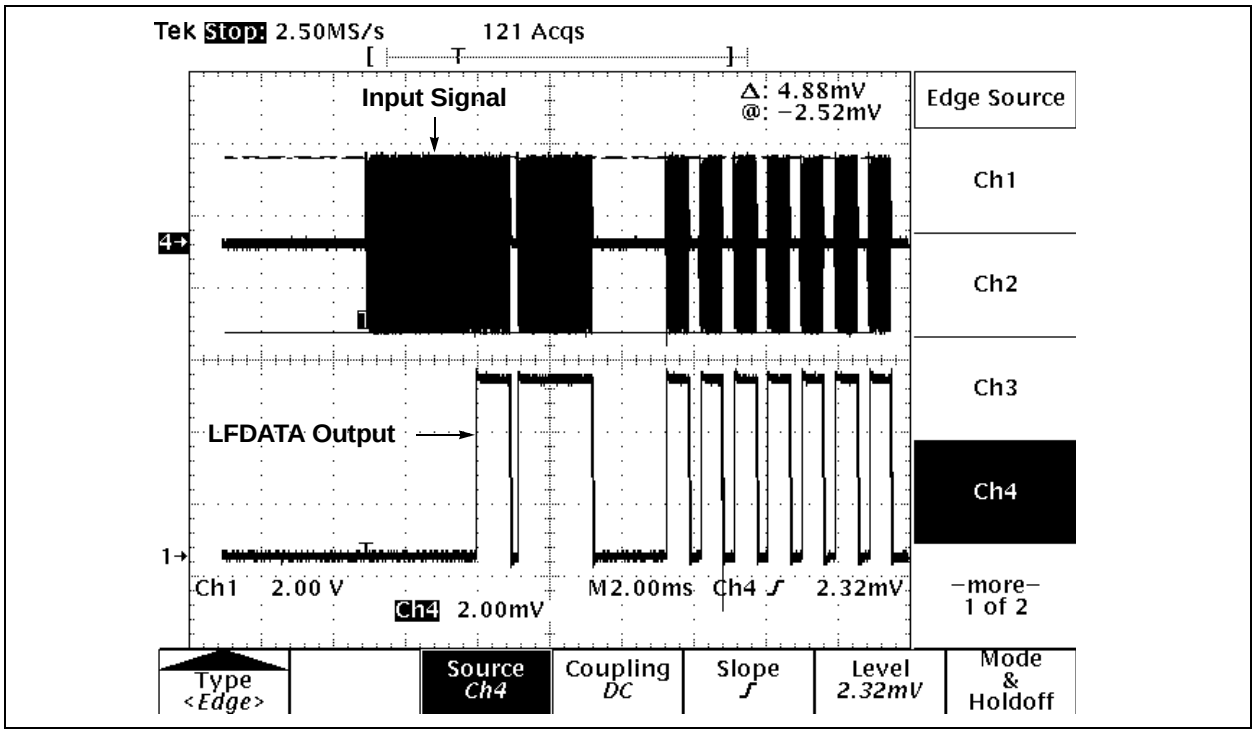
FIGURE 11-8: LF FIELD POWERING AND BATTERY BACK-UP EXAMPLE



Legend:
- C_{COM} = LCCOM charging capacitor.
- C_{POOL} = Pool capacitor (or battery back-up capacitor), charges in field and powers device.
- D_{BLOCK} = Battery protection from reverse charge. Schottky for low forward bias drop.
- D_{FLAT} = Field rectifier diodes.
- D_{LIM} = Voltage limiting diode, may be required to limit V_{DD} voltage when in strong fields.
- R_{COM} = C_{COM} discharge path.
- R_{LIM} = Current limiting resistor, required for air coil in strong fields.

Case I. When Output Enable Filter is disabled: Demodulated output is available immediately after the AGC stabilization time (TAGC). Figure 11-10 shows an example of demodulated output when the Output Enable Filter is disabled.

FIGURE 11-10: INPUT SIGNAL AND DEMODULATOR OUTPUT WHEN THE OUTPUT ENABLE FILTER IS DISABLED



Case II. When Output Enable Filter is enabled: Demodulated output is available only if the incoming signal meets the enable filter timing criteria that is defined in the Configuration Register 0 (Register 11-1). If the criteria is met, the output is available after the low timing (TOEL) of the Enable Filter. Figure 11-11 and Figure 11-12 shows examples of demodulated output when the Output Enable Filter is enabled.

11.31.3.1 ANALOG-TO-DIGITAL DATA CONVERSION OF RSSI SIGNAL

The AFE's RSSI output is an analog current. It needs an external Analog-to-Digital (ADC) data conversion device for digitized output. The ADC data conversion can be accomplished by using a stand-alone external ADC device or by firmware utilizing MCU's internal comparator along with a few external resistors and a capacitor. For slope ADC implementations, the external capacitor at the LFDATA pad needs to be discharged before data sampling. For this purpose, the internal pull-down MOSFET on the LFDATA pad can be utilized. The MOSFET can be turned on or off with bit RSSIFET<8> of the Configuration Register 2 (Register 11-3). When it is turned on, the internal MOSFET provides a discharge path for the external capacitor. This MOSFET option is valid only if RSSI output is selected and not controllable by users for demodulated or carrier clock output options.

See separate application notes for various external ADC implementation methods for this device.

11.32 AFE Configuration

11.32.1 SPI COMMUNICATION

The AFE SPI interface communication is used to read or write the AFE's Configuration registers and to send command only messages. For the SPI interface, the device has three pads; $\overline{CS}$, SCLK/$\overline{ALERT}$, and LFDATA/RSSI/CCLK/SDIO. Figure 11-15, Figure 11-14, Figure 11-16 and Figure 11-17 shows examples of the SPI communication sequences.

When the device powers up, these pins will be high-impedance inputs until firmware modifies them appropriately. The AFE pins connected to the MCU pins will be as follows.

$\overline{CS}$

- Pin is permanently an input with an internal pull-up.

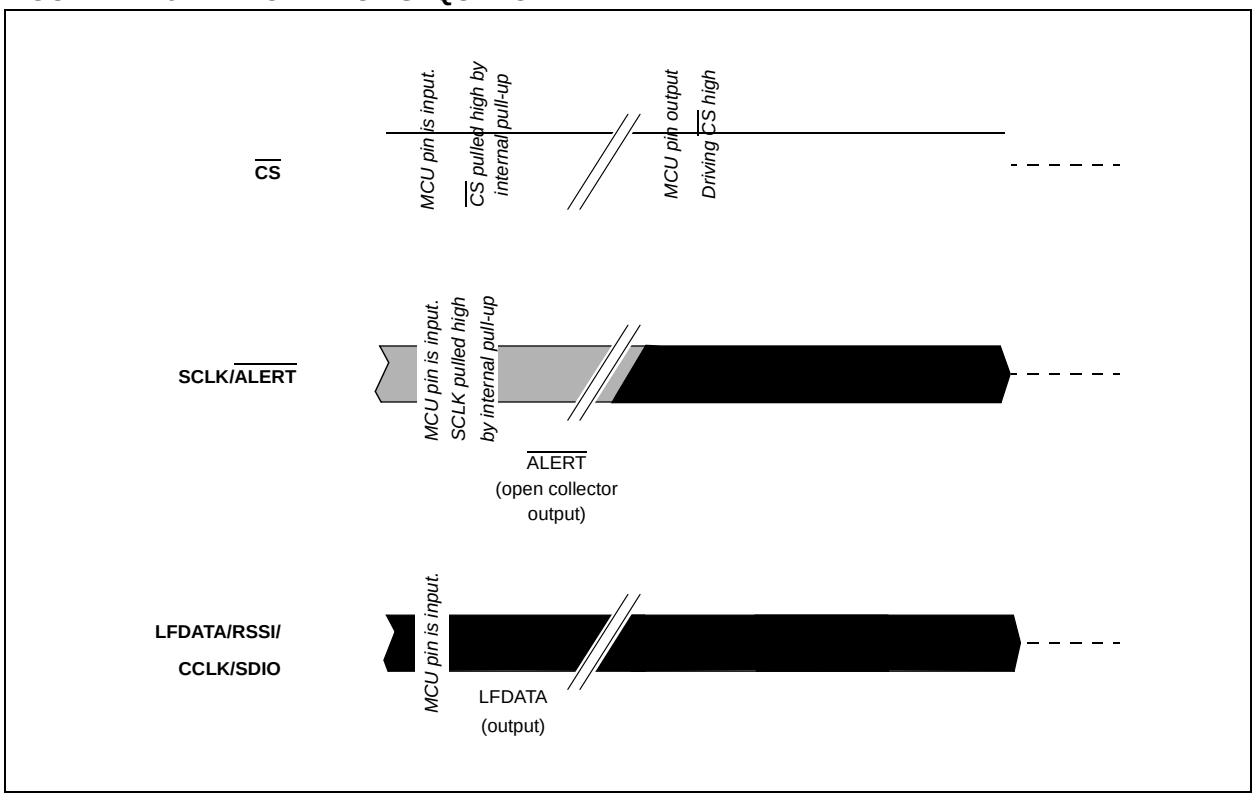
SCLK/$\overline{ALERT}$

- Pin is an open collector output when $\overline{CS}$ is high. An internal pull-up resistor exists internal to the AFE to ensure no spurious SPI communication between powering and the MCU configuring its pins. This pin becomes the SPI clock input when $\overline{CS}$ is low.

LFDATA/RSSI/CCLK/SDIO

- Pin is a digital output (LFDATA) so long as $\overline{CS}$ is high. During SPI communication, the pin is the SPI data input (SDI) unless performing a register Read, where it will be the SPI data output (SDO).

FIGURE 11-16: POWER-UP SEQUENCE



REGISTER 11-2: CONFIGURATION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATOUT1	DATOUT0	LCXTUN5	LCXTUN4	LCXTUN3	LCXTUN2	LCXTUN1	LCXTUN0	R1PAR
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8-7 **DATOUT<1:0>:** LFDATA Output type bit
00 = Demodulated output
01 = Carrier Clock output
10 = RSSI output
11 = RSSI output

bit 6-1 **LCXTUN<5:0>:** LCX Tuning Capacitance bit
000000 = +0 pF (Default)
:
111111 = +63 pF

bit 0 **R1PAR**: Register Parity Bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

REGISTER 11-3: CONFIGURATION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSSIFET	CLKDIV	LCYTUN5	LCYTUN4	LCYTUN3	LCYTUN2	LCYTUN1	LCYTUN0	R2PAR
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8 **RSSIFET**: Pull-down MOSFET on LFDATA pad bit (controllable by user in the RSSI mode only)
1 = Pull-down RSSI MOSFET on
0 = Pull-down RSSI MOSFET off

bit 7 **CLKDIV:** Carrier Clock Divide-by bit
1 = Carrier Clock/4
0 = Carrier Clock/1

bit 6-1 **LCYTUN<5:0>:** LCY Tuning Capacitance bit
000000 = +0 pF (Default)
:
111111 = +63 pF

bit 0 **R2PAR**: Register Parity Bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

REGISTER 11-8: AFE STATUS REGISTER 7

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CHZACT	CHYACT	CHXACT	AGCACT	WAKEZ	WAKEY	WAKEX	ALARM	PEI
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 8 **CHZACT**: Channel Z Active(1) bit (cleared via Soft Reset)
1 = Channel Z is passing data after TAGC
0 = Channel Z is not passing data after TAGC

bit 7 **CHYACT**: Channel Y Active(1) bit (cleared via Soft Reset)
1 = Channel Y is passing data after TAGC
0 = Channel Y is not passing data after TAGC

bit 6 **CHXACT**: Channel X Active(1) bit (cleared via Soft Reset)
1 = Channel X is passing data after TAGC
0 = Channel X is not passing data after TAGC

bit 5 **AGCACT**: AGC Active Status bit (real time, cleared via Soft Reset)
1 = AGC is active (Input signal is strong). AGC is active when input signal level is approximately > 20 mVPP range.
0 = AGC is inactive (Input signal is weak)

bit 4 **WAKEZ**: Wake-up Channel Z Indicator Status bit (cleared via Soft Reset)
1 = Channel Z caused a AFE wake-up (passed ÷64 clock counter)
0 = Channel Z did not cause a AFE wake-up

bit 3 **WAKEY**: Wake-up Channel Y Indicator Status bit (cleared via Soft Reset)
1 = Channel Y caused a AFE wake-up (passed ÷64 clock counter)
0 = Channel Y did not cause a AFE wake-up

bit 2 **WAKEX**: Wake-up Channel X Indicator Status bit (cleared via Soft Reset)
1 = Channel X caused a AFE wake-up (passed ÷64 clock counter)
0 = Channel X did not cause a AFE wake-up

bit 1 **ALARM**: Indicates whether an Alarm timer time-out has occurred (cleared via read "Status Register command")
1 = The Alarm timer time-out has occurred. It may cause the $\overline{\text{ALERT}}$ output to go low depending on the state of bit 4 of the Configuration register 0
0 = The Alarm timer is not timed out

bit 0 **PEI**: Parity Error Indicator bit – indicates whether a Configuration register parity error has occurred (real time)
1 = A parity error has occurred and caused the $\overline{\text{ALERT}}$ output to go low
0 = A parity error has not occurred

Note 1: Bit is high whenever channel is passing data. Bit is low in Standby mode.

See Table 11-7 for the bit conditions of the AFE Status Register after various SPI commands and the AFE Power-on Reset.

TABLE 11-7: AFE STATUS REGISTER BIT CONDITION (AFTER POWER-ON RESET AND VARIOUS SPI COMMANDS)

Condition	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CHZACT	CHYACT	CHXACT	AGCACT	WAKEZ	WAKEY	WAKEX	ALARM	PEI
POR	0	0	0	0	0	0	0	0	1
Read Command (STATUS Register only)	u	u	u	u	u	u	u	0	u
Sleep Command	u	u	u	u	u	u	u	u	u
Soft Reset Executed(1)	0	0	0	0	0	0	0	u	u

Legend: u = unchanged

Note 1: See **Section 11.20 "Soft Reset"** and **Section 11.32.2.4 "Soft Reset Command"** for the condition of Soft Reset execution.

12.3 Power-on Reset

The on-chip POR circuit holds the chip in Reset until V_{DD} has reached a high enough level for proper operation. To take advantage of the POR, simply connect the $\overline{MCLR}$ pin through a resistor to V_{DD}. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for V_{DD} is required. See **Section 15.0 "Electrical Specifications"** for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until V_{DD} reaches V_{BOD} (see **Section 12.6 "Brown-out Reset (BOR)"**).

Note:	The POR circuit does not produce an internal Reset when V_{DD} declines. To re-enable the POR, V_{DD} must reach V_{SS} for a minimum of 100 µs.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to the Application Note *AN607, "Power-up Trouble Shooting"* (DS00607).

12.4 Wake-up Reset (WUR)

The PIC12F635/PIC16F636/639 has a modified wake-up from Sleep mechanism. When waking from Sleep, the WUR function resets the device and releases Reset when V_{DD} reaches an acceptable level.

If the $\overline{WURE}$ bit is enabled ('0') in the Configuration Word register, the device will Wake-up Reset from Sleep through one of the following events:

1. On any event that causes a wake-up event. The peripheral must be enabled to generate an interrupt or wake-up, GIE state is ignored.
2. When WURE is enabled, RA3 will always generate an interrupt-on-change signal during Sleep.

The $\overline{WUR}$, $\overline{POR}$ and $\overline{BOR}$ bits in the PCON register and the $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device Reset.

To allow WUR upon RA3 change:

1. Enable the WUR function, $\overline{WURE}$ Configuration Bit = 0.
2. Enable RA3 as an input, MCLRE Configuration Bit = 0.
3. Read PORTA to establish the current state of RA3.
4. Execute SLEEP instruction.
5. When RA3 changes state, the device will wake-up and then reset. The $\overline{WUR}$ bit in PCON will be cleared to '0'.

12.4.1 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from the 31 kHz LFINTOSC oscillator. For more information, see **Section 3.5 "Internal Clock Modes"**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level. A Configuration bit, $\overline{PWRTE}$, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip due to:

- V_{DD} variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 15.0 "Electrical Specifications"**).

Note:	Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

12.5 $\overline{MCLR}$

PIC12F635/PIC16F636/639 has a noise filter in the $\overline{MCLR}$ Reset path. The filter will ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{MCLR}$ pin low. See Figure 12-2 for the recommended $\overline{MCLR}$ circuit.

An internal $\overline{MCLR}$ option is enabled by clearing the MCLRE bit in the Configuration Word register. When cleared, $\overline{MCLR}$ is internally tied to V_{DD} and an internal weak pull-up is enabled for the $\overline{MCLR}$ pin. In-Circuit Serial Programming is not affected by selecting the internal $\overline{MCLR}$ option.

12.9 Interrupts

The PIC12F635/PIC16F636/639 has multiple interrupt sources:

- External Interrupt RA2/INT
- Timer0 Overflow Interrupt
- PORTA Change Interrupts
- 2 Comparator Interrupts
- Timer1 Overflow Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Register 1 (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

A Global Interrupt Enable bit GIE of the INTCON register enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIE1 register. GIE is cleared on Reset.

The Return from Interrupt instruction, `RETFIE`, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- PORTA Change Interrupt
- TMR0 Overflow Interrupt

The peripheral interrupt flags are contained in the special register, PIR1. The corresponding interrupt enable bit is contained in special register, PIE1.

The following interrupt flags are contained in the PIR1 register:

- EEPROM Data Write Interrupt
- 2 Comparator Interrupts
- Timer1 Overflow Interrupt
- Fail-Safe Clock Monitor Interrupt

When an interrupt is serviced:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

For external interrupt events, such as the INT pin or PORTA change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 12-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.
2:	When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, comparators or data EEPROM modules, refer to the respective peripheral section.

12.9.1 RA2/INT INTERRUPT

External interrupt on RA2/INT pin is edge-triggered; either rising if the INTEDG bit of the OPTION register is set, or falling if the INTEDG bit is clear. When a valid edge appears on the RA2/INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The RA2/INT interrupt can wake-up the processor from Sleep if the INTE bit was set prior to going into Sleep. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up (0004h). See **Section 12.12 "Power-Down Mode (Sleep)"** for details on Sleep and Figure 12-10 for timing of wake-up from Sleep through RA2/INT interrupt.

Note:	The CMCON0 (19h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

14.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C18 and MPLAB C30 C Compilers
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PICSTART® Plus Development Programmer
  - MPLAB PM3 Device Programmer
  - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (assembly or C)
  - Mixed assembly and C
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

15.2 DC Characteristics: PIC12F635/PIC16F636-I (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Sym	Device Characteristics	Min	Typ†	Max	Units	Conditions	
							VDD	Note
D010	IDD	**Supply Current(1,2)**	—	11	16	µA	2.0	FOSC = 32.768 kHz LP Oscillator mode
			—	18	28	µA	3.0	
			—	35	54	µA	5.0	
D011			—	140	240	µA	2.0	FOSC = 1 MHz XT Oscillator mode
			—	220	380	µA	3.0	
			—	380	550	µA	5.0	
D012			—	260	360	µA	2.0	FOSC = 4 MHz XT Oscillator mode
			—	420	650	µA	3.0	
			—	0.8	1.1	mA	5.0	
D013			—	130	220	µA	2.0	FOSC = 1 MHz EC Oscillator mode
			—	215	360	µA	3.0	
			—	360	520	µA	5.0	
D014			—	220	340	µA	2.0	FOSC = 4 MHz EC Oscillator mode
			—	375	550	µA	3.0	
			—	0.65	1.0	mA	5.0	
D015			—	8	20	µA	2.0	FOSC = 31 kHz LFINTOSC mode
			—	16	40	µA	3.0	
			—	31	65	µA	5.0	
D016			—	340	450	µA	2.0	FOSC = 4 MHz HFINTOSC mode
			—	500	700	µA	3.0	
			—	0.8	1.2	mA	5.0	
D017			—	410	650	µA	2.0	FOSC = 8 MHz HFINTOSC mode
			—	700	950	µA	3.0	
			—	1.30	1.65	mA	5.0	
D018			—	230	400	µA	2.0	FOSC = 4 MHz EXTRC mode
			—	400	680	µA	3.0	
			—	0.63	1.1	mA	5.0	
D019			—	2.6	3.25	mA	4.5	FOSC = 20 MHz HS Oscillator mode
			—	2.6	3.25	mA	5.0	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled. MCU only, Analog Front-End not included.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. MCU only, Analog Front-End not included.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral ∆ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

15.2 DC Characteristics: PIC12F635/PIC16F636-I (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Sym	Device Characteristics	Min	Typ†	Max	Units	Conditions	
							VDD	Note
D020	IPD	**Power-down Base Current(4)**	—	0.15	1.2	µA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
			—	0.20	1.5	µA	3.0	
			—	0.35	1.8	µA	5.0	
D021			—	1.0	2.2	µA	2.0	WDT Current(1)
			—	2.0	4.0	µA	3.0	
			—	3.0	7.0	µA	5.0	
D022A			—	58	60	µA	3.0	BOR Current(1)
			—	109	122	µA	5.0	
D022B			—	22	28	µA	2.0	PLVD Current
			—	25	35	µA	3.0	
			—	33	45	µA	5.0	
D023			—	32	45	µA	2.0	Comparator Current(3)
			—	60	78	µA	3.0	
			—	120	160	µA	5.0	
D024A			—	30	36	µA	2.0	CVREF Current(1) (high-range)
			—	45	55	µA	3.0	
			—	75	95	µA	5.0	
D024B			—	39	47	µA	2.0	CVREF Current(1) (low-range)
			—	59	72	µA	3.0	
			—	98	124	µA	5.0	
D025			—	4.5	7.0	µA	2.0	T1OSC Current(3)
			—	5.0	8.0	µA	3.0	
			—	6.0	12	µA	5.0	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled. MCU only, Analog Front-End not included.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. MCU only, Analog Front-End not included.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral ∆ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

TABLE 15-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym**	**Characteristic**	**Freq Tolerance**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
OS06	TWARM	Internal Oscillator Switch when running(3)	—	—	—	2	TOSC	Slowest clock
OS07	TSC	Fail-Safe Sample Clock Period(1)	—	—	21	—	ms	LFINTOSC/64
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(2)	±1%	7.92	8.0	8.08	MHz	VDD = 3.5V, 25°C
			±2%	7.84	8.0	8.16	MHz	2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C
			±5%	7.60	8.0	8.40	MHz	2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.)
OS09*	LFOSC	Internal Uncalibrated LFINTOSC Frequency	—	15	31	45	kHz	
OS10*	TIOSCST	HFINTOSC Oscillator Wake-up from Sleep Start-up Time	—	5.5	12	24	µs	VDD = 2.0V, -40°C to +85°C
			—	3.5	7	14	µs	VDD = 3.0V, -40°C to +85°C
			—	3	6	11	µs	VDD = 5.0V, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

3: By design.

FIGURE 16-2: MAXIMUM IDD vs. FOSC OVER VDD (EC MODE)

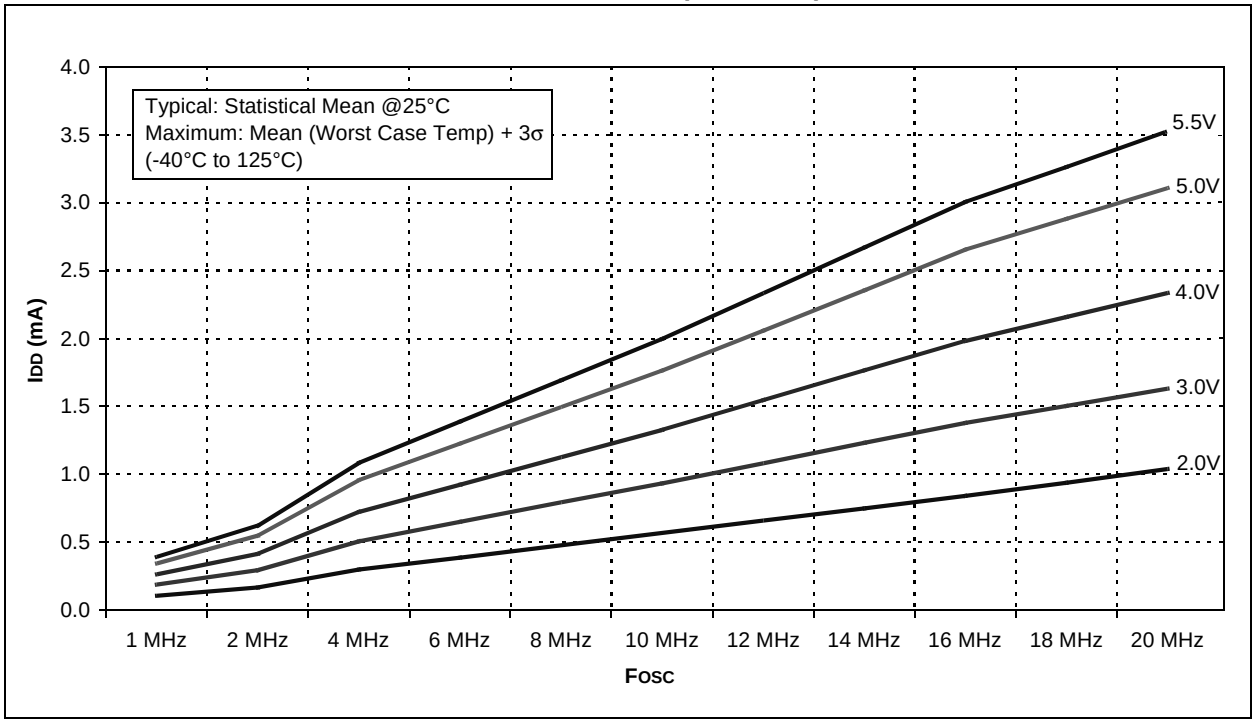
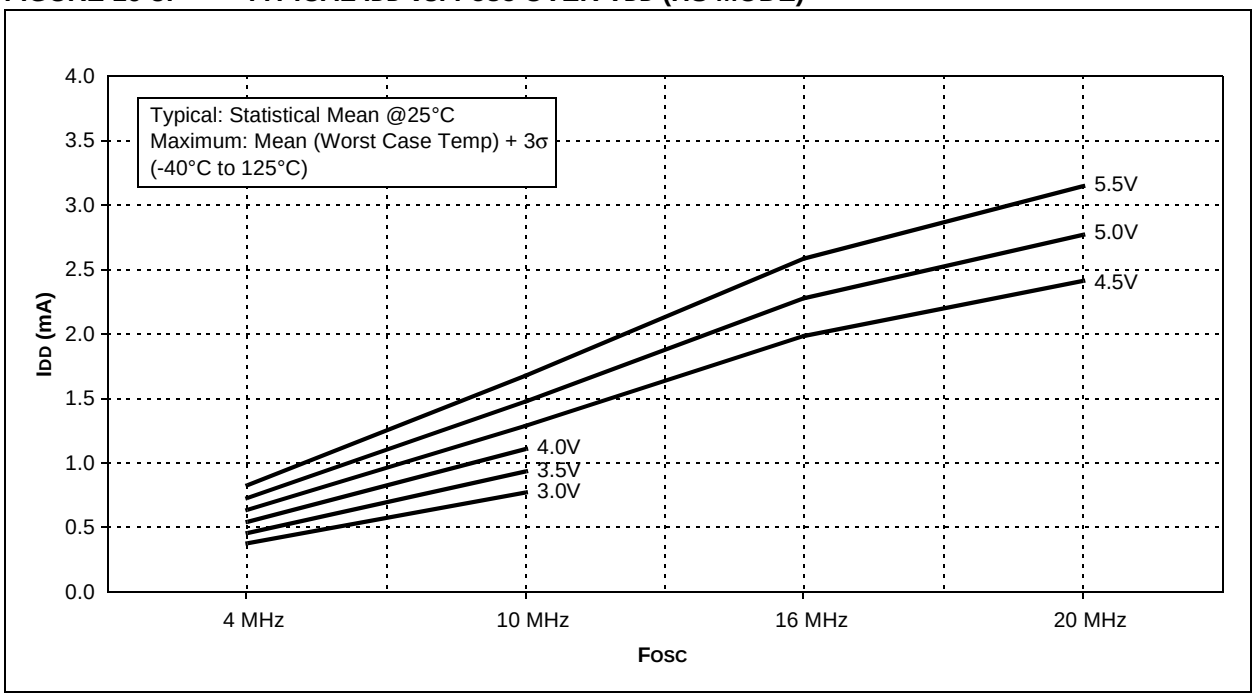


FIGURE 16-3: TYPICAL IDD vs. FOSC OVER VDD (HS MODE)

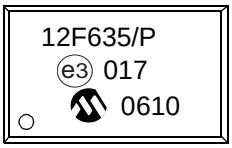


17.0 PACKAGING INFORMATION

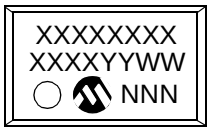
17.1 Package Marking Information

8-Lead PDIP

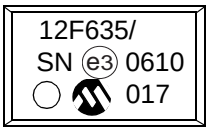
Example



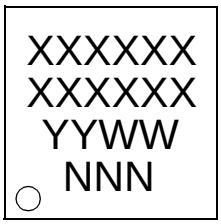
8-Lead SOIC



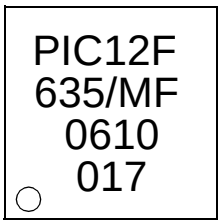
Example



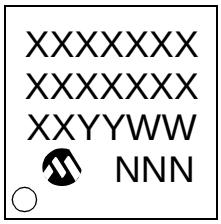
8-Lead DFN (4x4x0.9 mm)



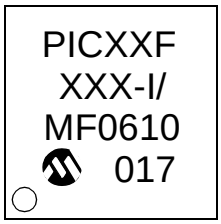
Example



8-Lead DFN-S (6x5 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard PIC device marking consists of Microchip part number, year code, week code and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.