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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f639t-i-ss

PIC12F635/PIC16F636/639

TABLE 2-2: PIC12F635 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR/WUR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32,137
81h	OPTION_REG	RAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	63,137
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	32,137
83h	STATUS	IRP	RP1	RP0	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	26,137
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	32,137
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter				---	0 0000	32,137
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF ⁽³⁾	0000 000x	28,137
8Ch	PIE1	EEIE	LVDIE	CRIE	—	C1IE	OSFIE	—	TMR1IE	000- 00-0	29,137
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	ULPWUE	SBOREN	\overline{WUR}	—	\overline{POR}	\overline{BOR}	--01 q-qq	31,137
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	~110 q000	36,137
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	40,137
91h	—	Unimplemented								—	—
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -000	--00 -000
95h	WPUDA ⁽²⁾	—	—	WPUDA5	WPUDA4	—	WPUDA2	WPUDA1	WPUDA0	--11 -111	--11 -111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
97h	WDA ⁽²⁾	—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0	--11 -111	--11 -111
9Bh	—	Unimplemented								—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
9Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----
9Eh	—	Unimplemented								—	—
9Fh	—	Unimplemented								—	—

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

- Note** 1: Other (non Power-up) Resets include \overline{MCLR} Reset and Watchdog Timer Reset during normal operation.
2: GP3 pull-up is enabled when pin is configured as \overline{MCLR} in the Configuration Word register.
3: \overline{MCLR} and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset, but will set again if the mismatch exists.

3.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

3.1 Overview

The Oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 3-1 illustrates a block diagram of the Oscillator module.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured from one of two internal oscillators, with a choice of speeds selectable via software. Additional clock features include:

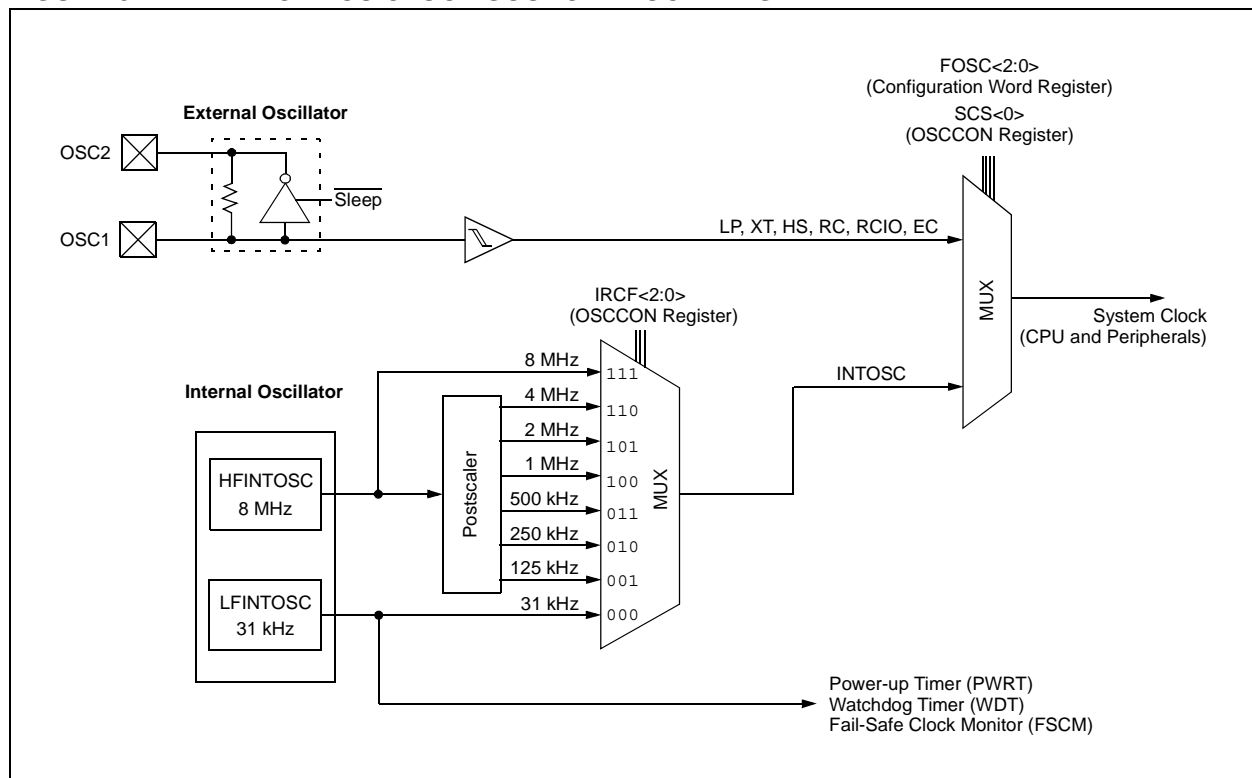
- Selectable system clock source between external or internal via software.
- Two-Speed Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch automatically to the internal oscillator.

The Oscillator module can be configured in one of eight clock modes.

1. EC – External clock with I/O on OSC2/CLKOUT.
2. LP – 32 kHz Low-Power Crystal mode.
3. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
4. HS – High Gain Crystal or Ceramic Resonator mode.
5. RC – External Resistor-Capacitor (RC) with Fosc/4 output on OSC2/CLKOUT.
6. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
7. INTOSC – Internal oscillator with Fosc/4 output on OSC2 and I/O on OSC1/CLKIN.
8. INTOSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.

Clock Source modes are configured by the FOSC<2:0> bits in the Configuration Word register (CONFIG). The internal clock can be generated from two internal oscillators. The HFINTOSC is a calibrated high-frequency oscillator. The LFINTOSC is an uncalibrated low-frequency oscillator.

FIGURE 3-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



PIC12F635/PIC16F636/639

3.2 Oscillator Control

The Oscillator Control (OSCCON) register (Figure 3-1) controls the system clock and frequency selection options. The OSCCON register contains the following bits:

- Frequency selection bits (IRCF)
- Frequency Status bits (HTS, LTS)
- System clock control bits (OSTS, SCS)

REGISTER 3-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R/W-1	R/W-1	R/W-0	R-1	R-0	R-0	R/W-0
—	IRCF2	IRCF1	IRCF0	OSTS ⁽¹⁾	HTS	LTS	SCS
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IRCF<2:0>:** Internal Oscillator Frequency Select bits

111 = 8 MHz

110 = 4 MHz (default)

101 = 2 MHz

100 = 1 MHz

011 = 500 kHz

010 = 250 kHz

001 = 125 kHz

000 = 31 kHz (LFINTOSC)

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit⁽¹⁾

1 = Device is running from the external clock defined by FOSC<2:0> of the Configuration Word

0 = Device is running from the internal oscillator (HFINTOSC or LFINTOSC)

bit 2 **HTS:** HFINTOSC Status bit (High Frequency – 8 MHz to 125 kHz)

1 = HFINTOSC is stable

0 = HFINTOSC is not stable

bit 1 **LTS:** LFINTOSC Stable bit (Low Frequency – 31 kHz)

1 = LFINTOSC is stable

0 = LFINTOSC is not stable

bit 0 **SCS:** System Clock Select bit

1 = Internal oscillator is used for system clock

0 = Clock source defined by FOSC<2:0> of the Configuration Word

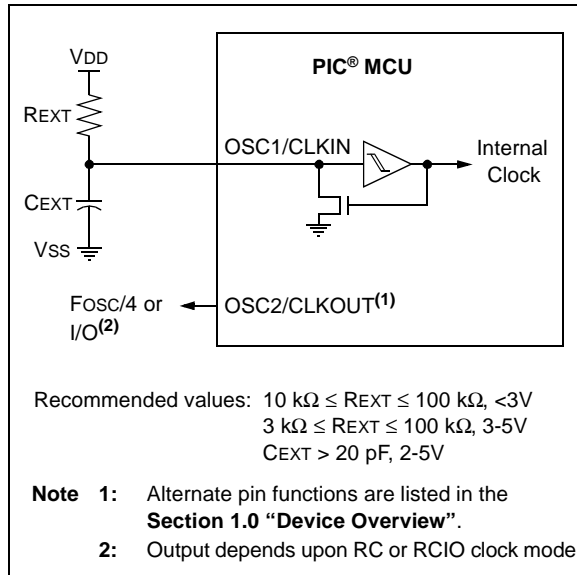
Note 1: Bit resets to '0' with Two-Speed Start-up and LP, XT or HS selected as the Oscillator mode or Fail-Safe mode is enabled.

3.4.4 EXTERNAL RC MODES

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes: RC and RCIO.

In RC mode, the RC circuit connects to OSC1. OSC2/CLKOUT outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 3-5 shows the external RC mode connections.

FIGURE 3-5: EXTERNAL RC MODES



In RCIO mode, the RC circuit is connected to OSC1. OSC2 becomes an additional general purpose I/O pin. The RC oscillator frequency is a function of the supply voltage, the resistor (R_{EXT}) and capacitor (C_{EXT}) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

3.5 Internal Clock Modes

The Oscillator module has two independent, internal oscillators that can be configured or selected as the system clock source.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 8 MHz. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 3-2).
2. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits $IRCF<2:0>$ of the OSCCON register.

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit of the OSCCON register. See **Section 3.6 “Clock Switching”** for more information.

3.5.1 INTOSC AND INTOSCIO MODES

The INTOSC and INTOSCIO modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the $FOSC<2:0>$ bits in the Configuration Word register (CONFIG). See **Section 12.0 “Special Features of the CPU”** for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTOSCIO** mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.

3.5.2 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 8 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 3-2).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). One of seven frequencies can be selected via software using the $IRCF<2:0>$ bits of the OSCCON register. See **Section 3.5.4 “Frequency Select Bits (IRCF)”** for more information.

The HFINTOSC is enabled by selecting any frequency between 8 MHz and 125 kHz by setting the $IRCF<2:0>$ bits of the OSCCON register $\neq 000$. Then, set the System Clock Source (SCS) bit of the OSCCON register to ‘1’ or enable Two-Speed Start-up by setting the IESO bit in the Configuration Word register (CONFIG) to ‘1’.

The HF Internal Oscillator (HTS) bit of the OSCCON register indicates whether the HFINTOSC is stable or not.

3.6 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bit of the OSCCON register.

3.6.1 SYSTEM CLOCK SELECT (SCS) BIT

The System Clock Select (SCS) bit of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bit of the OSCCON register = 0, the system clock source is determined by configuration of the FOSC<2:0> bits in the Configuration Word register (CONFIG).
- When the SCS bit of the OSCCON register = 1, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<2:0> bits of the OSCCON register. After a Reset, the SCS bit of the OSCCON register is always cleared.

Note: Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bit of the OSCCON register. The user can monitor the OSTS bit of the OSCCON register to determine the current system clock source.

3.6.2 OSCILLATOR START-UP TIME-OUT STATUS (OSTS) BIT

The Oscillator Start-up Time-out Status (OSTS) bit of the OSCCON register indicates whether the system clock is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes.

3.7 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.

This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

Note: Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCCON register to remain clear.

When the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) is enabled (see **Section 3.4.1 “Oscillator Start-up Timer (OST)”**). The OST will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as the OST is counting. When the OST count reaches 1024 and the OSTS bit of the OSCCON register is set, program execution switches to the external oscillator.

3.7.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Word register) = 1; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS (of the OSCCON register) = 0.
- FOSC<2:0> bits in the Configuration Word register (CONFIG) configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured to be anything other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

3.7.2 TWO-SPEED START-UP SEQUENCE

1. Wake-up from Power-on Reset or Sleep.
2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF<2:0> bits of the OSCCON register.
3. OST enabled to count 1024 clock cycles.
4. OST timed out, wait for falling edge of the internal oscillator.
5. OSTS is set.
6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
7. System clock is switched to external clock source.

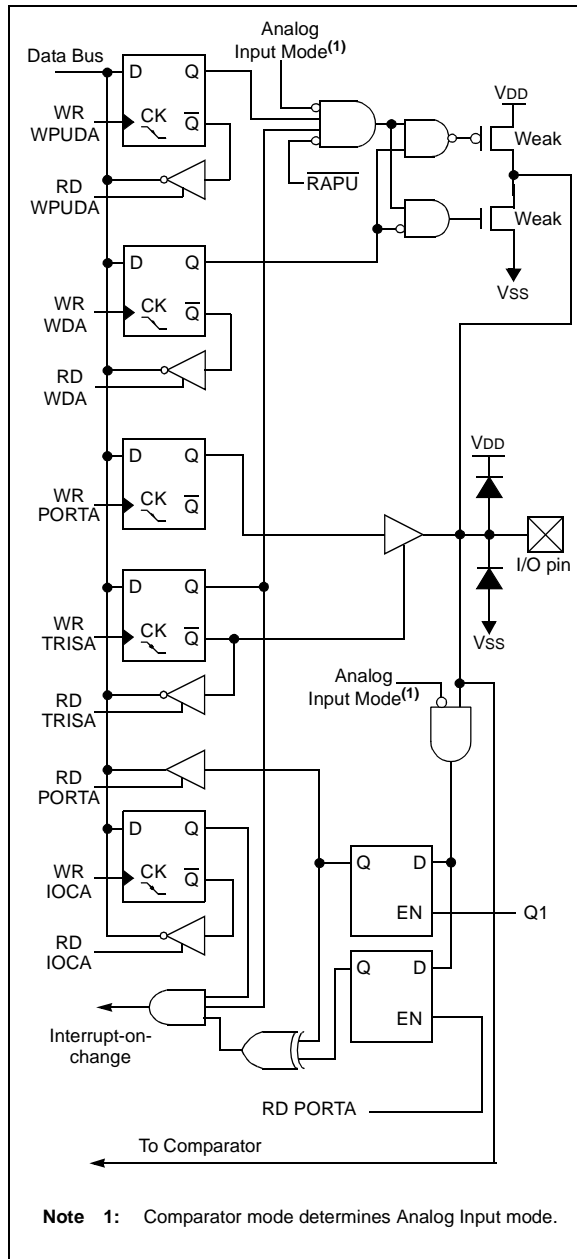
PIC12F635/PIC16F636/639

4.2.4.2 RA1/C1IN-/V_{REF}/ICSPCLK

Figure 4-2 shows the diagram for this pin. The RA1 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input to the comparator
- In-Circuit Serial Programming™ clock

FIGURE 4-2: BLOCK DIAGRAM OF RA1

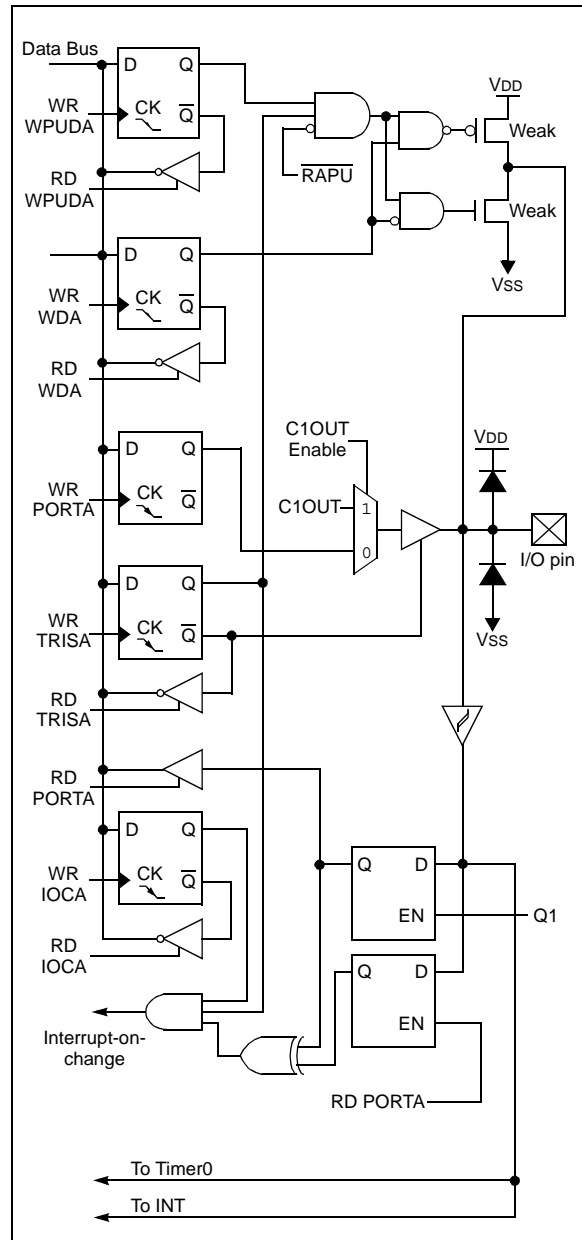


4.2.4.3 RA2/T0CKI/INT/C1OUT

Figure 4-3 shows the diagram for this pin. The RA2 pin is configurable to function as one of the following:

- a general purpose I/O
- the clock input for Timer0
- an external edge-triggered interrupt
- a digital output from the comparator

FIGURE 4-3: BLOCK DIAGRAM OF RA2



6.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 interrupt enable bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note: The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

6.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set

The device will wake-up on an overflow and execute the next instruction. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

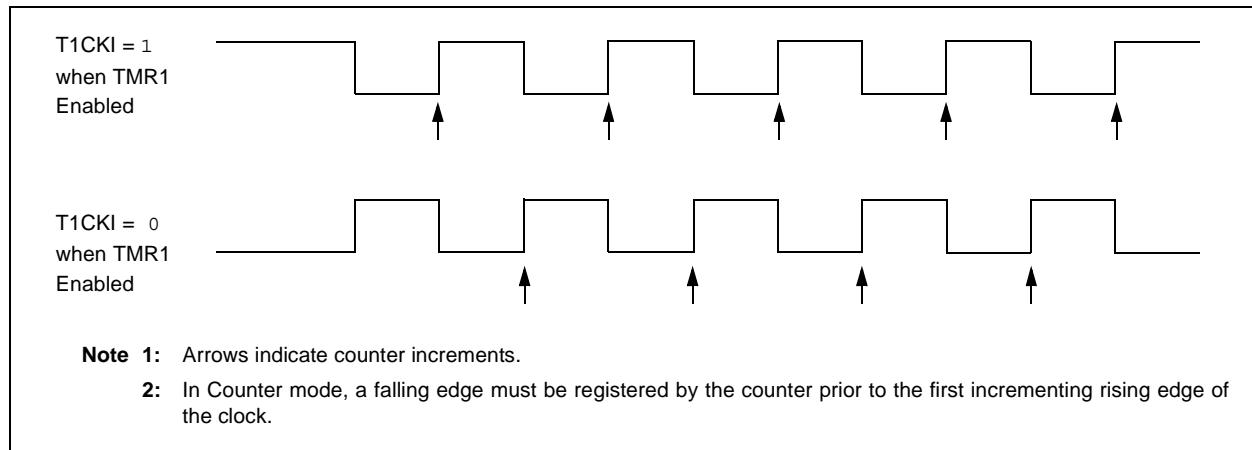
6.9 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see **Section 7.0 “Comparator Module”**.

FIGURE 6-2: TIMER1 INCREMENTING EDGE



8.0 PROGRAMMABLE LOW-VOLTAGE DETECT (PLVD) MODULE

The Programmable Low-Voltage Detect (PLVD) module is a power supply detector which monitors the internal power supply. This module is typically used in key fobs and other devices, where certain actions need to be taken as a result of a falling battery voltage.

The PLVD module includes the following capabilities:

- Eight programmable trip points
- Interrupt on falling V_{DD}
- Stable reference indication
- Operation during Sleep

A Block diagram of the PLVD module is shown in Figure 8-1.

FIGURE 8-1: PLVD BLOCK DIAGRAM

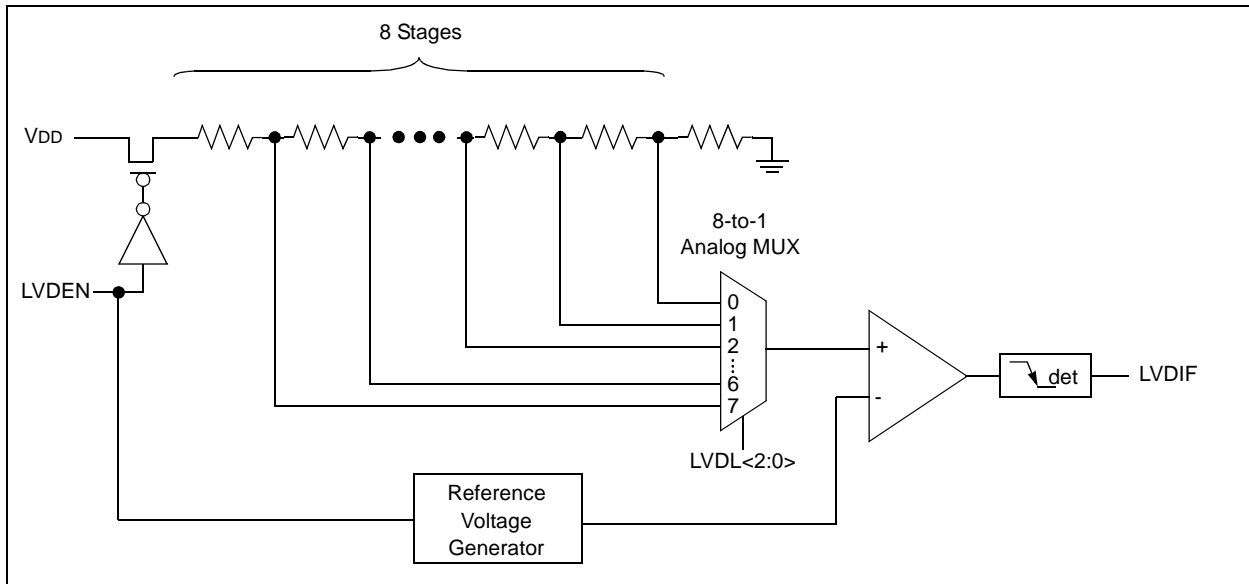
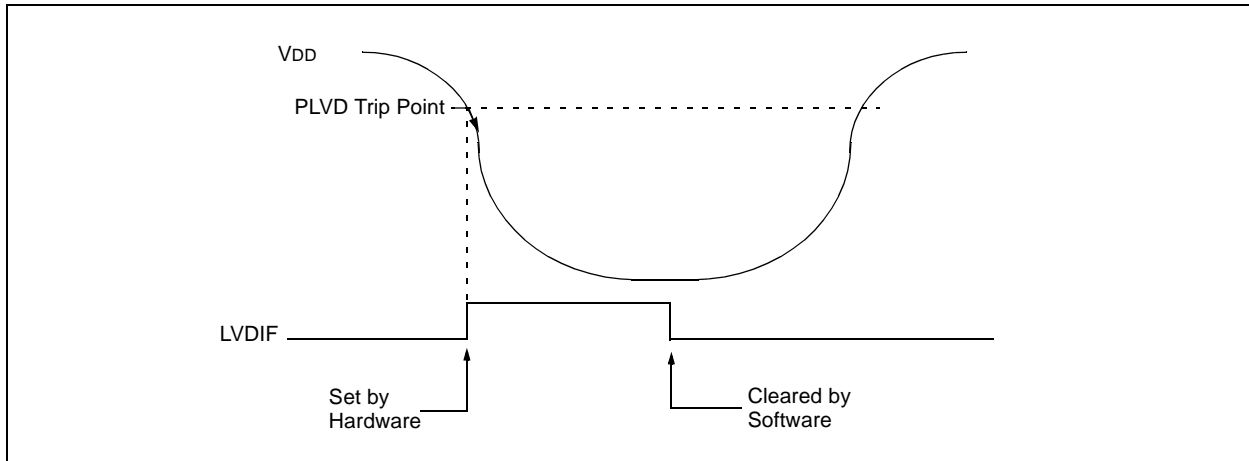


FIGURE 8-2: PLVD OPERATION



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REGISTER 11-8: AFE STATUS REGISTER 7

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CHZACT	CHYACT	CHXACT	AGCACT	WAKEZ	WAKEY	WAKEX	ALARM	PEI
bit 8								bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 8	CHZACT: Channel Z Active ⁽¹⁾ bit (cleared via Soft Reset) 1 = Channel Z is passing data after TAGC 0 = Channel Z is not passing data after TAGC
bit 7	CHYACT: Channel Y Active ⁽¹⁾ bit (cleared via Soft Reset) 1 = Channel Y is passing data after TAGC 0 = Channel Y is not passing data after TAGC
bit 6	CHXACT: Channel X Active ⁽¹⁾ bit (cleared via Soft Reset) 1 = Channel X is passing data after TAGC 0 = Channel X is not passing data after TAGC
bit 5	AGCACT: AGC Active Status bit (real time, cleared via Soft Reset) 1 = AGC is active (Input signal is strong). AGC is active when input signal level is approximately > 20 mVPP range. 0 = AGC is inactive (Input signal is weak)
bit 4	WAKEZ: Wake-up Channel Z Indicator Status bit (cleared via Soft Reset) 1 = Channel Z caused a AFE wake-up (passed +64 clock counter) 0 = Channel Z did not cause a AFE wake-up
bit 3	WAKEY: Wake-up Channel Y Indicator Status bit (cleared via Soft Reset) 1 = Channel Y caused a AFE wake-up (passed +64 clock counter) 0 = Channel Y did not cause a AFE wake-up
bit 2	WAKEX: Wake-up Channel X Indicator Status bit (cleared via Soft Reset) 1 = Channel X caused a AFE wake-up (passed +64 clock counter) 0 = Channel X did not cause a AFE wake-up
bit 1	ALARM: Indicates whether an Alarm timer time-out has occurred (cleared via read "Status Register command") 1 = The Alarm timer time-out has occurred. It may cause the ALERT output to go low depending on the state of bit 4 of the Configuration register 0 0 = The Alarm timer is not timed out
bit 0	PEI: Parity Error Indicator bit – indicates whether a Configuration register parity error has occurred (real time) 1 = A parity error has occurred and caused the ALERT output to go low 0 = A parity error has not occurred

Note 1: Bit is high whenever channel is passing data. Bit is low in Standby mode.

See Table 11-7 for the bit conditions of the AFE Status Register after various SPI commands and the AFE Power-on Reset.

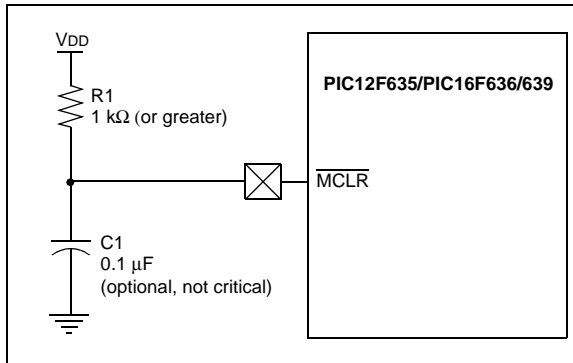
TABLE 11-7: AFE STATUS REGISTER BIT CONDITION (AFTER POWER-ON RESET AND VARIOUS SPI COMMANDS)

Condition	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CHZACT	CHYACT	CHXACT	AGCACT	WAKEZ	WAKEY	WAKEX	ALARM	PEI
POR	0	0	0	0	0	0	0	0	1
Read Command (STATUS Register only)	u	u	u	u	u	u	u	0	u
Sleep Command	u	u	u	u	u	u	u	u	u
Soft Reset Executed ⁽¹⁾	0	0	0	0	0	0	0	u	u

Legend: u = unchanged

Note 1: See Section 11.20 "Soft Reset" and Section 11.32.2.4 "Soft Reset Command" for the condition of Soft Reset execution.

FIGURE 12-2: RECOMMENDED $\overline{\text{MCLR}}$ CIRCUIT



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12.7 Time-out Sequence

On power-up, the time-out sequence is as follows: first, PWRT time-out is invoked after POR has expired, then OST is activated after the PWRT time-out has expired. The total time-out will vary based on oscillator Configuration and PWRTE bit status. For example, in EC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 12-4, Figure 12-5 and Figure 12-6 depict time-out sequences. The device can execute code from the INTOSC, while OST is active, by enabling Two-Speed Start-up or Fail-Safe Clock Monitor (See **Section 3.7.2 “Two-Speed Start-up Sequence”** and **Section 3.8 “Fail-Safe Clock Monitor”**).

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then bringing MCLR high will begin execution immediately (see Figure 12-5). This is useful for testing purposes or to synchronize more than one PIC12F635/PIC16F636/639 device operating in parallel.

Table 12-5 shows the Reset conditions for some special registers, while Table 12-4 shows the Reset conditions for all the registers.

12.8 Power Control (PCON) Register

The Power Control register, PCON (address 8Eh), has two Status bits to indicate what type of Reset that last occurred.

Bit 0 is $\overline{\text{BOR}}$ (Brown-out). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}} = 0$, indicating that a Brown-out has occurred. The $\overline{\text{BOR}}$ Status bit is a “don’t care” and is not necessarily predictable if the brown-out circuit is disabled ($\text{BOREN}<1:0> = 00$ in the Configuration Word register).

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset). It is a ‘0’ on Power-on Reset and unaffected otherwise. The user must write a ‘1’ to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{\text{POR}}$ is ‘0’, it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see **Section 4.2.3 “Ultra Low-Power Wake-up”** and **Section 12.6 “Brown-out Reset (BOR)”**.

TABLE 12-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	
XT, HS, LP	TPWRT + 1024 • TOSC	1024 • TOSC	TPWRT + 1024 • TOSC	1024 • TOSC	1024 • TOSC
RC, EC, INTOSC	TPWRT	—	TPWRT	—	—

TABLE 12-2: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT RESET

Name	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets ⁽¹⁾
CONFIG ⁽²⁾	BOREN1	BOREN0	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—
PCON			—	—	ULPWUE	SBOREN	$\overline{\text{WUR}}$	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	--01 --qq	--0u ---uu
STATUS			IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, — = unimplemented bit, reads as ‘0’, q = value depends on condition. Shaded cells are not used by BOR.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

Note 2: See Configuration Word register (Register 12-1) for operation of all register bits.

TABLE 12-3: PCON BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{WUR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Condition
0	x	x	1	1	Power-on Reset
u	0	u	1	1	Brown-out Reset
u	u	u	0	u	WDT Reset
u	u	u	0	0	WDT Wake-up
u	u	u	u	u	MCLR Reset during normal operation
u	u	u	1	0	MCLR Reset during Sleep
u	u	0	1	0	Wake-up Reset during Sleep
u	0	u	1	1	Brown-out Reset during Sleep

Legend: u = unchanged, x = unknown

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12.9.2 TIMER INTERRUPT

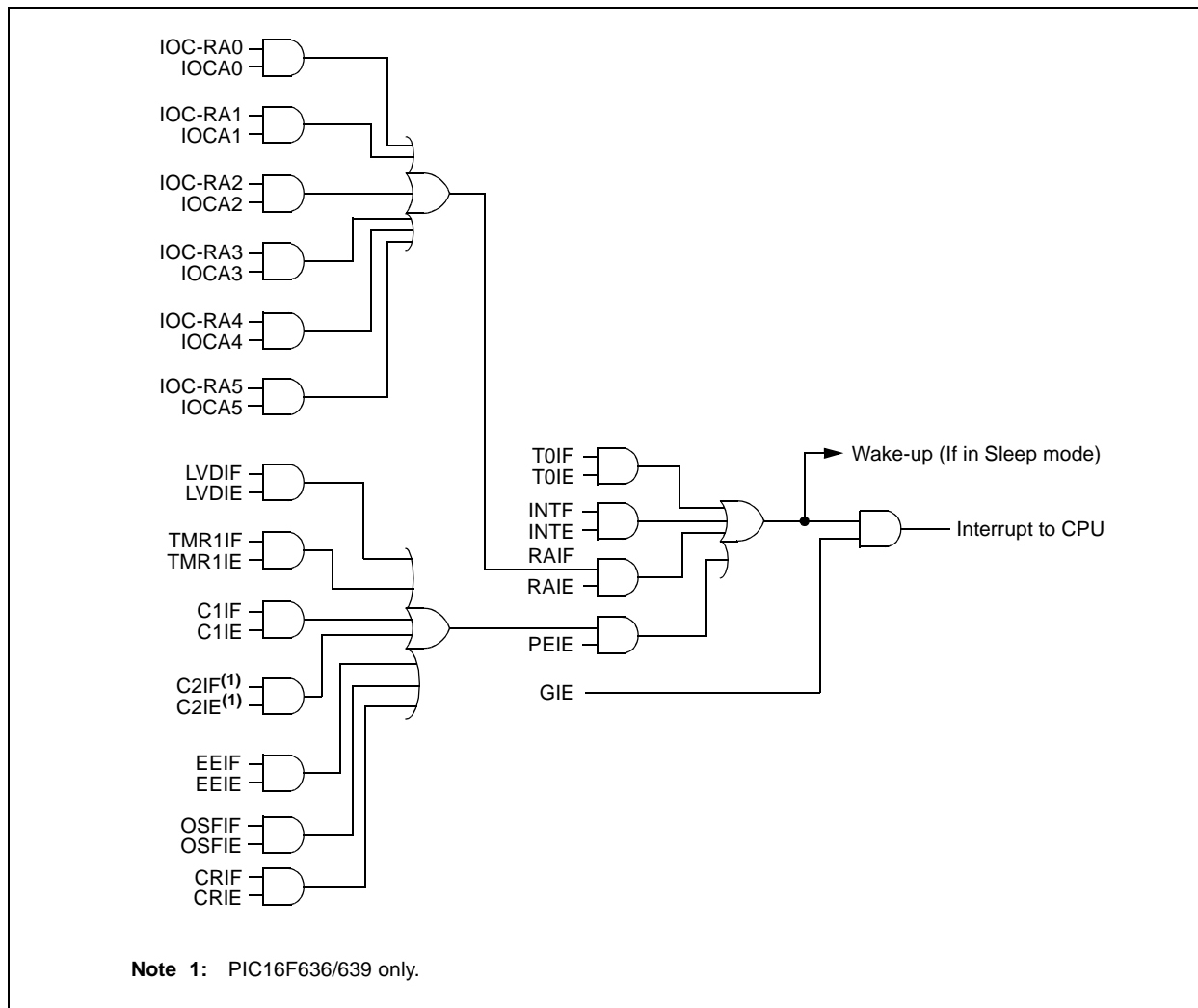
An overflow (FFh → 00h) in the TMR0 register will set the T0IF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing T0IE bit of the INTCON register. See **Section 5.0 “Timer0 Module”** for operation of the Timer0 module.

12.9.3 PORTA INTERRUPT

An input change on PORTA change sets the RAIF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing the RAIE bit of the INTCON register. Plus, individual pins can be configured through the IOCA register.

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RAIF interrupt flag may not get set.

FIGURE 12-7: INTERRUPT LOGIC



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FIGURE 12-8: INT PIN INTERRUPT TIMING

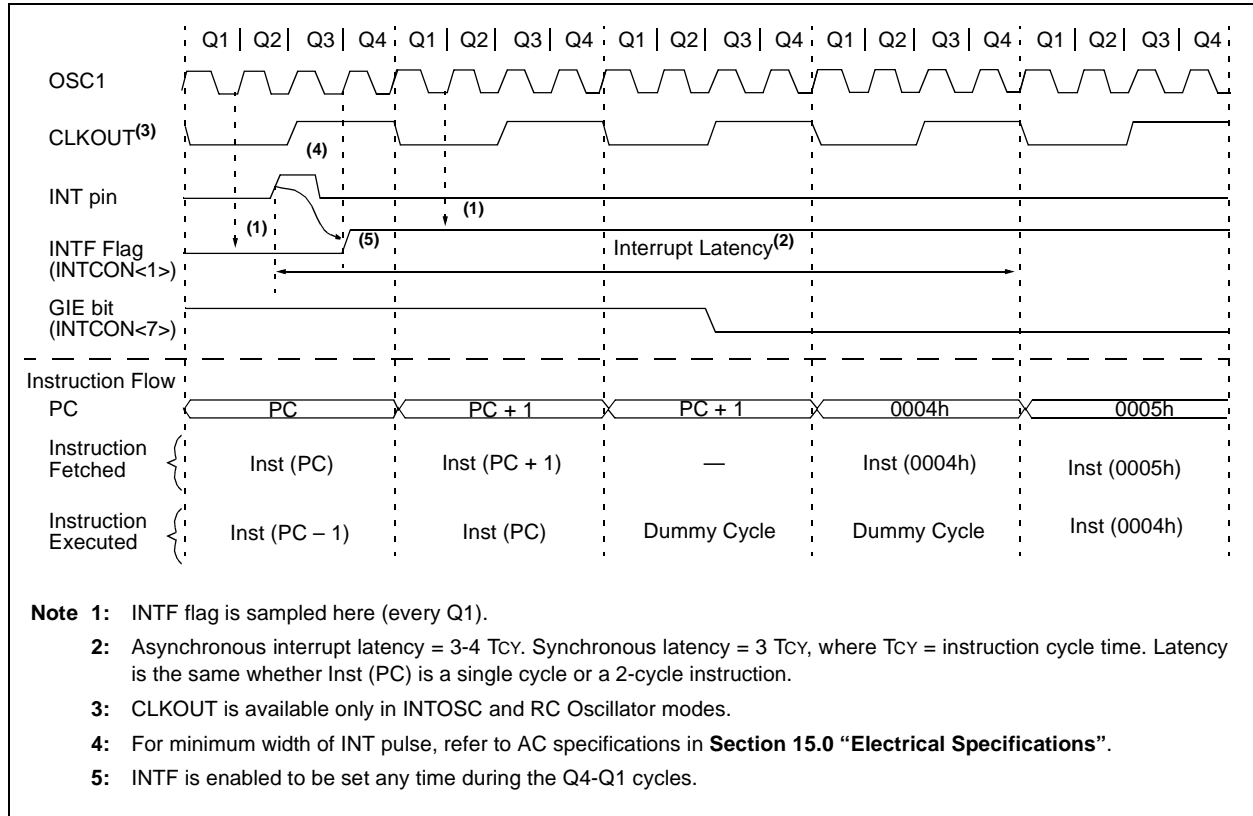


TABLE 12-6: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
PIR1	EEIF	LVDIF	CRIF	C2IF ⁽¹⁾	C1IF	OSFIF	—	TMR1IF	0000 00-0	0000 00-0
PIE1	EEIE	LVDIE	CRIE	C2IE ⁽¹⁾	C1IE	OSFIE	—	TMR1IE	0000 00-0	0000 00-0

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0', q = value depends upon condition.
Shaded cells are not used by the Interrupt module.

Note 1: PIC16F636/639 only.

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MOVF	Move f
Syntax:	[<i>label</i>] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) \rightarrow (\text{dest})$
Status Affected:	Z
Description:	The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
Example:	<pre>MOVF FSR, 0</pre> <p>After Instruction</p> <p>W = value in FSR register Z = 1</p>

MOVLW	Move literal to W
Syntax:	[<i>label</i>] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k \rightarrow (W)$
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.
Words:	1
Cycles:	1
Example:	<pre>MOVLW 0x5A</pre> <p>After Instruction</p> <p>W = 0x5A</p>

MOVWF	Move W to f
Syntax:	[<i>label</i>] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
Example:	<pre>MOVWF OPTION F</pre> <p>Before Instruction</p> <p>OPTION = 0xFF W = 0x4F</p> <p>After Instruction</p> <p>OPTION = 0x4F W = 0x4F</p>

NOP	No Operation
Syntax:	[<i>label</i>] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Words:	1
Cycles:	1
Example:	<pre>NOP</pre>

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RLF Rotate Left f through Carry

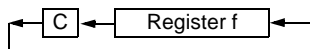
Syntax: [*label*] RLF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example: RLF REG1,0

Before Instruction

REG1 = 1110 0110
C = 0

After Instruction

REG1 = 1110 0110
W = 1100 1100
C = 1

SLEEP Enter Sleep mode

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → \overline{TO} ,
0 → \overline{PD}

Status Affected: \overline{TO} , \overline{PD}

Description: The power-down Status bit, \overline{PD} is cleared. Time-out Status bit, \overline{TO} is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

RRF Rotate Right f through Carry

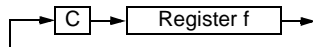
Syntax: [*label*] RRF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SUBLW Subtract W from literal

Syntax: [*label*] SUBLW k

Operands: $0 \leq k \leq 255$

Operation: $k - (W) \rightarrow (W)$

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

C = 0	$W > k$
C = 1	$W \leq k$
DC = 0	$W<3:0> > k<3:0>$
DC = 1	$W<3:0> \leq k<3:0>$

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15.4 DC Characteristics: PIC12F635/PIC16F636-I (Industrial) PIC12F635/PIC16F636-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D090	VOH	Output High Voltage I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V (Ind.)
D092		OSC2/CLKOUT (RC mode)	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V (Ind.) IOH = -1.0 mA, VDD = 4.5V (Ext.)
D100	IULP	Ultra Low-power Wake-up Current	—	200	—	nA	
D101	COSC2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A	CIO	All I/O pins	—	—	50*	pF	
D120	ED	Data EEPROM Memory Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C +85°C ≤ TA ≤ +125°C Using EECON1 to read/write VMIN = Minimum operating voltage
D120A	ED	Byte Endurance	10K	100K	—	E/W	
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	
D122	TDEW	Erase/Write cycle time	—	5	6	ms	Provided no other specifications are violated
D123	TRETD	Characteristic Retention	40	—	—	Year	
D124	TREF	Number of Total Erase/Write Cycles before Refresh ⁽⁴⁾	1M	10M	—	E/W	
D130	EP	Program Flash Memory Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C +85°C ≤ TA ≤ +125°C VMIN = Minimum operating voltage
D130A	ED	Cell Endurance	1K	10K	—	E/W	
D131	VPR	VDD for Read	VMIN	—	5.5	V	
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.
- 2:** Negative current is defined as current sourced by the pin.
- 3:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 4:** See **Section 9.4.1 "Using the Data EEPROM"** for additional information.

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15.7 DC Characteristics: PIC16F639-I (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature		-40°C ≤ TA ≤ +85°C for industrial		
			Supply Voltage		2.0V ≤ VDD ≤ 3.6V		
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D090	VOH	Output High Voltage					
		I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 3.6V (Ind.)
D092		OSC2/CLKOUT (RC mode)	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 3.6V (Ind.) IOH = -1.0 mA, VDD = 3.6V (Ext.)
D093		Digital Output High Voltage LFDATA/SDIO for Analog Front-End (AFE)	VDD – 0.5	—	—	V	Analog Front-End (AFE) section IOH = -400 μA, VDD = 2.0V
D100	COSC2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	—	50*	pF	
D102	IULP	Ultra Low-power Wake-up Current	—	200	—	nA	
D120	ED	Data EEPROM Memory Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	5	6	ms	Provided no other specifications are violated
D123	TRETD	Characteristic Retention	40	—	—	Year	
D124	TREF	Number of Total Erase/Write Cycles before Refresh ⁽¹⁾	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
D130	EP	Program Flash Memory Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	Provided no other specifications are violated
D134	TRETD	Characteristic Retention	40	—	—	Year	

* These parameters are characterized but not tested.

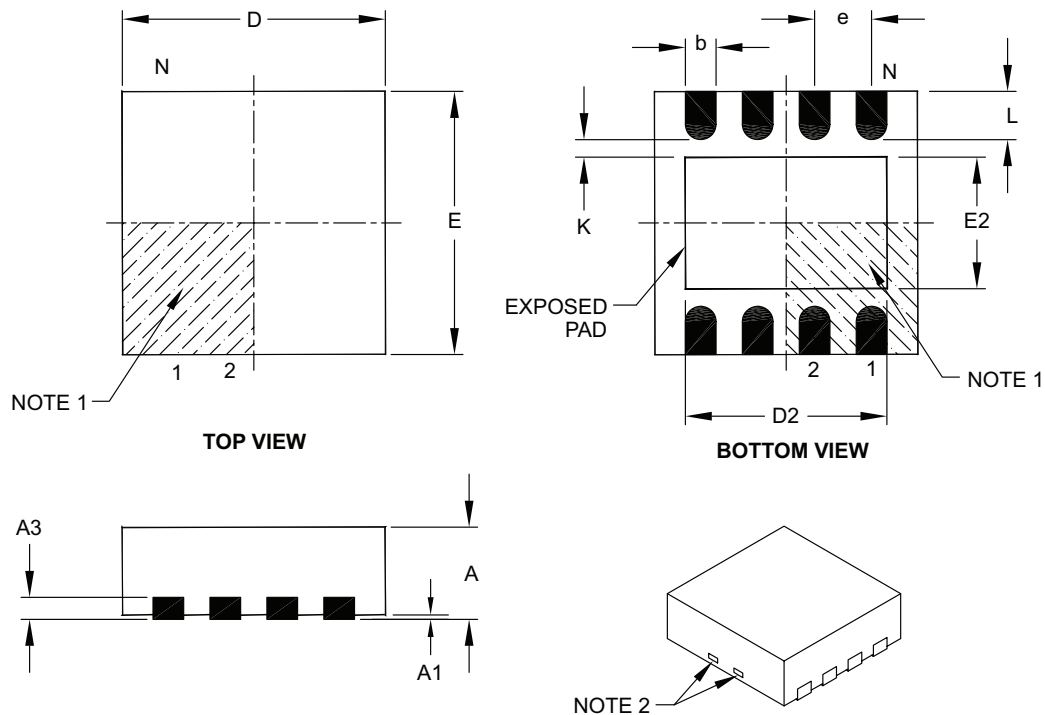
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note** 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.
- 2: Negative current is defined as current sourced by the pin.
- 3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 4: See **Section 9.4.1 "Using the Data EEPROM"** for additional information

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8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.80 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	4.00 BSC		
Exposed Pad Width	E2	0.00	2.20	2.80
Overall Width	E	4.00 BSC		
Exposed Pad Length	D2	0.00	3.00	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.55	0.65
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131C

PIC12F635/PIC16F636/639

NOTES: