Infineon Technologies - XE169FH200F100LABFXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	1.6MB (1.6M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	112K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 30x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-176-12
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe169fh200f100labfxuma1

XE169xH Data Sheet
Revision History: V1.3 2011-07

Previous Versions:
V1.2, 2010-09
V1.1, 2010-02 Preliminary

Page	Subjects (major changes since last revision)
10	Clarified available Flash and SRAM memory allocation.
82	USIC “QSPI” protocol shortcut removed due to ambiguity (interpreted as Queued SPI or Quad SPI).
110	Relaxed the conditions for short-term deviation of internal clock source frequency Δf_{INT}.
110	Added startup time from power-on t_{SPO}
113	Removed the 128MHz conditions for N_{WSFLE}
120	Added the minimum PLL free running frequency. Reduced the min/max bandwidth.
145	Thermal resistance values updated.

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Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
14	P8.1	O0 / I	St/B	**Bit 1 of Port 8, General Purpose Input/Output**
	CCU60_CC61	O1	St/B	**CCU60 Channel 1 Output**
	CC1_CC1	O2	St/B	**CC1 Channel 1 Output**
	U4C1_MCLKOUT	O3	St/B	**USIC4 Channel 1 Master Clock Output**
	CCU60_CC61INB	I	St/B	**CCU60 Channel 1 Input**
	RxDC1F	I	St/B	**CAN Node 1 Receive Data Input**
15	P8.0	O0 / I	St/B	**Bit 0 of Port 8, General Purpose Input/Output**
	CCU60_CC60	O1	St/B	**CCU60 Channel 0 Output**
	CC1_CC0	O2	St/B	**CC1 Channel 0 Output**
	U4C1_SELO1	O3	St/B	**USIC4 Channel 1 Select/Control 1 Output**
	CCU60_CC60INB	I	St/B	**CCU60 Channel 0 Input**
18	P6.0	O0 / I	DA/A	**Bit 0 of Port 6, General Purpose Input/Output**
	EMUX0	O1	DA/A	**External Analog MUX Control Output 0 (ADC0)**
	TxDC2	O2	DA/A	**CAN Node 2 Transmit Data Output**
	$\overline{\text{BRKOUT}}$	O3	DA/A	**OCDS Break Signal Output**
	ADCx_REQGTyG	I	DA/A	**External Request Gate Input for ADC0/1**
	U1C1_DX0E	I	DA/A	**USIC1 Channel 1 Shift Data Input**
19	P6.1	O0 / I	DA/A	**Bit 1 of Port 6, General Purpose Input/Output**
	EMUX1	O1	DA/A	**External Analog MUX Control Output 1 (ADC0)**
	T3OUT	O2	DA/A	**GPT12E Timer T3 Toggle Latch Output**
	U1C1_DOUT	O3	DA/A	**USIC1 Channel 1 Shift Data Output**
	ADCx_REQTRyE	I	DA/A	**External Request Trigger Input for ADC0/1**
	RxDC2E	I	DA/A	**CAN Node 2 Receive Data Input**
	ESR1_6	I	DA/A	**ESR1 Trigger Input 6**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
78	P4.1	O0 / I	St/B	**Bit 1 of Port 4, General Purpose Input/Output**
	U3C0_SELO 3	O1	St/B	**USIC3 Channel Select/Control 3 Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	CC2_CC25	O3 / I	St/B	**CAPCOM2 CC25IO Capture Inp./ Compare Out.**
	$\overline{\text{CS1}}$	OH	St/B	**External Bus Interface Chip Select 1 Output**
	CCU62_CCP OS0B	I	St/B	**CCU62 Position Input 0**
	T4EUDB	I	St/B	**GPT12E Timer T4 External Up/Down Control Input**
	ESR1_8	I	St/B	**ESR1 Trigger Input 8**
79	P2.4	O0 / I	St/B	**Bit 4 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_CC17	O3 / I	St/B	**CAPCOM2 CC17IO Capture Inp./ Compare Out.**
	A17	OH	St/B	**External Bus Interface Address Line 17**
	ESR1_0	I	St/B	**ESR1 Trigger Input 0**
	U0C0_DX0F	I	St/B	**USIC0 Channel 0 Shift Data Input**
	RxDC1A	I	St/B	**CAN Node 1 Receive Data Input**
80	P11.1	O0 / I	St/B	**Bit 1 of Port 11, General Purpose Input/Output**
	CCU61_COU T61	O1	St/B	**CCU61 Channel 1 Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	U3C1_SELO 0	O3	St/B	**USIC3 Channel 1 Select/Control 0 Output**
	CCU63_CCP OS1A	I	St/B	**CCU63 Position Input 1**
	CCU61_CTR APD	I	St/B	**CCU61 Emergency Trap Input**
	U3C1_DX2A	I	St/B	**USIC3 Channel 1 Shift Control Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
103	P3.0	O0 / I	St/B	**Bit 0 of Port 3, General Purpose Input/Output**
	U2C0_DOUT	O1	St/B	**USIC2 Channel 0 Shift Data Output**
	ESR1_1	I	St/B	**ESR1 Trigger Input 1**
	U2C0_DX0A	I	St/B	**USIC2 Channel 0 Shift Data Input**
	RxDC3B	I	St/B	**CAN Node 3 Receive Data Input**
	U2C0_DX1A	I	St/B	**USIC2 Channel 0 Shift Clock Input**
104	P12.5	O0 / I	St/B	**Bit 5 of Port 12, General Purpose Input/Output**
	CC1_CC5	O1 / I	St/B	**CAPCOM1 CC5IO Capture Inp./ Compare Out.**
	U4C0_SCLKOUT	O2	St/B	**USIC4 Channel 0 Shift Clock Output**
	TxDC3	O3	St/B	**CAN Node 3 Transmit Data Output**
	CCU63_CCPOS2B	I	St/B	**CCU63 Position Input 2**
	U4C0_DX1E	I	St/B	**USIC4 Channel 0 Shift Clock Input**
105	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_CC61	O2	St/B	**CCU60 Channel 1 Output**
	AD1	OH / IH	St/B	**External Bus Interface Address/Data Line 1**
	CCU60_CC61INA	I	St/B	**CCU60 Channel 1 Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
148	P13.2	O0 / I	St/B	**Bit 2 of Port 13, General Purpose Input/Output**
	CC1_CC10	O1 / I	St/B	**CAPCOM1 CC10IO Capture Inp./ Compare Out.**
	CCU60_CC61	O2	St/B	**CCU60 Channel 1Output**
	U3C0_DOUT	O3	St/B	**USIC3 Channel 0 Shift Data Output**
	T3EUDC	I	St/B	**GPT12E Timer T3 External Up/Down Control Input**
	CCU60_CC61INC	I	St/B	**CCU60 Channel 2 Input**
	U4C1_DX1B	I	St/B	**USIC4 Channel 0 Shift Control Input**
149	P9.3	O0 / I	St/B	**Bit 3 of Port 9, General Purpose Input/Output**
	CCU63_COUT60	O1	St/B	**CCU63 Channel 0 Output**
	$\overline{\text{BRKOUT}}$	O2	St/B	**OCDS Break Signal Output**
150	P10.13	O0 / I	St/B	**Bit 13 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC3	O2	St/B	**CAN Node 3 Transmit Data Output**
	U1C0_SELO3	O3	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	$\overline{\text{WR}}$/$\overline{\text{WRL}}$	OH	St/B	**External Bus Interface Write Strobe Output** Active for each external write access, when $\overline{\text{WR}}$, active for ext. writes to the low byte, when $\overline{\text{WRL}}$.
	U1C0_DX0D	I	St/B	**USIC1 Channel 0 Shift Data Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
170	$\overline{\text{ESR1}}$	O0 / I	St/B	**External Service Request 1** After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC0E	I	St/B	**CAN Node 0 Receive Data Input**
	U1C0_DX0F	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2C	I	St/B	**USIC1 Channel 0 Shift Control Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2B	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX2C	I	St/B	**USIC2 Channel 1 Shift Control Input**
171	$\overline{\text{ESR2}}$	O0 / I	St/B	**External Service Request 2** After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC1E	I	St/B	**CAN Node 1 Receive Data Input**
	CCU60_CTRAPC	I	St/B	**CCU60 Emergency Trap Input**
	CCU61_CTRAPC	I	St/B	**CCU61 Emergency Trap Input**
	CCU62_CTRAPC	I	St/B	**CCU62 Emergency Trap Input**
	CCU63_CTRAPC	I	St/B	**CCU63 Emergency Trap Input**
	U1C1_DX0D	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2C	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX0E	I	St/B	**USIC2 Channel 1 Shift Data Input**
	U2C1_DX2B	I	St/B	**USIC2 Channel 1 Shift Control Input**
172	$\overline{\text{ESR0}}$	O0 / I	St/B	**External Service Request 0** After power-up, $\overline{\text{ESR0}}$ operates as open-drain bidirectional reset with a weak pull-up.
	U1C0_DX0E	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2B	I	St/B	**USIC1 Channel 0 Shift Control Input**

Up to 24 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

8 Kbytes of on-chip Stand-By SRAM (SBRAM) provide storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see **Table 7**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

The on-chip Flash memory stores code, constant data, and control data. The 1,600 Kbytes of on-chip Flash memory consist of 1 module of 64 Kbytes (preferably for data storage) and 6 modules of 256 Kbytes. Each module is organized in 4-Kbyte sectors.
The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen device type.

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.6**.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

Memory Content Protection

The contents of on-chip memories can be protected against soft errors (induced e.g. by radiation) by activating the parity mechanism or the Error Correction Code (ECC).
The parity mechanism can detect a single-bit error and prevent the software from using incorrect data or executing incorrect instructions.
The ECC mechanism can detect and automatically correct single-bit errors. This supports the stable operation of the system.

It is strongly recommended to activate the ECC mechanism wherever possible because this dramatically increases the robustness of an application against such soft errors.

With this hardware most XE169xH instructions are executed in a single machine cycle of 10 ns @ 100-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, no matter how many bits are shifted. Also, multiplication and most MAC instructions execute in one cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast; for example, a 32-/16-bit division is started within 4 cycles while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, eliminates the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word-wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided for storage of temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area); it is accessed by the CPU with the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared with the stack pointer value during each stack access to detect stack overflow or underflow.

The high performance of the CPU hardware implementation can be best utilized by the programmer with the highly efficient XE169xH instruction set. This includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE169xH to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

7) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pins leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \ K_{OV})$. The additional error current may distort the input voltage on analog inputs.
8) Value is controlled by on-chip regulator

Table 17 Switching Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT} CC	–	25 + 0.9 x f_{SYS} [1]	25 + 1.4 x f_{SYS} [1]	mA	power_mode= active ; voltage_range= both [2][3][4]
Power supply current in stopover mode, EVVRs on	I_{SSO} CC	–	1.4	4.0	mA	power_mode= stopover ; voltage_range= both [4]

1) f_{SYS} in MHz

2) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched. In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 0.6 x f_{SYS}.

3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

4) The pad supply voltage has only a minor influence on this parameter.

Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XE169xH's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.
A small current is consumed because the drivers' input stages are switched.

The IO power domains can be supplied separately. Power domain A (V_{DDPA}) supplies the A/D converters and Port 6. Power domain B (V_{DDPB}) supplies the on-chip EVVRs and all other ports.

During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from V_{DDPA}.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 0.6×f_{SYS} mA.

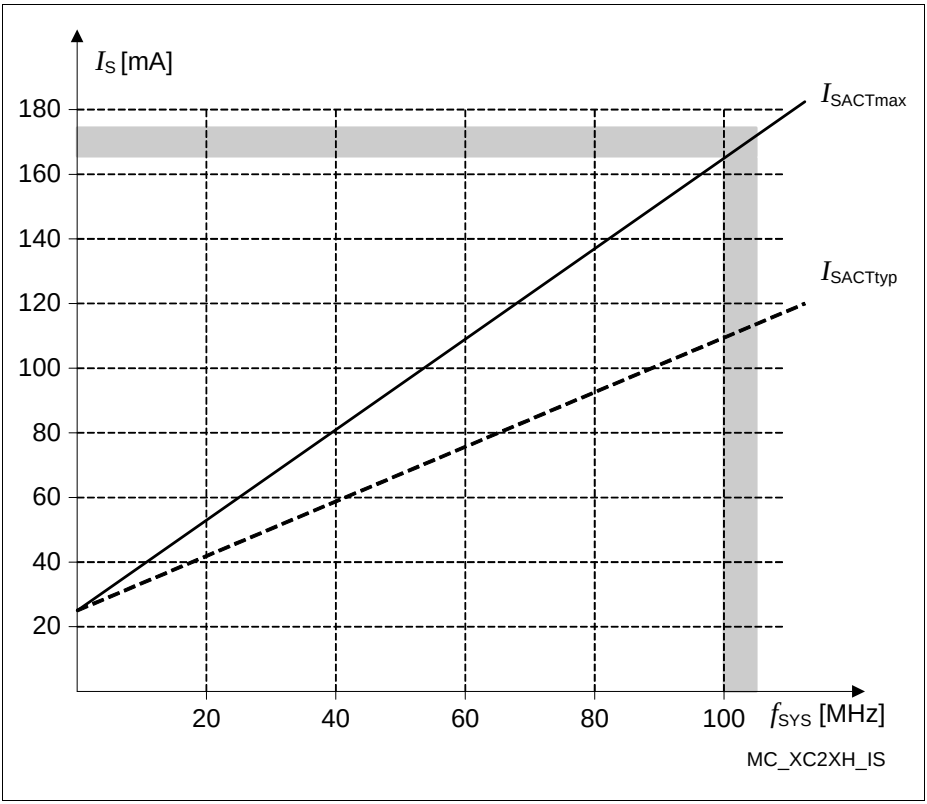

Figure 14 Supply Current in Active Mode as a Function of Frequency

Note: Operating Conditions apply.

Table 18 Leakage Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Leakage supply current[1)2)]	I_{LK1} CC	–	0.04	0.06	mA	T_J= 25 °C
		–	0.7	1.8	mA	T_J= 85 °C
		–	3.1	8.6	mA	T_J= 125 °C
		–	6.6	19.2	mA	T_J= 150 °C

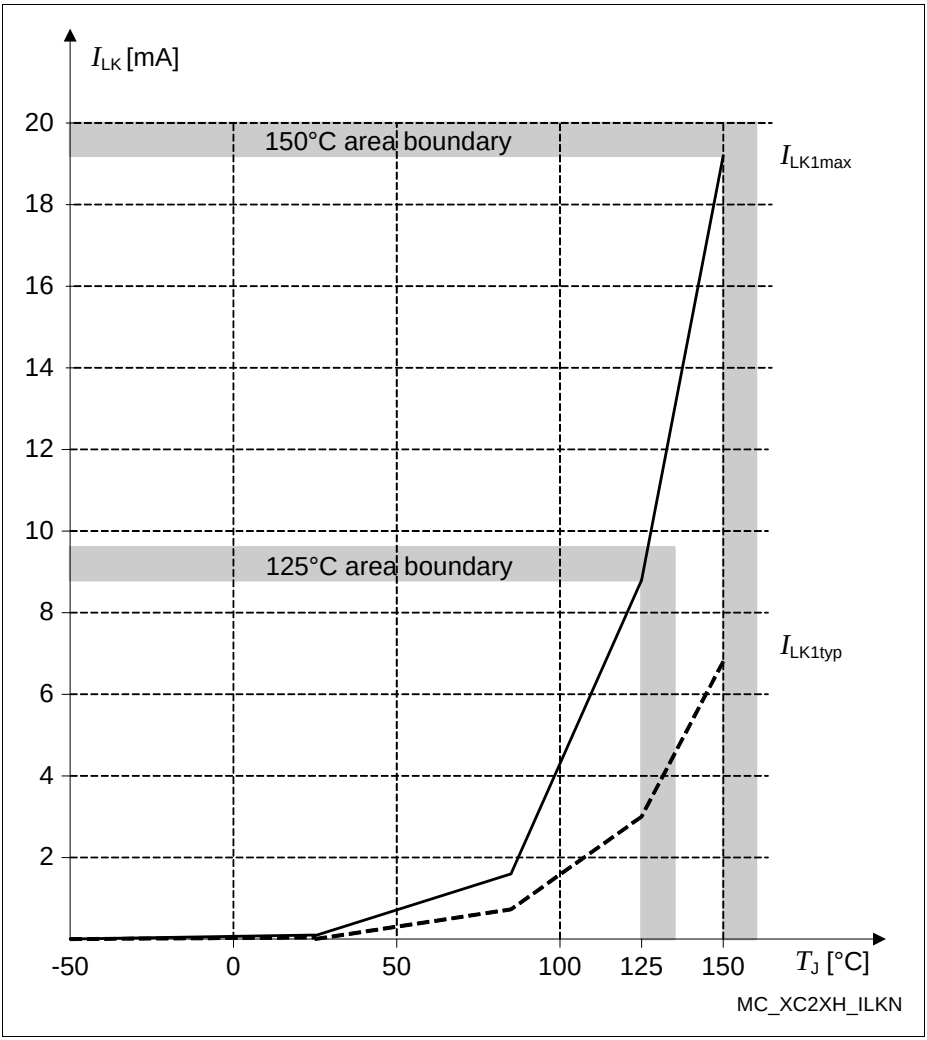

Figure 15 Leakage Supply Current as a Function of Temperature

Table 22 Coding of bit fields LEVxV in Register SWDCON0 (cont'd)

Code	Default Voltage Level	Notes[1)]
1010_B	4.6 V	
1011_B	4.7 V	
1100_B	4.8 V	
1101_B	4.9 V	
1110_B	5.0 V	
1111_B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Table 23 Coding of bit fields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes[1)]
000_B	0.95 V	
001_B	1.05 V	
010_B	1.15 V	
011_B	1.25 V	
100_B	1.35 V	LEV1V: reset request
101_B	1.45 V	LEV2V: interrupt request [2)]
110_B	1.55 V	
111_B	1.65 V	

1) The indicated default levels are selected automatically after a power reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and the PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.

1) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.
2) Overload conditions must not occur on pin XTAL1.

Note: For crystal or ceramic resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation.
The manufacturers of crystals and ceramic resonators offer an oscillator evaluation service. This evaluation checks the crystal/resonator specification limits to ensure a reliable oscillator operation.

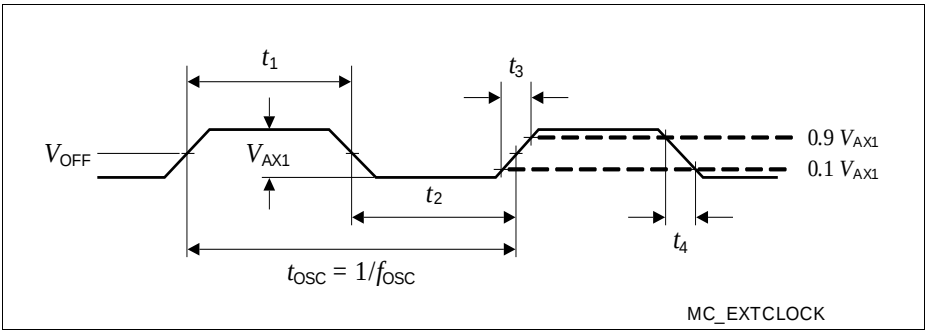

Figure 21 External Clock Drive XTAL1

4.7.5 External Bus Timing

The following parameters specify the behavior of the XE169xH bus interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 29 Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CLKOUT Cycle Time[1)]	t_5 CC	–	1 / f_{SYS}	–	ns	
CLKOUT high time	t_6 CC	2	–	–		
CLKOUT low time	t_7 CC	2	–	–		
CLKOUT rise time	t_8 CC	–	–	3	ns	
CLKOUT fall time	t_9 CC	–	–	3		

1) The CLKOUT cycle time is influenced by PLL jitter. For longer periods the relative deviation decreases (see PLL deviation formula).

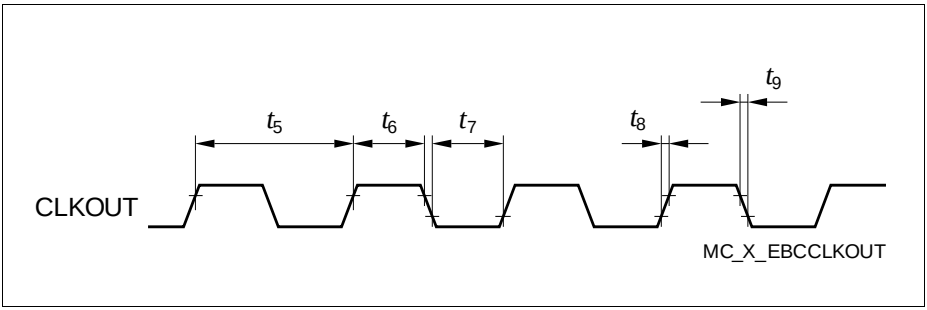

Figure 22 CLKOUT Signal Timing

Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

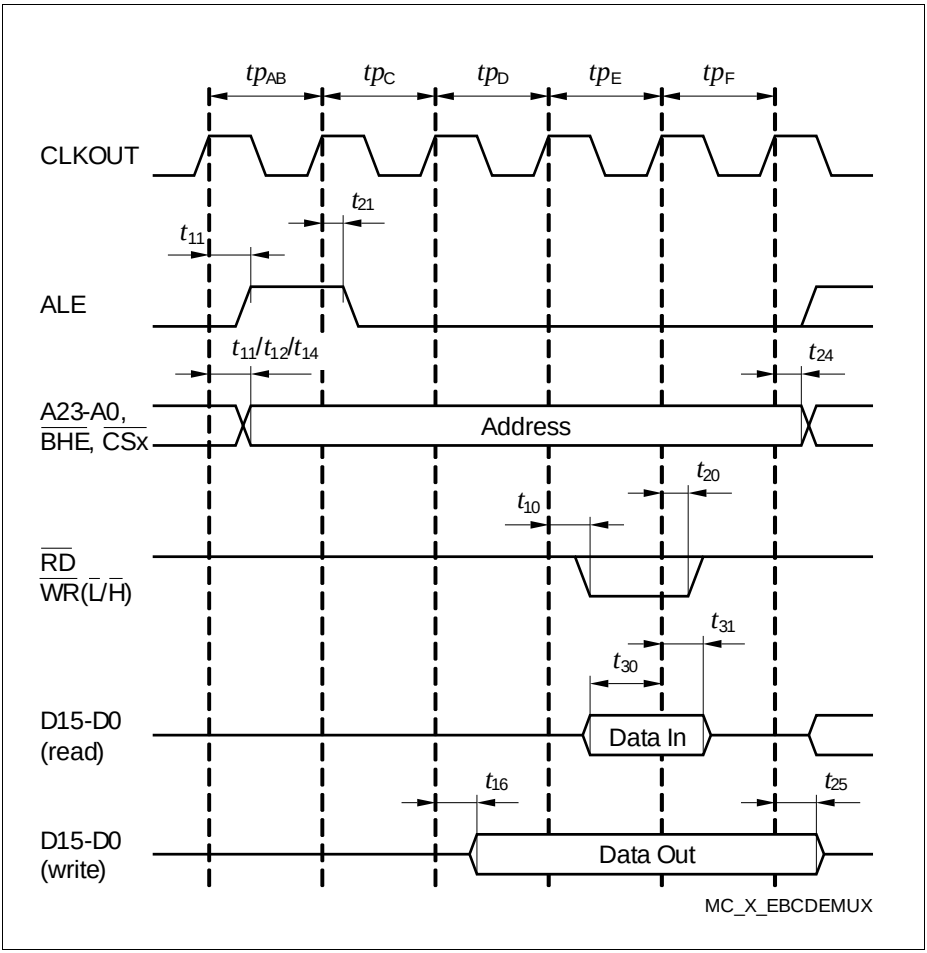

Figure 24 Demultiplexed Bus Cycle

4.7.5.1 Bus Cycle Control with the READY Input

The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum

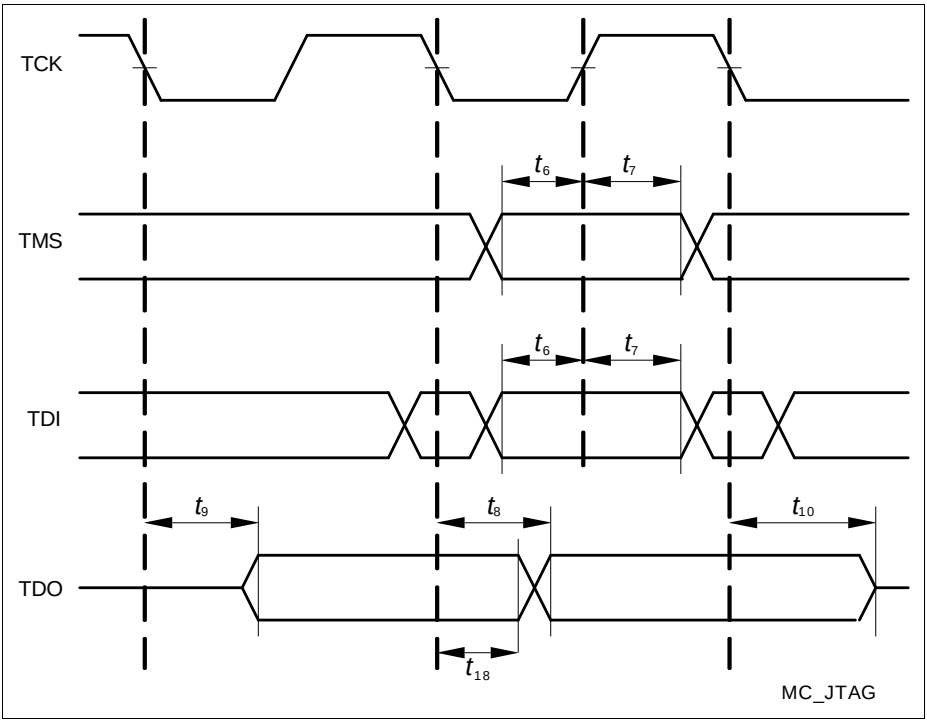

Figure 31 JTAG Timing

5.3 Quality Declarations

The operation lifetime of the XE169xH depends on the operating temperature. The life time decreases with increasing temperature as shown in **Table 43**.

Table 42 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	–	–	20	a	See **Table 43**
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020C

Table 43 Lifetime dependency from Temperature

Operating Time	Operating Temperature
20 a	$T_J \leq 110°C$
95 500 h	$T_J = 120°C$
68 500 h	$T_J = 125°C$
49 500 h	$T_J = 130°C$
26 400 h	$T_J = 140°C$
14 500 h	$T_J = 150°C$