# Infineon Technologies - XE169FH200F100LABKXUMA1 Datasheet

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | C166SV2 |
| Core Size | 16-Bit |
| Speed | 100MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | I²S, POR, PWM, WDT |
| Number of I/O | 118 |
| Program Memory Size | 1.6MB (1.6M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 112K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 30x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-176-12 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xe169fh200f100labkxuma1 |

**XE169xH Data Sheet**
**Revision History: V1.3 2011-07**

Previous Versions:
V1.2, 2010-09
V1.1, 2010-02 Preliminary

| Page | Subjects (major changes since last revision) |
|---|---|
| **10** | Clarified available Flash and SRAM memory allocation. |
| **82** | USIC “QSPI” protocol shortcut removed due to ambiguity (interpreted as Queued SPI or Quad SPI). |
| **110** | Relaxed the conditions for short-term deviation of internal clock source frequency $\Delta f_{INT}$. |
| **110** | Added startup time from power-on $t_{SPO}$ |
| **113** | Removed the 128MHz conditions for $N_{WSFLE}$ |
| **120** | Added the minimum PLL free running frequency. Reduced the min/max bandwidth. |
| **145** | Thermal resistance values updated. |

**Trademarks**

C166™, TriCore™ and DAVE™ are trademarks of Infineon Technologies AG.

**We Listen to Your Comments**
Is there any information in this document that you feel is wrong, unclear or missing? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
**mcdocu.comments@infineon.com**

## 1.2 Definition of Feature Variants

The XE169xH types are offered with several Flash memory sizes. **Table 2** and **Table 3** describe the location of the available Flash memory.

**Table 2 Continuous Flash Memory Ranges**

| Total Flash Size | 1st Range[1)] | 2nd Range | 3rd Range |
|---|---|---|---|
| 1,600 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $D8'FFFF_H$ | n.a. |
| 1,088 Kbytes | $C0'0000_H$ … $C0'EFFF_H$ | $C1'0000_H$ … $CF'FFFF_H$ | $D8'0000_H$ … $D8'FFFF_H$ |

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

**Table 3 Flash Memory Module Allocation (in Kbytes)**

| Total Flash Size | Flash 0[1)] | Flash 1 | Flash 2 | Flash 3 | Flash 4 | Flash 5 | Flash 6 |
|---|---|---|---|---|---|---|---|
| 1,600 | 256 | 255 | 256 | 256 | 256 | 256 | 64 |
| 1,088 | 256 | 255 | 256 | 256 | - | - | 64 |

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XE169xH types are offered with different interface options. **Table 4** lists the available channels for each option.

**Table 4 Interface Channel Association**

| Total Number | Available Channels / Message Objects |
|---|---|
| 16 ADC0 channels | CH0 … CH15 |
| 14 ADC1 channels | CH0 … CH7, CH16 … CH21 |
| 6 CAN nodes | CAN0, CAN1, CAN2, CAN3, CAN4, CAN5<br>256 message objects |
| 10 serial channels | U0C0, U0C1, U1C0, U1C1, U2C0, U2C1, U3C0, U3C1, U4C0, U4C1 |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 8 | P7.0 | O0 / I | St/B | **Bit 0 of Port 7, General Purpose Input/Output** |
| | T3OUT | O1 | St/B | **GPT12E Timer T3 Toggle Latch Output** |
| | T6OUT | O2 | St/B | **GPT12E Timer T6 Toggle Latch Output** |
| | TDO_A | OH / IH | St/B | **JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it. |
| | ESR2_1 | I | St/B | **ESR2 Trigger Input 1** |
| | RxDC4B | I | St/B | **CAN Node 4 Receive Data Input** |
| | U4C1_DX0C | I | St/B | **USIC4 Channel 0 Receive Data Input** |
| 9 | P7.3 | O0 / I | St/B | **Bit 3 of Port 7, General Purpose Input/Output** |
| | EMUX1 | O1 | St/B | **External Analog MUX Control Output 1 (ADC1)** |
| | U0C1_DOUT | O2 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U0C0_DOUT | O3 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | CCU62_CCPOS1A | I | St/B | **CCU62 Position Input 1** |
| | TMS_C | IH | St/B | **JTAG Test Mode Selection Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it. |
| | U0C1_DX0F | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| 10 | P8.2 | O0 / I | St/B | **Bit 2 of Port 8, General Purpose Input/Output** |
| | CCU60_CC62 | O1 | St/B | **CCU60 Channel 2 Output** |
| | TxDC1 | O2 | St/B | **CAN Node 1 Transmit Data Output** |
| | U1C1_DOUT | O3 | St/B | **USIC1 Channel 1 Shift Data output** |
| | CCU60_CC62INB | I | St/B | **CCU60 Channel 2 Input** |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 106 | P0.3 | O0 / I | St/B | **Bit 3 of Port 0, General Purpose Input/Output** |
| | U1C0_SELO 0 | O1 | St/B | **USIC1 Channel 0 Select/Control 0 Output** |
| | U1C1_SELO 1 | O2 | St/B | **USIC1 Channel 1 Select/Control 1 Output** |
| | CCU61_COU T60 | O3 | St/B | **CCU61 Channel 0 Output** |
| | A3 | OH | St/B | **External Bus Interface Address Line 3** |
| | U1C0_DX2A | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| | RxDC0B | I | St/B | **CAN Node 0 Receive Data Input** |
| 107 | P3.1 | O0 / I | St/B | **Bit 1 of Port 3, General Purpose Input/Output** |
| | U2C0_DOUT | O1 | St/B | **USIC2 Channel 0 Shift Data Output** |
| | TxDC3 | O2 | St/B | **CAN Node 3 Transmit Data Output** |
| | U2C0_DX0B | I | St/B | **USIC2 Channel 0 Shift Data Input** |
| 108 | P12.4 | O0 / I | St/B | **Bit 4 of Port 12, General Purpose Input/Output** |
| | CC1_CC4 | O1 / I | St/B | **CAPCOM1 CC4IO Capture Inp./ Compare Out.** |
| | U4C0_SELO 3 | O2 | St/B | **USIC4 Channel 0 Master Clock Output** |
| | CCU63_T12 HRF | I | St/B | **External Run Control Input for T12 of CCU63** |
| 109 | P10.2 | O0 / I | St/B | **Bit 2 of Port 10, General Purpose Input/Output** |
| | U0C0_SCLK OUT | O1 | St/B | **USIC0 Channel 0 Shift Clock Output** |
| | CCU60_CC6 2 | O2 | St/B | **CCU60 Channel 2 Output** |
| | U3C0_SELO 1 | O3 | St/B | **USIC3 Channel 0 Select/Control 1 Output** |
| | AD2 | OH / IH | St/B | **External Bus Interface Address/Data Line 2** |
| | CCU60_CC6 2INA | I | St/B | **CCU60 Channel 2 Input** |
| | U0C0_DX1B | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| | U3C0_DX2B | I | St/B | **USIC3 Channel 0 Shift Control Input** |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 143 | P10.11 | O0 / I | St/B | **Bit 11 of Port 10, General Purpose Input/Output** |
| | U1C0_SCLKOUT | O1 | St/B | **USIC1 Channel 0 Shift Clock Output** |
| | $\overline{\text{BRKOUT}}$ | O2 | St/B | **OCDS Break Signal Output** |
| | U3C0_SELO0 | O3 | St/B | **USIC3 Channel 0 Select/Control 0 Output** |
| | AD11 | OH / IH | St/B | **External Bus Interface Address/Data Line 11** |
| | U1C0_DX1D | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| | RxDC2B | I | St/B | **CAN Node 2 Receive Data Input** |
| | TMS_B | IH | St/B | **JTAG Test Mode Selection Input**<br>If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. |
| | U3C0_DX2A | I | St/B | **USIC3 Channel 0 Shift Control Input** |
| 144 | P13.1 | O0 / I | St/B | **Bit 1 of Port 13, General Purpose Input/Output** |
| | T3OUT | O1 | St/B | **GPT12E Timer T3 Toggle Latch Output** |
| | CCU60_CC62 | O2 | St/B | **CCU60 Channel 2 Output** |
| | TxDC4 | O3 | St/B | **CAN Node 4 Transmit Data Output** |
| | U3C0_DX0D | I | St/B | **USIC3 Channel 0 Shift Data Input** |
| | CCU60_CC62INC | I | St/B | **CCU60 Channel 2 Input** |
| | U4C1_DX2B | I | St/B | **USIC4 Channel 1 Shift Control Input** |
| | TxDC4 | O3 | St/B | **CAN Node 4 transmit Data Output** |
| 145 | P9.2 | O0 / I | St/B | **Bit 2 of Port 9, General Purpose Input/Output** |
| | CCU63_CC62 | O1 | St/B | **CCU63 Channel 2 Output** |
| | CC1_CC4 | O2 | St/B | **CAPCOM1 CC4 Compare Output** |
| | CCU63_CC62INA | I | St/B | **CCU63 Channel 2 Input** |
| | CAPINB | I | St/B | **GPT12E Register CAPREL Capture Input** |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 148 | P13.2 | O0 / I | St/B | **Bit 2 of Port 13, General Purpose Input/Output** |
| | CC1_CC10 | O1 / I | St/B | **CAPCOM1 CC10IO Capture Inp./ Compare Out.** |
| | CCU60_CC61 | O2 | St/B | **CCU60 Channel 1Output** |
| | U3C0_DOUT | O3 | St/B | **USIC3 Channel 0 Shift Data Output** |
| | T3EUDC | I | St/B | **GPT12E Timer T3 External Up/Down Control Input** |
| | CCU60_CC61INC | I | St/B | **CCU60 Channel 2 Input** |
| | U4C1_DX1B | I | St/B | **USIC4 Channel 0 Shift Control Input** |
| 149 | P9.3 | O0 / I | St/B | **Bit 3 of Port 9, General Purpose Input/Output** |
| | CCU63_COUT60 | O1 | St/B | **CCU63 Channel 0 Output** |
| | $\overline{\text{BRKOUT}}$ | O2 | St/B | **OCDS Break Signal Output** |
| 150 | P10.13 | O0 / I | St/B | **Bit 13 of Port 10, General Purpose Input/Output** |
| | U1C0_DOUT | O1 | St/B | **USIC1 Channel 0 Shift Data Output** |
| | TxDC3 | O2 | St/B | **CAN Node 3 Transmit Data Output** |
| | U1C0_SELO3 | O3 | St/B | **USIC1 Channel 0 Select/Control 3 Output** |
| | $\overline{\text{WR}}$/$\overline{\text{WRL}}$ | OH | St/B | **External Bus Interface Write Strobe Output** Active for each external write access, when $\overline{\text{WR}}$, active for ext. writes to the low byte, when $\overline{\text{WRL}}$. |
| | U1C0_DX0D | I | St/B | **USIC1 Channel 0 Shift Data Input** |

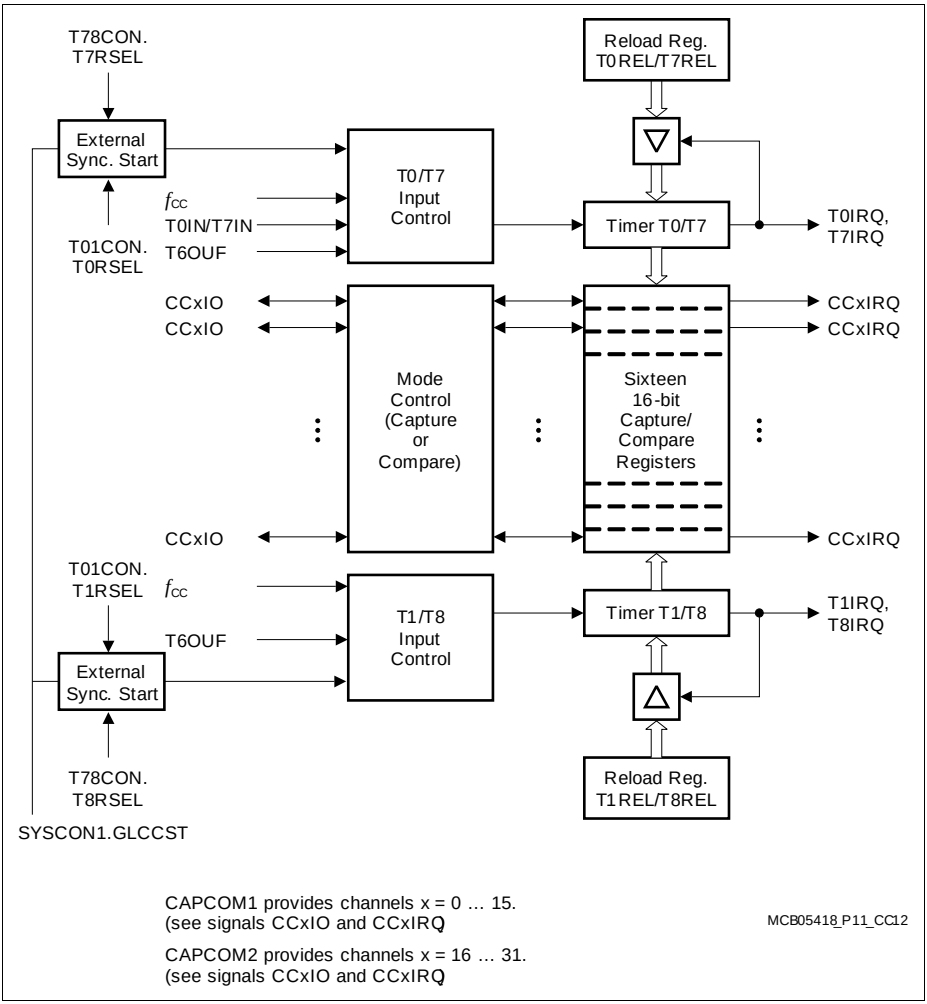


**Figure 6 CAPCOM Unit Block Diagram**

## 3.9 Capture/Compare Units CCU6x

The XE169xH types feature the CCU60, CCU61, CCU62 and CCU63 unit(s).

CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

**Timer 12 Features**

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

**Timer 13 Features**

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

**Additional Features**

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

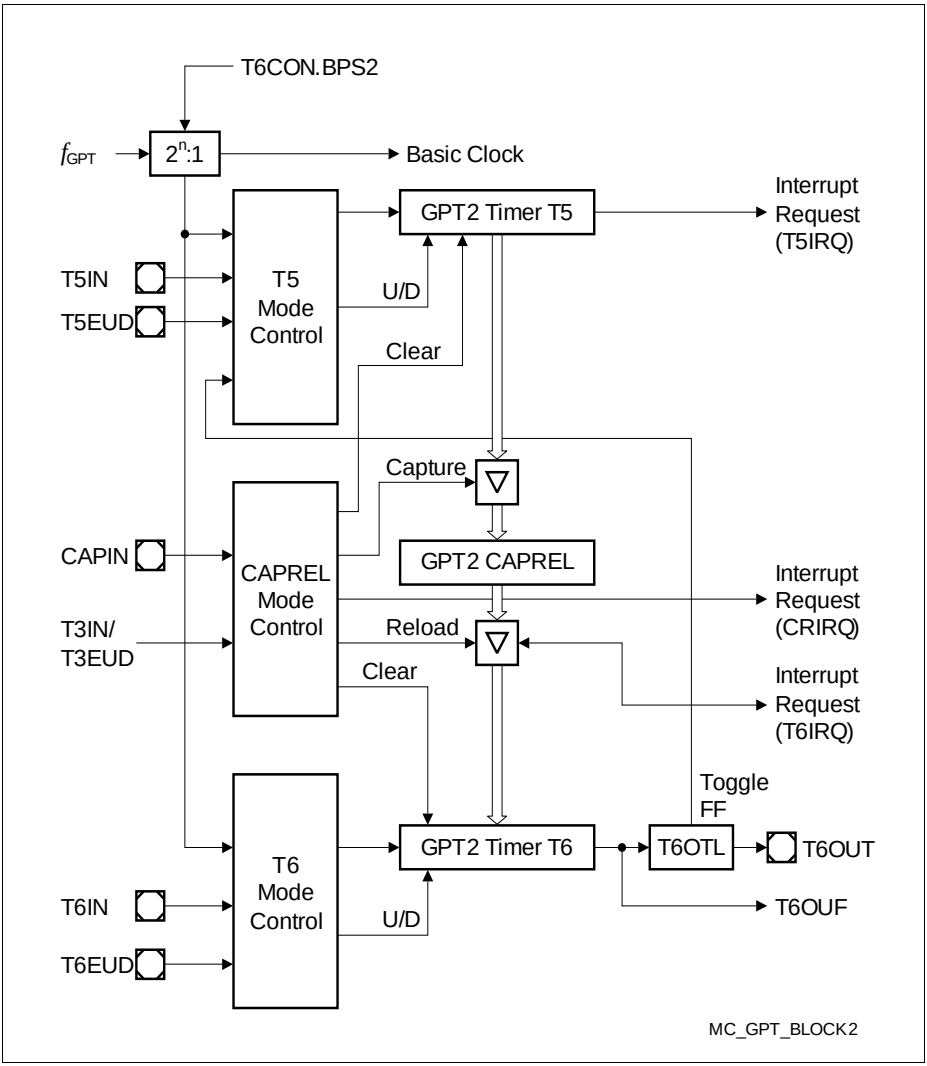


**Figure 9 Block Diagram of GPT2**

## 3.13 Universal Serial Interface Channel Modules (USIC)

The XE169xH features the USIC modules USIC0, USIC1, USIC2, USIC3, USIC4. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

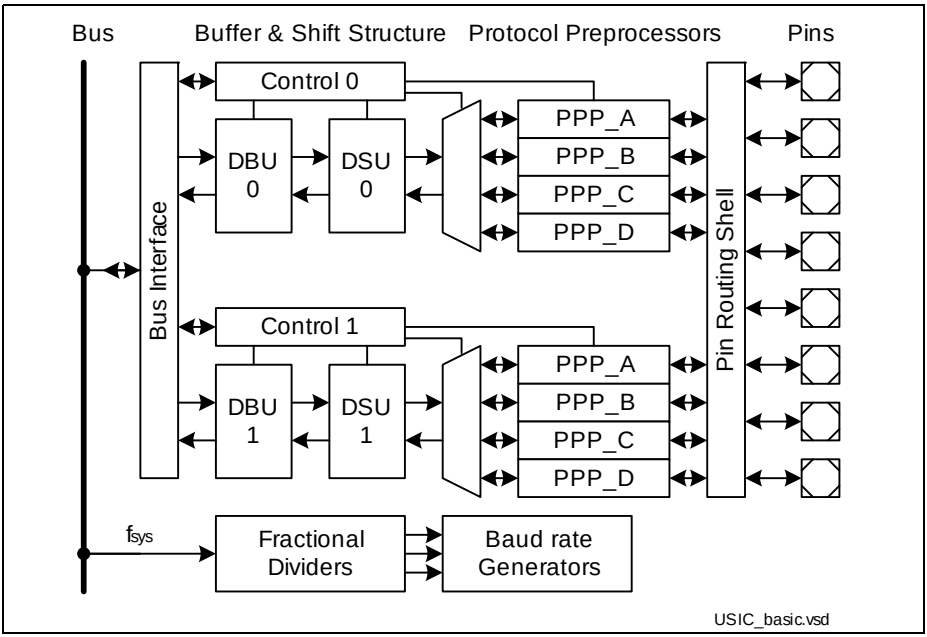


**Figure 11 General Structure of a USIC Module**

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

## 3.19 Instruction Set Summary

Table 10 lists the instructions of the XE169xH.
The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

**Table 10 Instruction Set Summary**

| Mnemonic | Description | Bytes |
|---|---|---|
| ADD(B) | Add word (byte) operands | 2 / 4 |
| ADDC(B) | Add word (byte) operands with Carry | 2 / 4 |
| SUB(B) | Subtract word (byte) operands | 2 / 4 |
| SUBC(B) | Subtract word (byte) operands with Carry | 2 / 4 |
| MUL(U) | (Un)Signed multiply direct GPR by direct GPR (16- × 16-bit) | 2 |
| DIV(U) | (Un)Signed divide register MDL by direct GPR (16-/16-bit) | 2 |
| DIVL(U) | (Un)Signed long divide reg. MD by direct GPR (32-/16-bit) | 2 |
| CPL(B) | Complement direct word (byte) GPR | 2 |
| NEG(B) | Negate direct word (byte) GPR | 2 |
| AND(B) | Bitwise AND, (word/byte operands) | 2 / 4 |
| OR(B) | Bitwise OR, (word/byte operands) | 2 / 4 |
| XOR(B) | Bitwise exclusive OR, (word/byte operands) | 2 / 4 |
| BCLR/BSET | Clear/Set direct bit | 2 |
| BMOV(N) | Move (negated) direct bit to direct bit | 4 |
| BAND/BOR/BXOR | AND/OR/XOR direct bit with direct bit | 4 |
| BCMP | Compare direct bit to direct bit | 4 |
| BFLDH/BFLDL | Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data | 4 |
| CMP(B) | Compare word (byte) operands | 2 / 4 |
| CMPD1/2 | Compare word data to GPR and decrement GPR by 1/2 | 2 / 4 |
| CMPI1/2 | Compare word data to GPR and increment GPR by 1/2 | 2 / 4 |
| PRIOR | Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR | 2 |
| SHL/SHR | Shift left/right direct word GPR | 2 |

### 4.3.3 Power Consumption

The power consumed by the XE169xH depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current $I_S$ depends on the device activity
- The leakage current $I_{LK}$ depends on the device temperature

To determine the actual power consumption, always both components, switching current $I_S$ and leakage current $I_{LK}$ must be added:

$I_{DDP} = I_S + I_{LK}$.

*Note: The power consumption values are not subject to production test. They are verified by design/characterization.*
*To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.*

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.

*Note: The maximum values cover the complete specified operating range of all manufactured devices.*
*The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.*
*After a power reset, the decoupling capacitors for $V_{DDIM}$ and $V_{DDI1}$ are charged with the maximum possible current.*

For additional information, please refer to **Section 5.2**, **Thermal Considerations**.

*Note: Operating Conditions apply.*

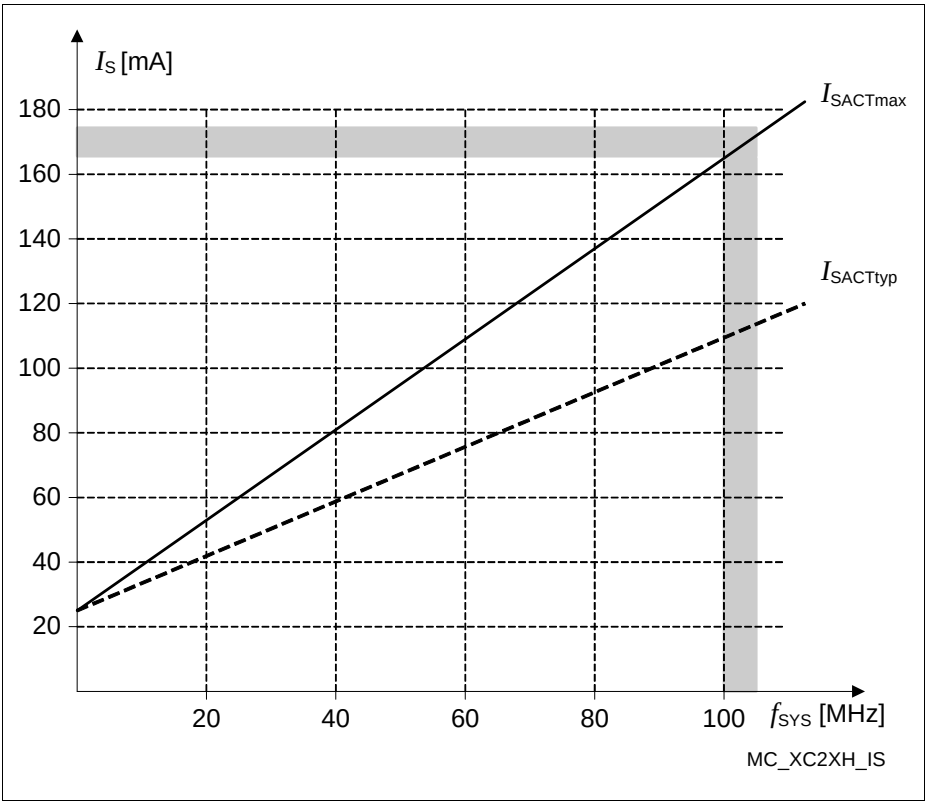


**Figure 14 Supply Current in Active Mode as a Function of Frequency**

*Note: Operating Conditions apply.*

**Table 18 Leakage Power Consumption**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Leakage supply current[1)2)] | $I_{LK1}$ CC | – | 0.04 | 0.06 | mA | $T_J$= 25 °C |
| | | – | 0.7 | 1.8 | mA | $T_J$= 85 °C |
| | | – | 3.1 | 8.6 | mA | $T_J$= 125 °C |
| | | – | 6.6 | 19.2 | mA | $T_J$= 150 °C |

1) The supply current caused by leakage depends mainly on the junction temperature and the supply voltage. The temperature difference between the junction temperature $T_J$ and the ambient temperature $T_A$ must be taken into account. As this fraction of the supply current does not depend on device activity, it must be added to other power consumption values.
2) All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at $V_{DDP}$ - 0.1 V to $V_{DDP}$ and all outputs (including pins configured as outputs) are disconnected.

*Note: A fraction of the leakage current flows through domain DMP_A (pin $V_{DDPA}$). This current can be calculated as 7,000 $\times e^{-\alpha}$, with $\alpha$ = 5000 / (273 + 1.3 $\times T_J$). For $T_J$ = 150°C, this results in a current of 160 $\mu$A.*

The leakage power consumption can be calculated according to the following formulas:

$I_{LK1} = 600{,}000 \times e^{-\alpha}$ with $\alpha = 5000 / (273 + B \times T_J)$

Parameter B must be replaced by

- 1.1 for typical values
- 1.4 for maximum values

## 4.4 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

*Note: Operating Conditions apply.*

**Table 19 ADC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Switched capacitance at an analog input | $C_{AINSW}$ CC | – | – | 6 | pF | not subject to production test |
| Total capacitance at an analog input | $C_{AINT}$ CC | – | – | 14 | pF | not subject to production test |
| Switched capacitance at the reference input | $C_{AREFSW}$ CC | – | – | 10 | pF | not subject to production test |
| Total capacitance at the reference input | $C_{AREFT}$ CC | – | – | 21 | pF | not subject to production test |
| Differential Non-Linearity Error | $\lvert EA_{DNL}\rvert$ CC | – | 0.8 | 1 | LSB | |
| Gain Error | $\lvert EA_{GAIN}\rvert$ CC | – | 0.4 | 0.8 | LSB | |
| Integral Non-Linearity | $\lvert EA_{INL}\rvert$ CC | – | 0.8 | 1.2 | LSB | |
| Offset Error | $\lvert EA_{OFF}\rvert$ CC | – | 0.5 | 0.8 | LSB | |
| Analog clock frequency | $f_{ADCI}$ SR | 0.5 | – | 16.5 | MHz | voltage_range= lower |
| | | 0.5 | – | 20 | MHz | voltage_range= upper |
| Input resistance of the selected analog channel | $R_{AIN}$ CC | – | – | 2 | kOhm | not subject to production test |
| Input resistance of the reference input | $R_{AREF}$ CC | – | – | 2 | kOhm | not subject to production test |

## 4.7 AC Parameters

These parameters describe the dynamic behavior of the XE169xH.

### 4.7.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

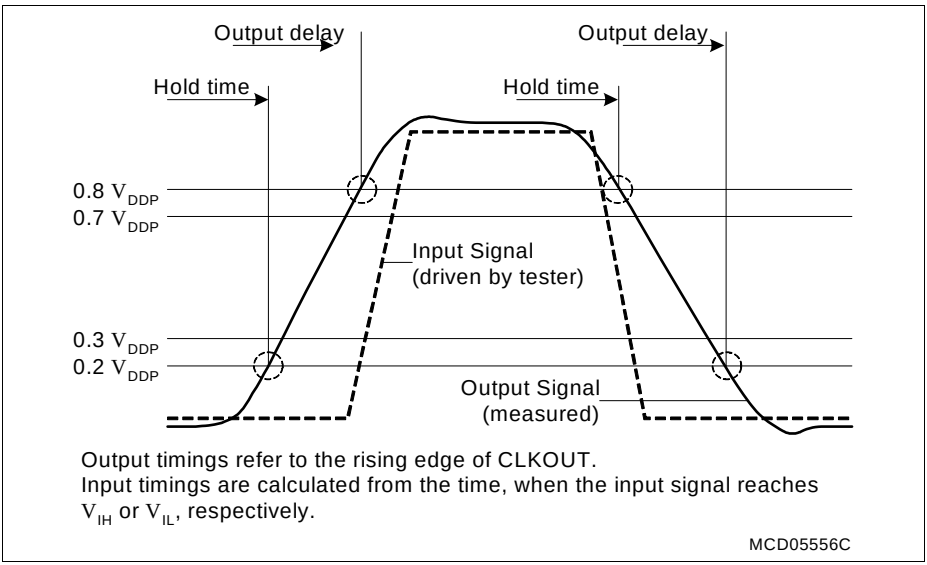


**Figure 17 Input Output Waveforms**

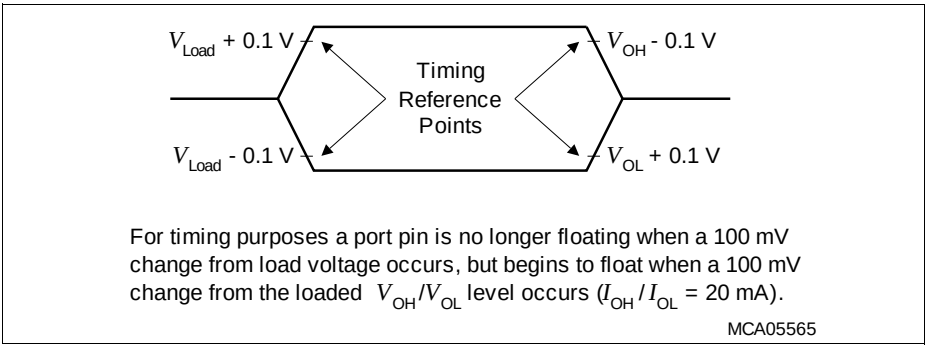


**Figure 18 Floating Waveforms**

**Table 28 Standard Pad Parameters for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum output driver current (absolute value)[1)] | $I_{Omax}$ CC | – | – | 2.5 | mA | Driver_Strength = Medium |
| | | – | – | 10 | mA | Driver_Strength = Strong |
| | | – | – | 0.5 | mA | Driver_Strength = Weak |
| Nominal output driver current (absolute value) | $I_{Onom}$ CC | – | – | 1.0 | mA | Driver_Strength = Medium |
| | | – | – | 2.5 | mA | Driver_Strength = Strong |
| | | – | – | 0.1 | mA | Driver_Strength = Weak |

duration of an asynchronous READY signal for safe synchronization is one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{RD}$ or $\overline{WR}$).

If the next bus cycle is controlled by READY, an active READY signal must be disabled before the first valid sample point in the next bus cycle. This sample point depends on the programmed phases of the next cycle.

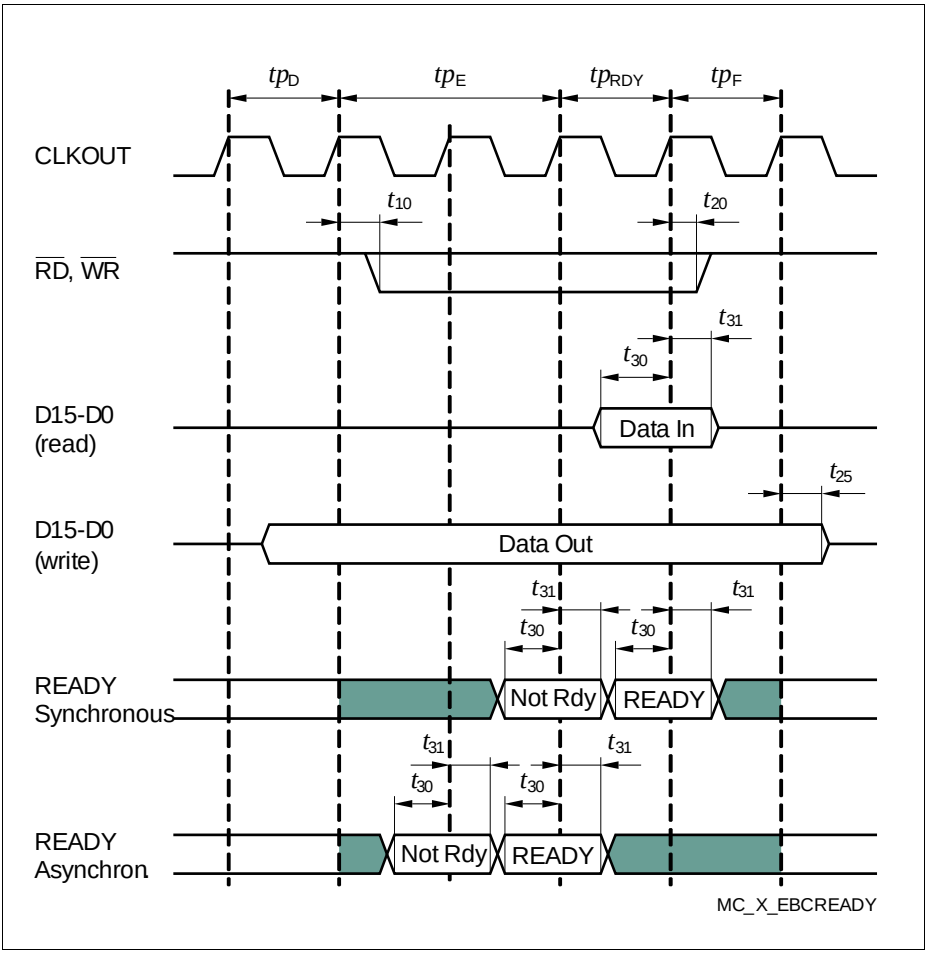


**Figure 25 READY Timing**

**Table 40 JTAG Interface Timing for Lower Voltage Range** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TDI/TMS hold after TCK rising edge | $t_7$ SR | 6 | – | – | ns | |
| TDO valid from TCK falling edge (propagation delay)[1] | $t_8$ CC | – | 32 | 36 | ns | |
| TDO high impedance to valid output from TCK falling edge[2][1] | $t_9$ CC | – | 32 | 36 | ns | |
| TDO valid output to high impedance from TCK falling edge[1] | $t_{10}$ CC | – | 32 | 36 | ns | |
| TDO hold after TCK falling edge[1] | $t_{18}$ CC | 5 | – | – | ns | |

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

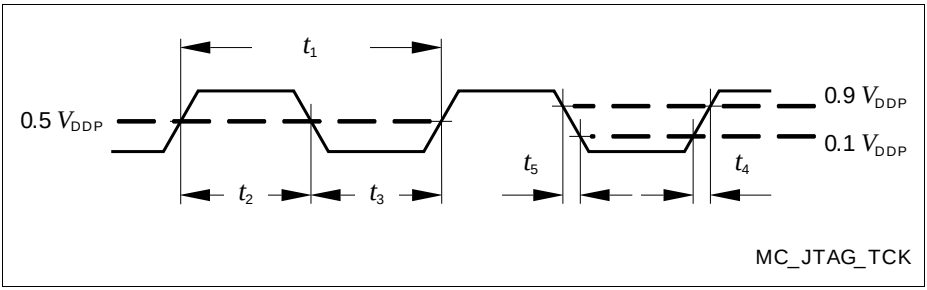


**Figure 30 Test Clock Timing (TCK)**

## 5.3 Quality Declarations

The operation lifetime of the XE169xH depends on the operating temperature. The life time decreases with increasing temperature as shown in **Table 43**.

**Table 42 Quality Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operation lifetime | $t_{OP}$ CC | – | – | 20 | a | See **Table 43** |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ SR | – | – | 2 000 | V | EIA/JESD22-A114-B |
| Moisture sensitivity level | MSL CC | – | – | 3 | – | JEDEC J-STD-020C |

**Table 43 Lifetime dependency from Temperature**

| Operating Time | Operating Temperature |
|---|---|
| 20 a | $T_J \leq 110°C$ |
| 95 500 h | $T_J = 120°C$ |
| 68 500 h | $T_J = 125°C$ |
| 49 500 h | $T_J = 130°C$ |
| 26 400 h | $T_J = 140°C$ |
| 14 500 h | $T_J = 150°C$ |