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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	925MHz
Primary Attributes	FPGA - 350K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA, FC (31x31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5asxbb3d4f31c4n">https://www.e-xfl.com/product-detail/intel/5asxbb3d4f31c4n</a>

Feature	Description
Configuration	<ul style="list-style-type: none"><li>• Tamper protection-comprehensive design protection to protect your valuable IP investments</li><li>• Enhanced advanced encryption standard (AES) design security features</li><li>• CvP</li><li>• Partial and dynamic reconfiguration of the FPGA</li><li>• Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8, x16, and x32 ( Arria V GZ) configuration options</li><li>• Remote system upgrade</li></ul>

## Arria V Device Variants and Packages

Table 3: Device Variants for the Arria V Device Family

Variant	Description
Arria V GX	FPGA with integrated 6.5536 Gbps transceivers that provides bandwidth, cost, and power levels that are optimized for high-volume data and signal-processing applications
Arria V GT	FPGA with integrated 10.3125 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for cost-sensitive data and signal processing applications
Arria V GZ	FPGA with integrated 12.5 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for high-performance and cost-sensitive data and signal processing applications
Arria V SX	SoC with integrated ARM-based HPS and 6.5536 Gbps transceivers
Arria V ST	SoC with integrated ARM-based HPS and 10.3125 Gbps transceivers

### Arria V GX

This section provides the available options, maximum resource counts, and package plan for the Arria V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

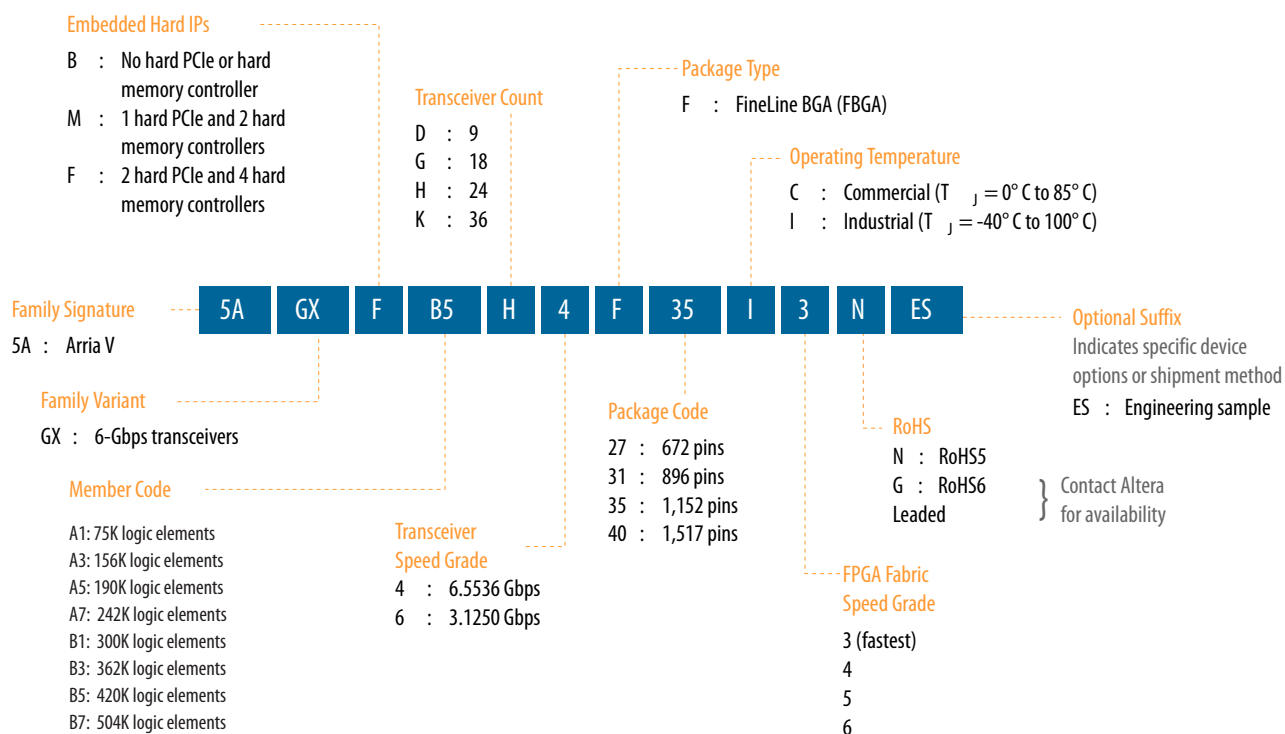
#### Related Information

##### [Altera Product Selector](#)

Provides the latest information about Altera products.

## Available Options

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



## Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
Logic Elements (LE) (K)		75	156	190	242	300	362	420	504
ALM		28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240
Register		113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960
Mem ory (Kb)	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
	MLAB	463	961	1,173	1,448	1,852	2,098	2,532	2,906
Variable-precision DSP Block		240	396	600	800	920	1,045	1,092	1,156
18 x 18 Multiplier		480	792	1,200	1,600	1,840	2,090	2,184	2,312
PLL		10	10	12	12	12	12	16	16

and eighteen 10-Gbps, twelve 6-Gbps and sixteen 10-Gbps, fifteen 6-Gbps and fourteen 10-Gbps, or up to thirty-six 6-Gbps with no 10-Gbps channels.

## Arria V GZ

This section provides the available options, maximum resource counts, and package plan for the Arria V GZ devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

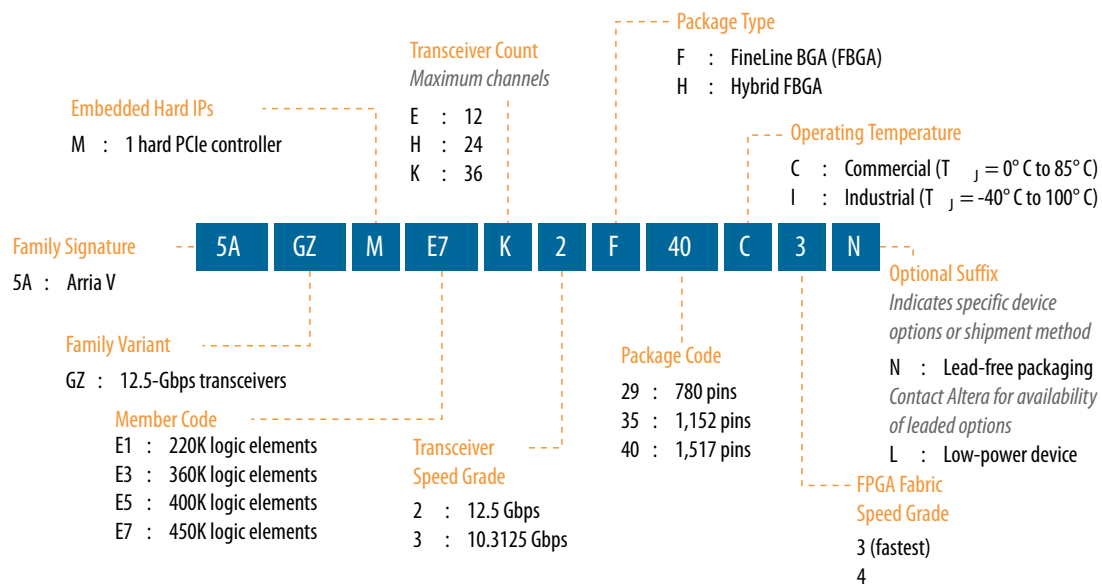
### Related Information

#### Altera Product Selector

Provides the latest information about Altera products.

## Available Options

Figure 3: Sample Ordering Code and Available Options for Arria V GZ Devices



## Maximum Resources

Table 8: Maximum Resource Counts for Arria V GZ Devices

Resource	Member Code			
	E1	E3	E5	E7
Logic Elements (LE) (K)	220	360	400	450
ALM	83,020	135,840	150,960	169,800
Register	332,080	543,360	603,840	679,200

Resource		Member Code			
		E1	E3	E5	E7
Memory (Kb)	M20K	11,700	19,140	28,800	34,000
	MLAB	2,594	4,245	4,718	5,306
Variable-precision DSP Block		800	1,044	1,092	1,139
18 x 18 Multiplier		1,600	2,088	2,184	2,278
PLL		20	20	24	24
12.5 Gbps Transceiver		24	24	36	36
GPIO <sup>(7)</sup>		414	414	674	674
LVDS	Transmitter	99	99	166	166
	Receiver	108	108	168	168
PCIe Hard IP Block		1	1	1	1

**Related Information**

[High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)

Provides the number of LVDS channels in each device package.

**Package Plan****Table 9: Package Plan for Arria V GZ Devices**

Member Code	H780 (33 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
E1	342	12	414	24	—	—
E3	342	12	414	24	—	—
E5	—	—	534	24	674	36
E7	—	—	534	24	674	36

**Arria V SX**

This section provides the available options, maximum resource counts, and package plan for the Arria V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

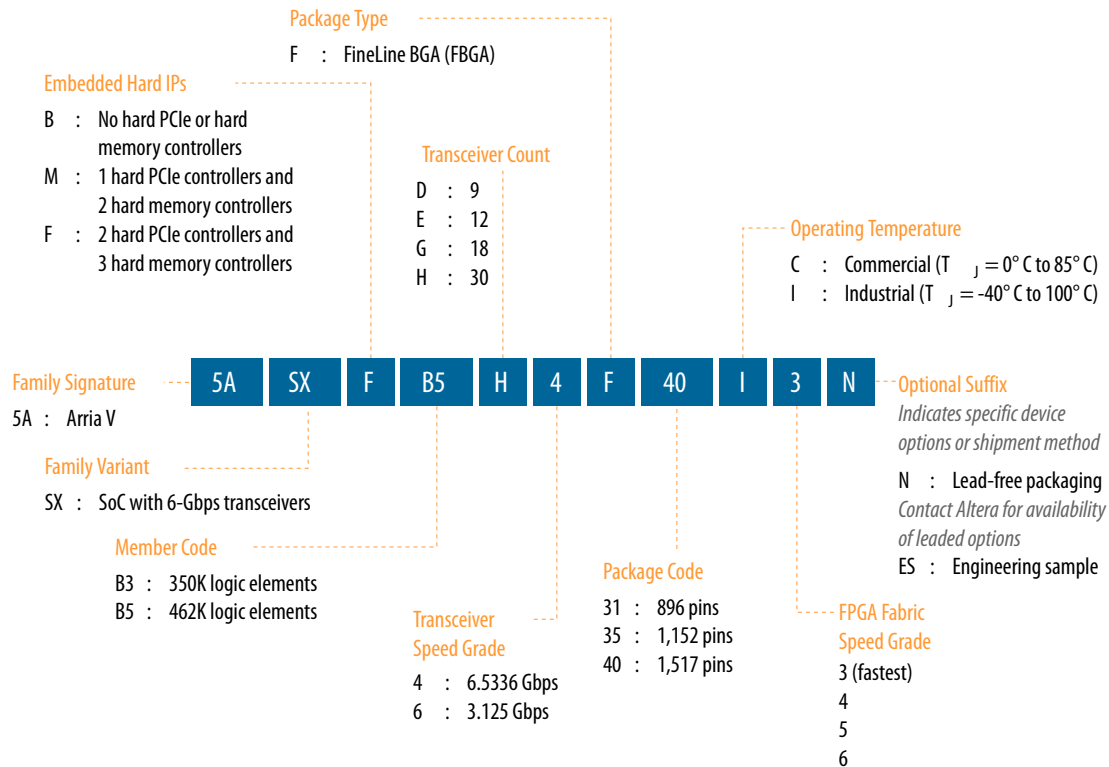
<sup>(7)</sup> The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

**Related Information****Altera Product Selector**

Provides the latest information about Altera products.

**Available Options****Figure 4: Sample Ordering Code and Available Options for Arria V SX Devices**

The –3 FPGA fabric speed grade is available only for industrial temperature devices.

**Maximum Resources****Table 10: Maximum Resource Counts for Arria V SX Devices**

Resource		Member Code	
		B3	B5
Logic Elements (LE) (K)		350	462
ALM		132,075	174,340
Register		528,300	697,360
Memory (Kb)	M10K	17,290	22,820
	MLAB	2,014	2,658
Variable-precision DSP Block		809	1,090
18 x 18 Multiplier		1,618	2,180

Resource		Member Code	
		B3	B5
FPGA PLL		14	14
HPS PLL		3	3
6 Gbps Transceiver		30	30
FPGA GPIO <sup>(8)</sup>		540	540
HPS I/O		208	208
LVDS	Transmitter	120	120
	Receiver	136	136
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		3	3
HPS Hard Memory Controller		1	1
ARM Cortex-A9 MPCore Processor		Dual-core	Dual-core

**Related Information**

[High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)

Provides the number of LVDS channels in each device package.

**Package Plan****Table 11: Package Plan for Arria V SX Devices**

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	F896 (31 mm)			F1152 (35 mm)			F1517 (40 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
B3	250	208	12	385	208	18	540	208	30
B5	250	208	12	385	208	18	540	208	30

**Arria V ST**

This section provides the available options, maximum resource counts, and package plan for the Arria V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

<sup>(8)</sup> The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

**Related Information**

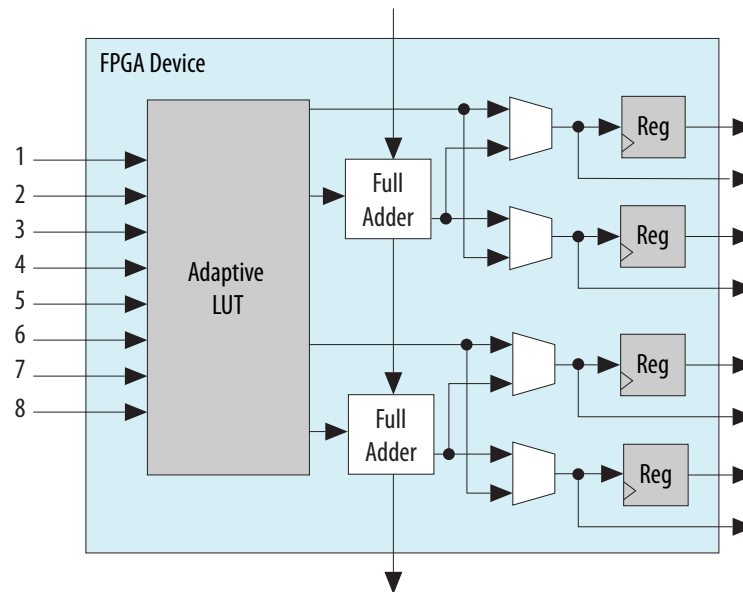
- **Managing Device I/O Pins chapter, Quartus Prime Handbook**  
Provides more information about vertical I/O migrations.
- **Power Management in Arria V Devices**  
Describes the power-up sequence required for Arria V GX and GT devices.

## Adaptive Logic Module

Arria V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

**Figure 7: ALM for Arria V Devices**



You can configure up to 50% of the ALMs in the Arria V devices as distributed memory using MLABs.

**Related Information**

**Embedded Memory Capacity in Arria V Devices** on page 20

Lists the embedded memory capacity for each device.



## Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- Double accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus Prime design software

**Table 14: Variable-Precision DSP Block Configurations for Arria V Devices**

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters	Two 18 x 18 with accumulate	1
Single-precision floating-point implementations	One 27 x 27	1
Very high precision fixed point implementations	One 36 x 36	2

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. Using two DSP block resources, you can also configure a 36 x 36 multiplier for high-precision applications. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

**Table 15: Number of Multipliers in Arria V Devices**

The table lists the variable-precision DSP resources by bit precision for each Arria V device.

Variant	Member Code	Variable-precision DSP Block	Independent Input and Output Multiplications Operator				18 x 18 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier	36 x 36 Multiplier		
Arria V GX	A1	240	720	480	240	—	240	240
	A3	396	1,188	792	396	—	396	396
	A5	600	1,800	1,200	600	—	600	600
	A7	800	2,400	1,600	800	—	800	800
	B1	920	2,760	1,840	920	—	920	920
	B3	1,045	3,135	2,090	1,045	—	1,045	1,045
	B5	1,092	3,276	2,184	1,092	—	1,092	1,092
	B7	1,156	3,468	2,312	1,156	—	1,156	1,156
Arria V GT	C3	396	1,188	792	396	—	396	396
	C7	800	2,400	1,600	800	—	800	800
	D3	1,045	3,135	2,090	1,045	—	1,045	1,045
	D7	1,156	3,468	2,312	1,156	—	1,156	1,156
Arria V GZ	E1	800	2,400	1,600	800	400	800	800
	E3	1,044	3,132	2,088	1,044	522	1,044	1,044
	E5	1,092	3,276	2,184	1,092	546	1,092	1,092
	E7	1,139	3,417	2,278	1,139	569	1,139	1,139
Arria V SX	B3	809	2,427	1,618	809	—	809	809
	B5	1,090	3,270	2,180	1,090	—	1,090	1,090
Arria V ST	D3	809	2,427	1,618	809	—	809	809
	D5	1,090	3,270	2,180	1,090	—	1,090	1,090

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

## Types of Embedded Memory

The Arria V devices contain two types of memory blocks:

- 20 Kb M20K or 10 Kb M10K blocks—blocks of dedicated memory resources. The M20K and M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Arria V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB. You can also configure these ALMs, in Arria V GZ devices, as ten 64 x 1 blocks, giving you one 64 x 10 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Arria V Devices

Table 16: Embedded Memory Capacity and Distribution in Arria V Devices

Variant	Member Code	M20K		M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Arria V GX	A1	—	—	800	8,000	741	463	8,463
	A3	—	—	1,051	10,510	1538	961	11,471
	A5	—	—	1,180	11,800	1877	1,173	12,973
	A7	—	—	1,366	13,660	2317	1,448	15,108
	B1	—	—	1,510	15,100	2964	1,852	16,952
	B3	—	—	1,726	17,260	3357	2,098	19,358
	B5	—	—	2,054	20,540	4052	2,532	23,072
	B7	—	—	2,414	24,140	4650	2,906	27,046
Arria V GT	C3	—	—	1,051	10,510	1538	961	11,471
	C7	—	—	1,366	13,660	2317	1,448	15,108
	D3	—	—	1,726	17,260	3357	2,098	19,358
	D7	—	—	2,414	24,140	4650	2,906	27,046
Arria V GZ	E1	585	11,700	—	—	4,151	2,594	14,294
	E3	957	19,140	—	—	6,792	4,245	23,385
	E5	1,440	28,800	—	—	7,548	4,718	33,518
	E7	1,700	34,000	—	—	8,490	5,306	39,306
Arria V SX	B3	—	—	1,729	17,290	3223	2,014	19,304
	B5	—	—	2,282	22,820	4253	2,658	25,478

## PLL Features

The PLLs in the Arria V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Counter reconfiguration
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- Dynamic phase shift
- Zero delay buffers

## Fractional PLL

In addition to integer PLLs, the Arria V devices use a fractional PLL architecture. The devices have up to 16 PLLs, each with 18 output counters. One fractional PLL can use up to 18 output counters and two adjacent fractional PLLs share the 18 output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

## FPGA General Purpose I/O

Arria V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage ( $V_{OD}$ ) and programmable pre-emphasis
- On-chip parallel termination ( $R_T$  OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Unused voltage reference ( $V_{REF}$ ) pins that can be configured as user I/Os (Arria V GX, GT, SX, and ST only)
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

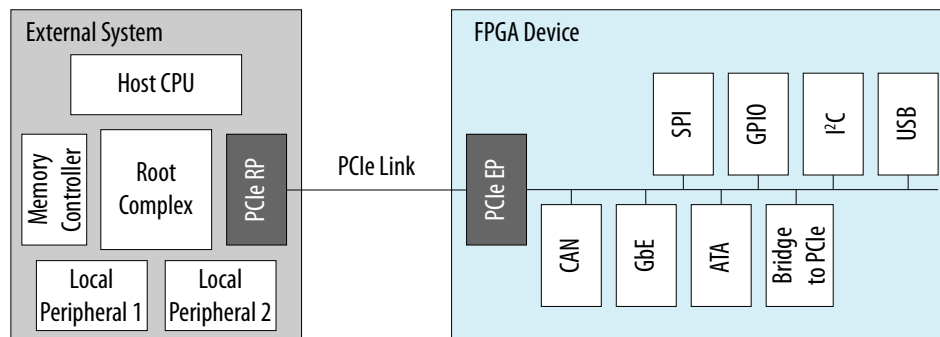
## PCIe Gen1, Gen2, and Gen 3 Hard IP

Arria V devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen3, Gen 2, and Gen 1 end point and root port for up to x8 lane configuration.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

**Figure 8: PCIe Multifunction for Arria V Devices**



The Arria V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Arria V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Arria V device provides improved end-to-end datapath protection using ECC.

## External Memory Interface

This section provides an overview of the external memory interface in Arria V devices.

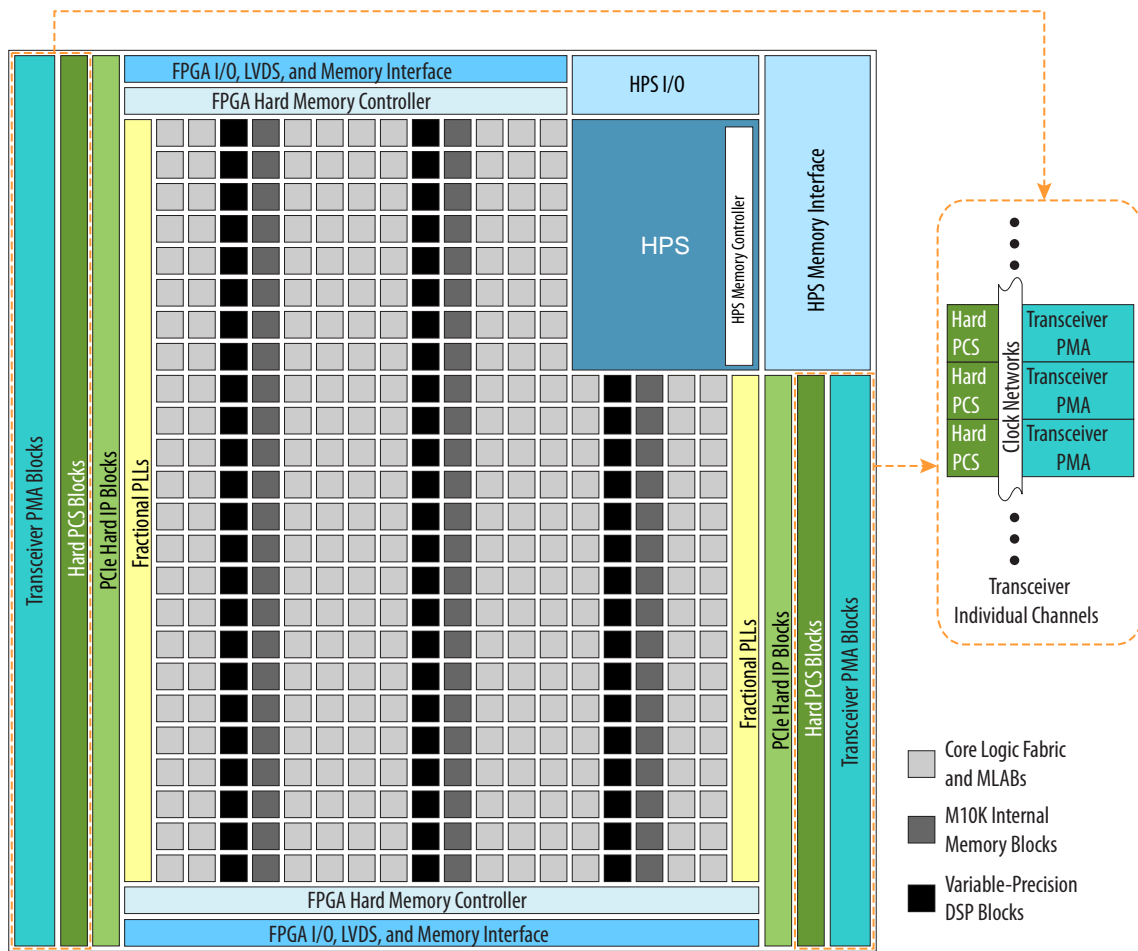
### Hard and Soft Memory Controllers

Arria V GX,GT, SX, and ST devices support up to four hard memory controllers for DDR3 and DDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Arria V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Arria V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices, QDR II+, QDR II, and DDR II+ SRAM devices, and RLDRAM II devices for maximum flexibility.

**Note:** DDR3 SDRAM leveling is supported only in Arria V GZ devices.

Figure 11: Device Chip Overview for Arria V SX and ST Devices



## PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 20: PMA Features of the Transceivers in Arria V Devices

Features	Capability
Backplane support	<ul style="list-style-type: none"> <li>Arria V GX, GT, SX, and ST devices—Driving capability at 6.5536 Gbps with up to 25 dB channel loss</li> <li>Arria V GZ devices—Driving capability at 12.5 Gbps with up to 16 dB channel loss</li> </ul>
Chip-to-chip support	<ul style="list-style-type: none"> <li>Arria V GX, GT, SX, and ST devices—Up to 10.3125 Gbps</li> <li>Arria V GZ devices—Up to 12.5 Gbps</li> </ul>

Features	Capability
PLL-based clock recovery	Superior jitter tolerance
Programmable serializer and deserializer (SERDES)	Flexible SERDES width
Equalization and pre-emphasis	<ul style="list-style-type: none"> <li>Arria V GX, GT, SX, and ST devices—Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization</li> <li>Arria V GZ devices—4-tap pre-emphasis and de-emphasis</li> </ul>
Ring oscillator transmit PLLs	611 Mbps to 10.3125 Gbps
LC oscillator ATX transmit PLLs (Arria V GZ devices only)	600 Mbps to 12.5 Gbps
Input reference clock range	27 MHz to 710 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

## PCS Features

The Arria V core logic connects to the PCS through an 8, 10, 16, 20, 32, 40, 64, 66, or 67 bit interface, depending on the transceiver data rate and protocol. Arria V devices contain PCS hard IP to support PCIe Gen1, Gen2, and Gen3, GbE, Serial RapidIO (SRIO), GPON, and CPRI.

All other standard and proprietary protocols within the following speed ranges are also supported:

- 611 Mbps to 6.5536 Gbps—supported through the custom double-width mode (up to 6.5536 Gbps) and custom single-width mode (up to 3.75 Gbps) of the transceiver PCS hard IP.
- 6.5536 Gbps to 10.3125 Gbps—supported through dedicated 80 or 64 bit interface that bypass the PCS hard IP and connects the PMA directly to the core logic. In Arria V GZ, this is supported in the transceiver PCS hard IP.

**Table 21: Transceiver PCS Features for Arria V GX, GT, ST, and SX Devices**

PCS Support <sup>(13)</sup>	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Custom single- and double-width modes	0.611 to ~6.5536	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Phase compensation FIFO</li> </ul>
SRIO	1.25 to 6.25		
Serial ATA	1.5, 3.0, 6.0		

<sup>(13)</sup> Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

PCS Support <sup>(13)</sup>	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
PCIe Gen1 (x1, x2, x4, x8)	2.5 and 5.0	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>PIPE 2.0 interface to the core logic</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Phase compensation FIFO</li> <li>Rate match FIFO</li> <li>PIPE 2.0 interface to the core logic</li> </ul>
PCIe Gen2 <sup>(14)</sup> (x1, x2, x4)			
GbE	1.25	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Phase compensation FIFO</li> <li>Rate match FIFO</li> </ul>
XAUI <sup>(15)</sup>	3.125	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>XAUI state machine for bonding four channels</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Phase compensation FIFO</li> <li>XAUI state machine for realigning four channels</li> <li>Deskew FIFO circuitry</li> </ul>
SDI	0.27 <sup>(16)</sup> , 1.485, 2.97	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> </ul>	<ul style="list-style-type: none"> <li>Byte deserializer</li> <li>Phase compensation FIFO</li> </ul>
GPON <sup>(17)</sup>	1.25 and 2.5		
CPRI <sup>(18)</sup>	0.6144 to 6.144	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>TX deterministic latency</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Phase compensation FIFO</li> <li>RX deterministic latency</li> </ul>

<sup>(13)</sup> Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

<sup>(14)</sup> PCIe Gen2 is supported only through the PCIe hard IP.

<sup>(15)</sup> XAUI is supported through the soft PCS.

<sup>(16)</sup> The 0.27 Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

<sup>(17)</sup> The GPON standard does not support burst mode.

<sup>(18)</sup> CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through the soft PCS.



Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
40GBASE-R Ethernet	4 x 10.3125	<ul style="list-style-type: none"> <li>TX FIFO</li> <li>64B/66B encoder</li> <li>Scrambler</li> <li>Alignment marker insertion</li> <li>Gearbox</li> <li>Block stripper</li> </ul>	<ul style="list-style-type: none"> <li>RX FIFO</li> <li>64B/66B decoder</li> <li>Descrambler</li> <li>Lane reorder</li> <li>Deskew</li> <li>Alignment marker lock</li> <li>Block synchronization</li> <li>Gear box</li> <li>Destripper</li> </ul>
100GBASE-R Ethernet	10 x 10.3125		
40G and 100G OTN	(4 +1) x 11.3	<ul style="list-style-type: none"> <li>TX FIFO</li> <li>Channel bonding</li> <li>Byte serializer</li> </ul>	<ul style="list-style-type: none"> <li>RX FIFO</li> <li>Lane deskew</li> <li>Byte deserializer</li> </ul>
	(10 +1) x 11.3		
GbE	1.25	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>Bit-slip</li> <li>Channel bonding</li> <li>GbE state machine</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>Deskew FIFO</li> <li>Rate match FIFO</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Byte ordering</li> <li>GbE state machine</li> </ul>
XAUI	3.125 to 4.25	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>Bit-slip</li> <li>Channel bonding</li> <li>XAUI state machine for bonding four channels</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>Deskew FIFO</li> <li>Rate match FIFO</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Byte ordering</li> <li>XAUI state machine for realigning four channels</li> </ul>
SRIO	1.25 to 6.25	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>Bit-slip</li> <li>Channel bonding</li> <li>SRIO V2.1-compliant x2 and x4 channel bonding</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>Deskew FIFO</li> <li>Rate match FIFO</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Byte ordering</li> <li>SRIO V2.1-compliant x2 and x4 deskew state machine</li> </ul>

## SoC with HPS

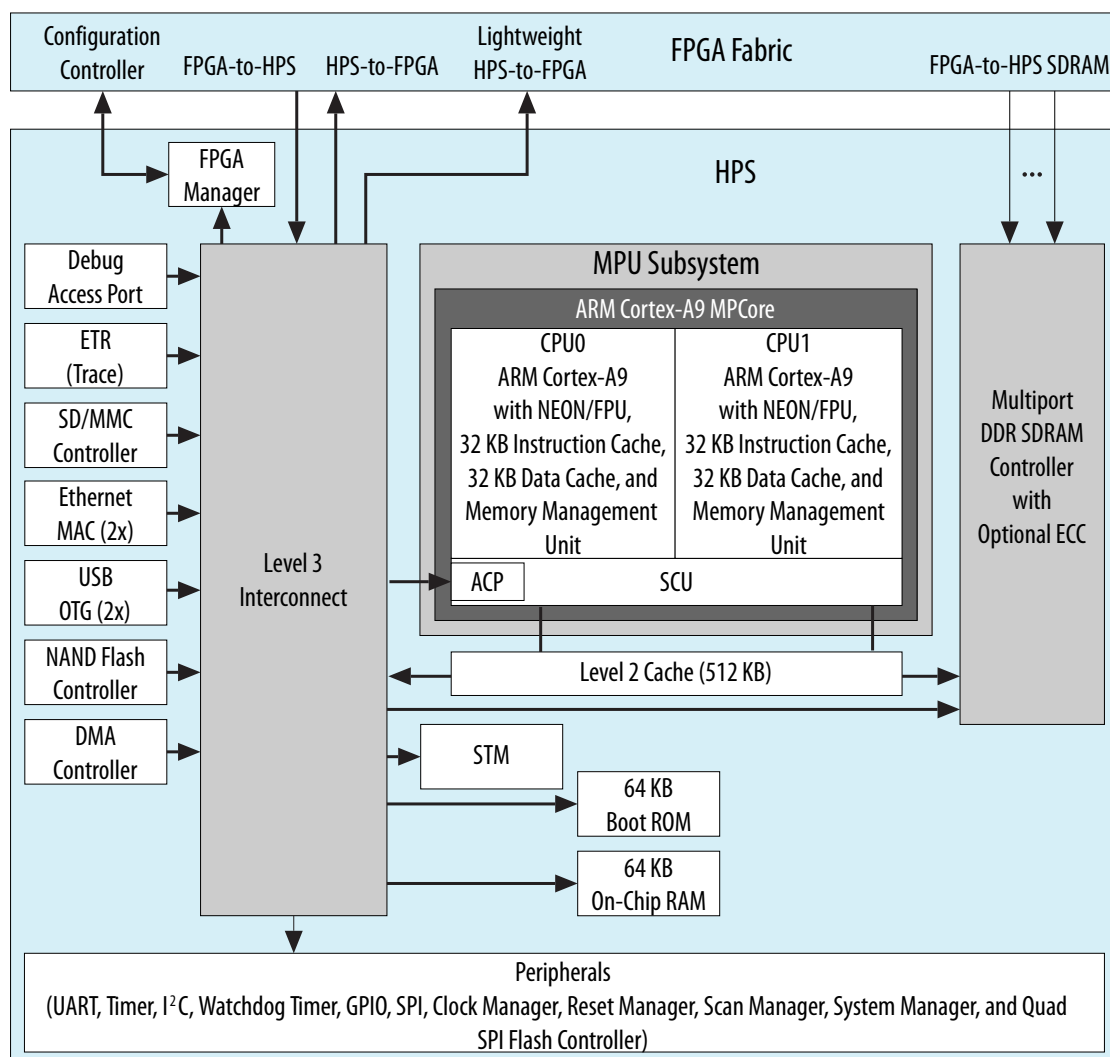
Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

## HPS Features

The HPS consists of a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

**Figure 12: HPS with Dual-Core ARM Cortex-A9 MPCore Processor**



Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration <sup>(20)</sup>	Remote System Update
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes <sup>(21)</sup>	
	32 bits <sup>(22)</sup>	100	—	Yes	Yes	—	
CvP (PCIe)	x1, x2, x4, and x8 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—
Configuration via HPS	16 bits	125	—	Yes	Yes	Yes <sup>(21)</sup>	Parallel flash loader
	32 bits	100	—	Yes	Yes	—	

Instead of using an external flash or ROM, you can configure the Arria V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Arria V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

**Note:** Although Arria V GZ devices support PCIe Gen3, you can use only PCIe Gen1 and PCIe Gen2 for CvP configuration scheme.

#### Related Information

#### [Configuration via Protocol \(CvP\) Implementation in Altera FPGAs User Guide](#)

Provides more information about CvP.

## Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Arria V devices consume less power than previous generation Arria V FPGAs:

- Total device core power consumption—less by up to 50%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Arria V devices contain several hard IP blocks, including PCIe Gen1, Gen2, and Gen3, GbE, SRIO, GPON, and CPRI protocols, that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

<sup>(20)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

<sup>(21)</sup> Supported at a maximum clock rate of 62.5 MHz.

<sup>(22)</sup> Arria V GZ only

## Document Revision History

Date	Version	Changes
December 2015	2015.12.21	<ul style="list-style-type: none"> <li>Updated RoHS and optional suffix information in sample ordering code and available options diagrams for Arria V GX and GT devices.</li> <li>Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.</li> </ul>
January 2015	2015.01.23	<ul style="list-style-type: none"> <li>Updated package dimension for Arria V GZ H780 package from 29 mm to 33 mm.</li> <li>Updated dual-core ARM Cortex-A9 MPCore processor maximum frequency from 800 MHz to 1.05 GHz.</li> </ul>
December 2013	2013.12.26	<ul style="list-style-type: none"> <li>10-Gbps Ethernet (10GbE) PCS and Interlaken PCS are for Arria V GZ only.</li> <li>Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables.</li> <li>Added link to <a href="#">Altera Product Selector</a> for each device variant.</li> <li>Added leaded package options.</li> <li>Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table.</li> <li>Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F896 package from 170 to 250.</li> <li>Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1152 package from 350 to 385.</li> <li>Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1517 package from 528 to 540.</li> <li>Corrected LVDS Transmitter for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 devices from 121 to 120.</li> <li>Added links to Altera's <a href="#">External Memory Spec Estimator</a> tool to the topics listing the external memory interface performance.</li> <li>Added x2 for PCIe Gen3, Gen 2, and Gen 1.</li> </ul>
August 2013	2013.08.19	<ul style="list-style-type: none"> <li>Removed the note about the PCIe hard IP on the right side of the device in the F896 package of the Arria V GX variant. These devices do not have PCIe hard IP on the right side.</li> <li>Added transceiver speed grade 6 to the available options of the Arria V SX variant.</li> <li>Corrected the maximum LVDS transmitter channel counts for the Arria V GX A1 and A3 devices from 68 to 67.</li> <li>Corrected the maximum FPGA GPIO count for Arria V ST D5 devices from 540 to 528.</li> </ul>

Date	Version	Changes
July 2012	2.1	<ul style="list-style-type: none"> <li>Added –I3 speed grade to Figure 1 for Arria V GX devices.</li> <li>Updated the 6-Gbps transceiver speed from 6.553 Gbps to 6.5536 Gbps in Figure 3 and Figure 1.</li> </ul>
June 2012	2.0	<ul style="list-style-type: none"> <li>Restructured the document.</li> <li>Added the “Embedded Memory Capacity” and “Embedded Memory Configurations” sections.</li> <li>Added Table 1, Table 3, Table 12, Table 15, and Table 16.</li> <li>Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 13, Table 14, and Table 19.</li> <li>Updated Figure 1, Figure 2, Figure 3, Figure 4, and Figure 8.</li> <li>Updated the “FPGA Configuration and Processor Booting” and “Hardware and Software Development” sections.</li> <li>Text edits throughout the document.</li> </ul>
February 2012	1.3	<ul style="list-style-type: none"> <li>Updated Table 1–7 and Table 1–8.</li> <li>Updated Figure 1–9 and Figure 1–10.</li> <li>Minor text edits.</li> </ul>
December 2011	1.2	Minor text edits.
November 2011	1.1	<ul style="list-style-type: none"> <li>Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–6, Table 1–7, Table 1–9, and Table 1–10.</li> <li>Added “SoC FPGA with HPS” section.</li> <li>Updated “Clock Networks and PLL Clock Sources” and “Ordering Information” sections.</li> <li>Updated Figure 1–5.</li> <li>Added Figure 1–6.</li> <li>Minor text edits.</li> </ul>
August 2011	1.0	Initial release.