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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

[Embedded - System On Chip \(SoC\)](#) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are [Embedded - System On Chip \(SoC\)](#)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

| | |
|-------------------------|---|
| Product Status | Obsolete |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 64KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 800MHz |
| Primary Attributes | FPGA - 350K Logic Elements |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 896-BBGA, FCBGA |
| Supplier Device Package | 896-FBGA, FC (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5asxbb3d4f31c5n |

| Advantage | Supporting Feature |
|--------------------|--|
| Lowest system cost | <ul style="list-style-type: none"> Requires as few as four power supplies to operate Available in thermal composite flip chip ball-grid array (BGA) packaging Includes innovative features such as Configuration via Protocol (CvP), partial reconfiguration, and design security |

Summary of Arria V Features

Table 2: Summary of Features for Arria V Devices

| Feature | Description |
|------------------------------|--|
| Technology | <ul style="list-style-type: none"> TSMC's 28-nm process technology: <ul style="list-style-type: none"> Arria V GX, GT, SX, and ST—28-nm low power (28LP) process Arria V GZ—28-nm high performance (28HP) process Lowest static power in its class (less than 1.2 W for 500K logic elements (LEs) at 85°C junction under typical conditions) 0.85 V, 1.1 V, or 1.15 V core nominal voltage |
| Packaging | <ul style="list-style-type: none"> Thermal composite flip chip BGA packaging Multiple device densities with identical package footprints for seamless migration between different device densities Leaded⁽¹⁾, lead-free (Pb-free), and RoHS-compliant options |
| High-performance FPGA fabric | <ul style="list-style-type: none"> Enhanced 8-input ALM with four registers Improved routing architecture to reduce congestion and improve compilation time |
| Internal memory blocks | <ul style="list-style-type: none"> M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) (Arria V GX, GT, SX, and ST devices only) M20K—20-Kb memory blocks with hard ECC (Arria V GZ devices only) Memory logic array block (MLAB)-640-bit distributed LUTRAM where you can use up to 50% of the ALMs as MLAB memory |

⁽¹⁾ Contact Altera for availability.

| Feature | Description | |
|---------------------------|---|--|
| Embedded Hard IP blocks | Variable-precision DSP | <ul style="list-style-type: none"> Native support for up to four signal processing precision levels: <ul style="list-style-type: none"> Three 9 x 9, two 18 x 18, or one 27 x 27 multiplier in the same variable-precision DSP block One 36 x 36 multiplier using two variable-precision DSP blocks (Arria V GZ devices only) 64-bit accumulator and cascade for systolic finite impulse responses (FIRs) Embedded internal coefficient memory Preadder/subtractor for improved efficiency |
| | Memory controller (Arria V GX, GT, SX, and ST only) | DDR3 and DDR2 |
| | Embedded transceiver I/O | <ul style="list-style-type: none"> Custom implementation: <ul style="list-style-type: none"> Arria V GX and SX devices—up to 6.5536 Gbps Arria V GT and ST devices—up to 10.3125 Gbps Arria V GZ devices—up to 12.5 Gbps PCI Express® (PCIe®) Gen2 (x1, x2, or x4) and Gen1 (x1, x2, x4, or x8) hard IP with multifunction support, endpoint, and root port PCIe Gen3 (x1, x2, x4, or x8) support (Arria V GZ only) Gbps Ethernet (GbE) and XAUI physical coding sublayer (PCS) Common Public Radio Interface (CPRI) PCS Gigabit-capable passive optical network (GPON) PCS 10-Gbps Ethernet (10GbE) PCS (Arria V GZ only) Serial RapidIO® (SRIO) PCS Interlaken PCS (Arria V GZ only) |
| Clock networks | <ul style="list-style-type: none"> Up to 650 MHz global clock network Global, quadrant, and peripheral clock networks Clock networks that are not used can be powered down to reduce dynamic power | |
| Phase-locked loops (PLLs) | <ul style="list-style-type: none"> High-resolution fractional PLLs Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) Integer mode and fractional mode LC oscillator ATX transmitter PLLs (Arria V GZ only) | |



| Feature | Description |
|---------------|--|
| Configuration | <ul style="list-style-type: none">• Tamper protection-comprehensive design protection to protect your valuable IP investments• Enhanced advanced encryption standard (AES) design security features• CvP• Partial and dynamic reconfiguration of the FPGA• Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8, x16, and x32 (Arria V GZ) configuration options• Remote system upgrade |

Arria V Device Variants and Packages

Table 3: Device Variants for the Arria V Device Family

| Variant | Description |
|------------|--|
| Arria V GX | FPGA with integrated 6.5536 Gbps transceivers that provides bandwidth, cost, and power levels that are optimized for high-volume data and signal-processing applications |
| Arria V GT | FPGA with integrated 10.3125 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for cost-sensitive data and signal processing applications |
| Arria V GZ | FPGA with integrated 12.5 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for high-performance and cost-sensitive data and signal processing applications |
| Arria V SX | SoC with integrated ARM-based HPS and 6.5536 Gbps transceivers |
| Arria V ST | SoC with integrated ARM-based HPS and 10.3125 Gbps transceivers |

Arria V GX

This section provides the available options, maximum resource counts, and package plan for the Arria V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

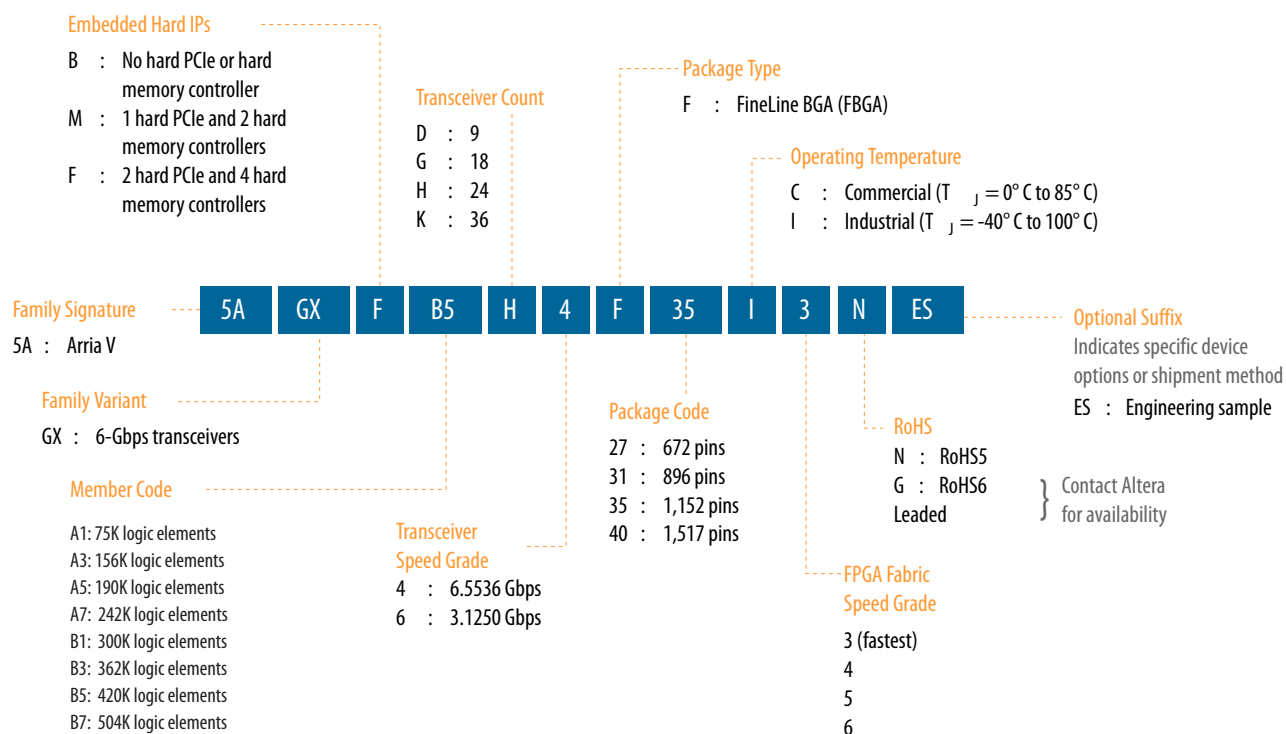
Related Information

[Altera Product Selector](#)

Provides the latest information about Altera products.

Available Options

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

| Resource | | Member Code | | | | | | | |
|------------------------------|------|-------------|---------|---------|---------|---------|---------|---------|---------|
| | | A1 | A3 | A5 | A7 | B1 | B3 | B5 | B7 |
| Logic Elements (LE) (K) | | 75 | 156 | 190 | 242 | 300 | 362 | 420 | 504 |
| ALM | | 28,302 | 58,900 | 71,698 | 91,680 | 113,208 | 136,880 | 158,491 | 190,240 |
| Register | | 113,208 | 235,600 | 286,792 | 366,720 | 452,832 | 547,520 | 633,964 | 760,960 |
| Mem ory (Kb) | M10K | 8,000 | 10,510 | 11,800 | 13,660 | 15,100 | 17,260 | 20,540 | 24,140 |
| | MLAB | 463 | 961 | 1,173 | 1,448 | 1,852 | 2,098 | 2,532 | 2,906 |
| Variable-precision DSP Block | | 240 | 396 | 600 | 800 | 920 | 1,045 | 1,092 | 1,156 |
| 18 x 18 Multiplier | | 480 | 792 | 1,200 | 1,600 | 1,840 | 2,090 | 2,184 | 2,312 |
| PLL | | 10 | 10 | 12 | 12 | 12 | 12 | 16 | 16 |

| Resource | | Member Code | | | | | | | |
|------------------------|-------------|-------------|-----|-----|-----|-----|-----|-----|-----|
| | | A1 | A3 | A5 | A7 | B1 | B3 | B5 | B7 |
| 6 Gbps Transceiver | | 9 | 9 | 24 | 24 | 24 | 24 | 36 | 36 |
| GPIO ⁽³⁾ | | 416 | 416 | 544 | 544 | 704 | 704 | 704 | 704 |
| LVD S | Transmitter | 67 | 67 | 120 | 120 | 160 | 160 | 160 | 160 |
| | Receiver | 80 | 80 | 136 | 136 | 176 | 176 | 176 | 176 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 |
| Hard Memory Controller | | 2 | 2 | 4 | 4 | 4 | 4 | 4 | 4 |

Related Information

[High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)

Provides the number of LVDS channels in each device package.

Package Plan**Table 5: Package Plan for Arria V GX Devices**

| Member Code | F672 (27 mm) | | F896 (31 mm) | | F1152 (35 mm) | | F1517 (40 mm) | |
|-------------|-----------------|------|-----------------|------|------------------|------|------------------|------|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| A1 | 336 | 9 | 416 | 9 | — | — | — | — |
| A3 | 336 | 9 | 416 | 9 | — | — | — | — |
| A5 | 336 | 9 | 384 | 18 | 544 | 24 | — | — |
| A7 | 336 | 9 | 384 | 18 | 544 | 24 | — | — |
| B1 | — | — | 384 | 18 | 544 | 24 | 704 | 24 |
| B3 | — | — | 384 | 18 | 544 | 24 | 704 | 24 |
| B5 | — | — | — | — | 544 | 24 | 704 | 36 |
| B7 | — | — | — | — | 544 | 24 | 704 | 36 |

Arria V GT

This section provides the available options, maximum resource counts, and package plan for the Arria V GT devices.

⁽³⁾ The number of GPIOs does not include transceiver I/Os. In the Quartus® Prime software, the number of user I/Os includes transceiver I/Os.

and eighteen 10-Gbps, twelve 6-Gbps and sixteen 10-Gbps, fifteen 6-Gbps and fourteen 10-Gbps, or up to thirty-six 6-Gbps with no 10-Gbps channels.

Arria V GZ

This section provides the available options, maximum resource counts, and package plan for the Arria V GZ devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

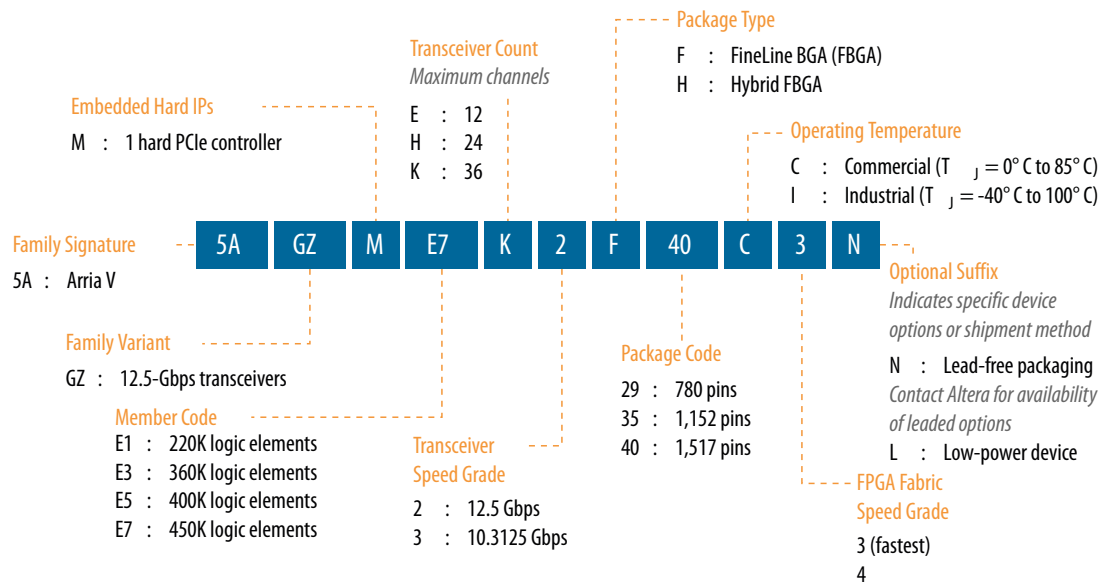
Related Information

Altera Product Selector

Provides the latest information about Altera products.

Available Options

Figure 3: Sample Ordering Code and Available Options for Arria V GZ Devices



Maximum Resources

Table 8: Maximum Resource Counts for Arria V GZ Devices

| Resource | Member Code | | | |
|-------------------------|-------------|---------|---------|---------|
| | E1 | E3 | E5 | E7 |
| Logic Elements (LE) (K) | 220 | 360 | 400 | 450 |
| ALM | 83,020 | 135,840 | 150,960 | 169,800 |
| Register | 332,080 | 543,360 | 603,840 | 679,200 |

| Resource | | Member Code | | | |
|------------------------------|-------------|-------------|--------|--------|--------|
| | | E1 | E3 | E5 | E7 |
| Memory (Kb) | M20K | 11,700 | 19,140 | 28,800 | 34,000 |
| | MLAB | 2,594 | 4,245 | 4,718 | 5,306 |
| Variable-precision DSP Block | | 800 | 1,044 | 1,092 | 1,139 |
| 18 x 18 Multiplier | | 1,600 | 2,088 | 2,184 | 2,278 |
| PLL | | 20 | 20 | 24 | 24 |
| 12.5 Gbps Transceiver | | 24 | 24 | 36 | 36 |
| GPIO ⁽⁷⁾ | | 414 | 414 | 674 | 674 |
| LVDS | Transmitter | 99 | 99 | 166 | 166 |
| | Receiver | 108 | 108 | 168 | 168 |
| PCIe Hard IP Block | | 1 | 1 | 1 | 1 |

Related Information

[High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)

Provides the number of LVDS channels in each device package.

Package Plan**Table 9: Package Plan for Arria V GZ Devices**

| Member Code | H780 (33 mm) | | F1152 (35 mm) | | F1517 (40 mm) | |
|-------------|-----------------|------|------------------|------|------------------|------|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| E1 | 342 | 12 | 414 | 24 | — | — |
| E3 | 342 | 12 | 414 | 24 | — | — |
| E5 | — | — | 534 | 24 | 674 | 36 |
| E7 | — | — | 534 | 24 | 674 | 36 |

Arria V SX

This section provides the available options, maximum resource counts, and package plan for the Arria V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

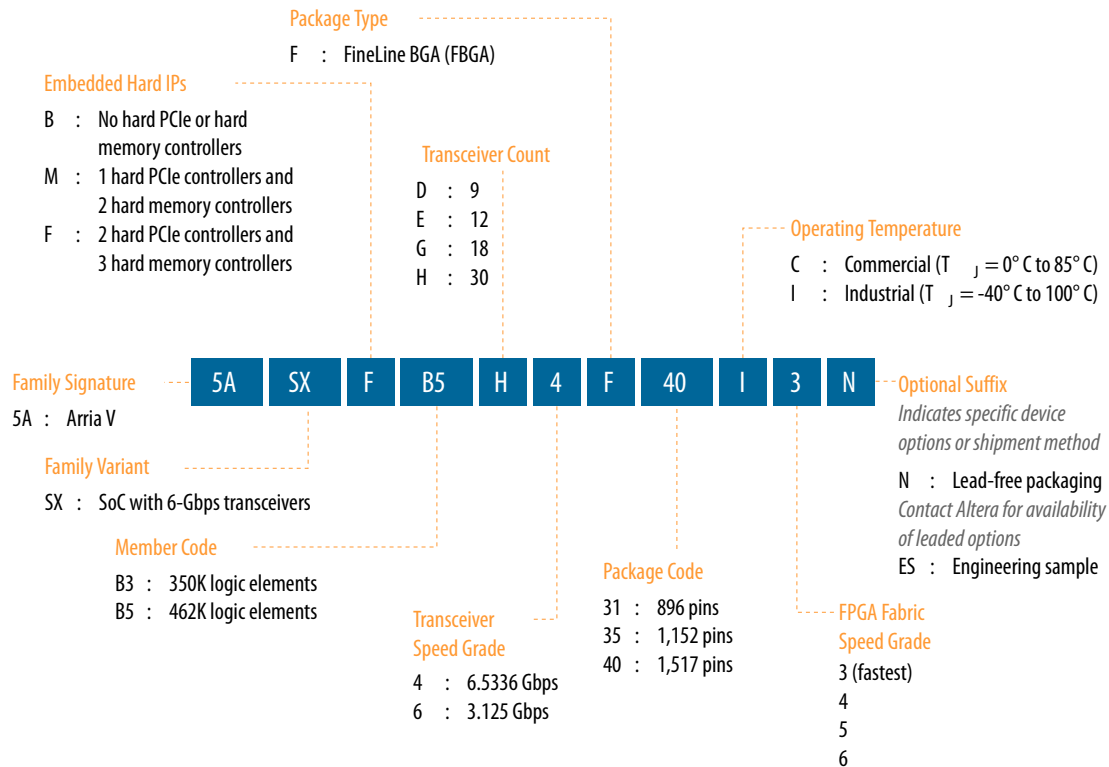
⁽⁷⁾ The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Related Information**Altera Product Selector**

Provides the latest information about Altera products.

Available Options**Figure 4: Sample Ordering Code and Available Options for Arria V SX Devices**

The –3 FPGA fabric speed grade is available only for industrial temperature devices.

**Maximum Resources****Table 10: Maximum Resource Counts for Arria V SX Devices**

| Resource | | Member Code | |
|------------------------------|------|-------------|---------|
| | | B3 | B5 |
| Logic Elements (LE) (K) | | 350 | 462 |
| ALM | | 132,075 | 174,340 |
| Register | | 528,300 | 697,360 |
| Memory (Kb) | M10K | 17,290 | 22,820 |
| | MLAB | 2,014 | 2,658 |
| Variable-precision DSP Block | | 809 | 1,090 |
| 18 x 18 Multiplier | | 1,618 | 2,180 |

| Resource | | Member Code | |
|--------------------------------|-------------|-------------|-----------|
| | | B3 | B5 |
| FPGA PLL | | 14 | 14 |
| HPS PLL | | 3 | 3 |
| 6 Gbps Transceiver | | 30 | 30 |
| FPGA GPIO ⁽⁸⁾ | | 540 | 540 |
| HPS I/O | | 208 | 208 |
| LVDS | Transmitter | 120 | 120 |
| | Receiver | 136 | 136 |
| PCIe Hard IP Block | | 2 | 2 |
| FPGA Hard Memory Controller | | 3 | 3 |
| HPS Hard Memory Controller | | 1 | 1 |
| ARM Cortex-A9 MPCore Processor | | Dual-core | Dual-core |

Related Information

[High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)

Provides the number of LVDS channels in each device package.

Package Plan**Table 11: Package Plan for Arria V SX Devices**

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

| Member Code | F896 (31 mm) | | | F1152 (35 mm) | | | F1517 (40 mm) | | |
|-------------|-----------------|---------|------|------------------|---------|------|------------------|---------|------|
| | FPGA GPIO | HPS I/O | XCVR | FPGA GPIO | HPS I/O | XCVR | FPGA GPIO | HPS I/O | XCVR |
| B3 | 250 | 208 | 12 | 385 | 208 | 18 | 540 | 208 | 30 |
| B5 | 250 | 208 | 12 | 385 | 208 | 18 | 540 | 208 | 30 |

Arria V ST

This section provides the available options, maximum resource counts, and package plan for the Arria V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

⁽⁸⁾ The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

I/O Vertical Migration for Arria V Devices

Figure 6: Vertical Migration Capability Across Arria V Device Packages and Densities

The arrows indicate the vertical migration paths. Some packages have several migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.

| Variant | Member Code | Package | | | | |
|------------|-------------|---------|------|------|--------|-------|
| | | F672 | F780 | F896 | F 1152 | F1517 |
| Arria V GX | A1 | | | | | |
| | A3 | | | | | |
| | A5 | | | | | |
| | A7 | | | | | |
| | B1 | | | | | |
| | B3 | | | | | |
| | B5 | | | | | |
| | B7 | | | | | |
| Arria V GT | C3 | | | | | |
| | C7 | | | | | |
| | D3 | | | | | |
| | D7 | | | | | |
| Arria V GZ | E1 | | | | | |
| | E3 | | | | | |
| | E5 | | | | | |
| | E7 | | | | | |
| Arria V SX | B3 | | | | | |
| | B5 | | | | | |
| Arria V ST | D3 | | | | | |
| | D5 | | | | | |

You can achieve the vertical migration shaded in red if you use only up to 320 GPIOs, up to nine 6 Gbps transceiver channels, and up to four 10 Gbps transceiver (for Arria V GT devices). This migration path is not shown in the Quartus Prime software Pin Migration View.

Note: To verify the pin migration compatibility, use the Pin Migration View window in the Quartus Prime software Pin Planner.

Note: Except for Arria V GX A5 and A7, and Arria V GT C7 devices, all other Arria V GX and GT devices require a specific power-up sequence. If you plan to migrate your design from Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices, your design must adhere to the same required power-up sequence.

Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- Double accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus Prime design software

Table 14: Variable-Precision DSP Block Configurations for Arria V Devices

| Usage Example | Multiplier Size (Bit) | DSP Block Resource |
|--|-----------------------------|--------------------|
| Low precision fixed point for video applications | Three 9 x 9 | 1 |
| Medium precision fixed point in FIR filters | Two 18 x 18 | 1 |
| FIR filters | Two 18 x 18 with accumulate | 1 |
| Single-precision floating-point implementations | One 27 x 27 | 1 |
| Very high precision fixed point implementations | One 36 x 36 | 2 |

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. Using two DSP block resources, you can also configure a 36 x 36 multiplier for high-precision applications. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

PLL Features

The PLLs in the Arria V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Counter reconfiguration
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- Dynamic phase shift
- Zero delay buffers

Fractional PLL

In addition to integer PLLs, the Arria V devices use a fractional PLL architecture. The devices have up to 16 PLLs, each with 18 output counters. One fractional PLL can use up to 18 output counters and two adjacent fractional PLLs share the 18 output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

FPGA General Purpose I/O

Arria V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- On-chip parallel termination (R_T OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Unused voltage reference (V_{REF}) pins that can be configured as user I/Os (Arria V GX, GT, SX, and ST only)
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

Related Information

[External Memory Interface Spec Estimator](#)

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Arria V devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at less than 170 mW
- 10 Gbps transceivers at less than 165 mW
- 6 Gbps transceivers at less than 105 mW

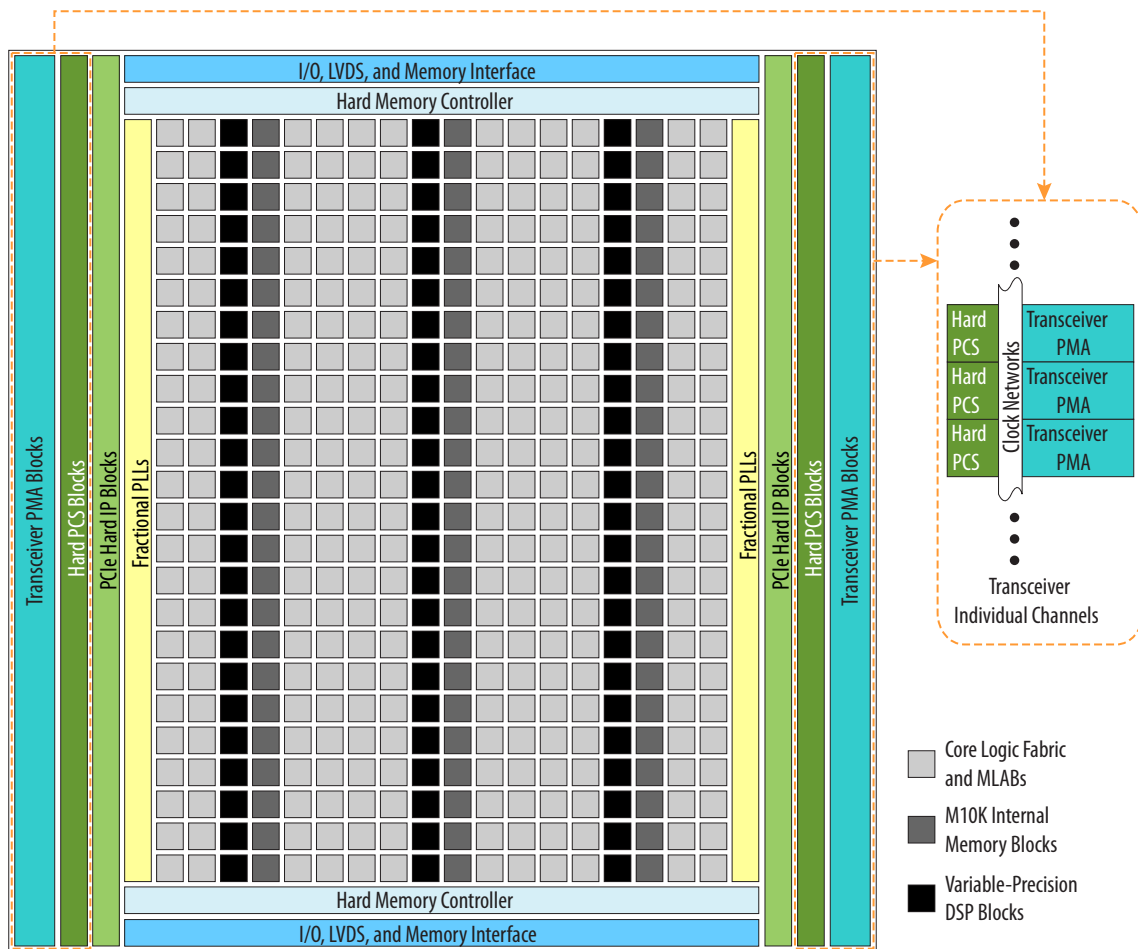
Arria V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left and right outer edges of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

The following figures are graphical representations of a top view of the silicon die, which corresponds to a reverse view for flip chip packages. Different Arria V devices may have different floorplans than the ones shown in the figures.

Figure 9: Device Chip Overview for Arria V GX and GT Devices



| Features | Capability |
|---|---|
| PLL-based clock recovery | Superior jitter tolerance |
| Programmable serializer and deserializer (SERDES) | Flexible SERDES width |
| Equalization and pre-emphasis | <ul style="list-style-type: none"> Arria V GX, GT, SX, and ST devices—Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization Arria V GZ devices—4-tap pre-emphasis and de-emphasis |
| Ring oscillator transmit PLLs | 611 Mbps to 10.3125 Gbps |
| LC oscillator ATX transmit PLLs (Arria V GZ devices only) | 600 Mbps to 12.5 Gbps |
| Input reference clock range | 27 MHz to 710 MHz |
| Transceiver dynamic reconfiguration | Allows the reconfiguration of a single channel without affecting the operation of other channels |

PCS Features

The Arria V core logic connects to the PCS through an 8, 10, 16, 20, 32, 40, 64, 66, or 67 bit interface, depending on the transceiver data rate and protocol. Arria V devices contain PCS hard IP to support PCIe Gen1, Gen2, and Gen3, GbE, Serial RapidIO (SRIO), GPON, and CPRI.

All other standard and proprietary protocols within the following speed ranges are also supported:

- 611 Mbps to 6.5536 Gbps—supported through the custom double-width mode (up to 6.5536 Gbps) and custom single-width mode (up to 3.75 Gbps) of the transceiver PCS hard IP.
- 6.5536 Gbps to 10.3125 Gbps—supported through dedicated 80 or 64 bit interface that bypass the PCS hard IP and connects the PMA directly to the core logic. In Arria V GZ, this is supported in the transceiver PCS hard IP.

Table 21: Transceiver PCS Features for Arria V GX, GT, ST, and SX Devices

| PCS Support ⁽¹³⁾ | Data Rates (Gbps) | Transmitter Data Path Feature | Receiver Data Path Feature |
|---------------------------------------|-------------------|--|--|
| Custom single- and double-width modes | 0.611 to ~6.5536 | <ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder | <ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO |
| SRIO | 1.25 to 6.25 | | |
| Serial ATA | 1.5, 3.0, 6.0 | | |

⁽¹³⁾ Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

| PCS Support ⁽¹³⁾ | Data Rates (Gbps) | Transmitter Data Path Feature | Receiver Data Path Feature |
|---|------------------------------------|--|--|
| PCIe Gen1 (x1, x2, x4, x8) | 2.5 and 5.0 | <ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder PIPE 2.0 interface to the core logic | <ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO Rate match FIFO PIPE 2.0 interface to the core logic |
| PCIe Gen2 ⁽¹⁴⁾ (x1, x2, x4) | | | |
| GbE | 1.25 | <ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder | <ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO Rate match FIFO |
| XAUI ⁽¹⁵⁾ | 3.125 | <ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder XAUI state machine for bonding four channels | <ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO XAUI state machine for realigning four channels Deskew FIFO circuitry |
| SDI | 0.27 ⁽¹⁶⁾ , 1.485, 2.97 | <ul style="list-style-type: none"> Phase compensation FIFO Byte serializer | <ul style="list-style-type: none"> Byte deserializer Phase compensation FIFO |
| GPON ⁽¹⁷⁾ | 1.25 and 2.5 | | |
| CPRI ⁽¹⁸⁾ | 0.6144 to 6.144 | <ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder TX deterministic latency | <ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO RX deterministic latency |

⁽¹³⁾ Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

⁽¹⁴⁾ PCIe Gen2 is supported only through the PCIe hard IP.

⁽¹⁵⁾ XAUI is supported through the soft PCS.

⁽¹⁶⁾ The 0.27 Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

⁽¹⁷⁾ The GPON standard does not support burst mode.

⁽¹⁸⁾ CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through the soft PCS.

Table 22: Transceiver PCS Features for Arria V GZ Devices

| Protocol | Data Rates (Gbps) | Transmitter Data Path Features | Receiver Data Path Features |
|-------------------------------|-------------------|---|--|
| Custom PHY | 0.6 to 9.80 | <ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding | <ul style="list-style-type: none"> Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer Byte ordering |
| GPON | 1.25 and 2.5 | | |
| Custom 10G PHY | 9.98 to 12.5 | <ul style="list-style-type: none"> TX FIFO Gear box Bit-slip | <ul style="list-style-type: none"> RX FIFO Gear box |
| PCIe Gen1 (x1, x2, x4, x8) | 2.5 and 5.0 | <ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding PIPE 2.0 interface to core logic | <ul style="list-style-type: none"> Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer, Byte ordering PIPE 2.0 interface to core logic |
| PCIe Gen2 (x1, x2, x4, x8) | | | |
| PCIe Gen3 (x1, x2, x4, x8) | 8.0 | <ul style="list-style-type: none"> Phase compensation FIFO 128B/130B encoder Scrambler Gear box Bit-slip | <ul style="list-style-type: none"> Block synchronization Rate match FIFO 128B/130B decoder Descrambler Phase compensation FIFO |
| 10GbE | 10.3125 | <ul style="list-style-type: none"> TX FIFO 64B/66B encoder Scrambler Gear box | <ul style="list-style-type: none"> RX FIFO 64B/66B decoder Descrambler Block synchronization Gear box |
| Interlaken | 3.125 to 12.5 | <ul style="list-style-type: none"> TX FIFO Frame generator CRC-32 generator Scrambler Disparity generator Gear box | <ul style="list-style-type: none"> RX FIFO Frame generator CRC-32 checker Frame decoder Descrambler Disparity checker Block synchronization Gear box |

SoC with HPS

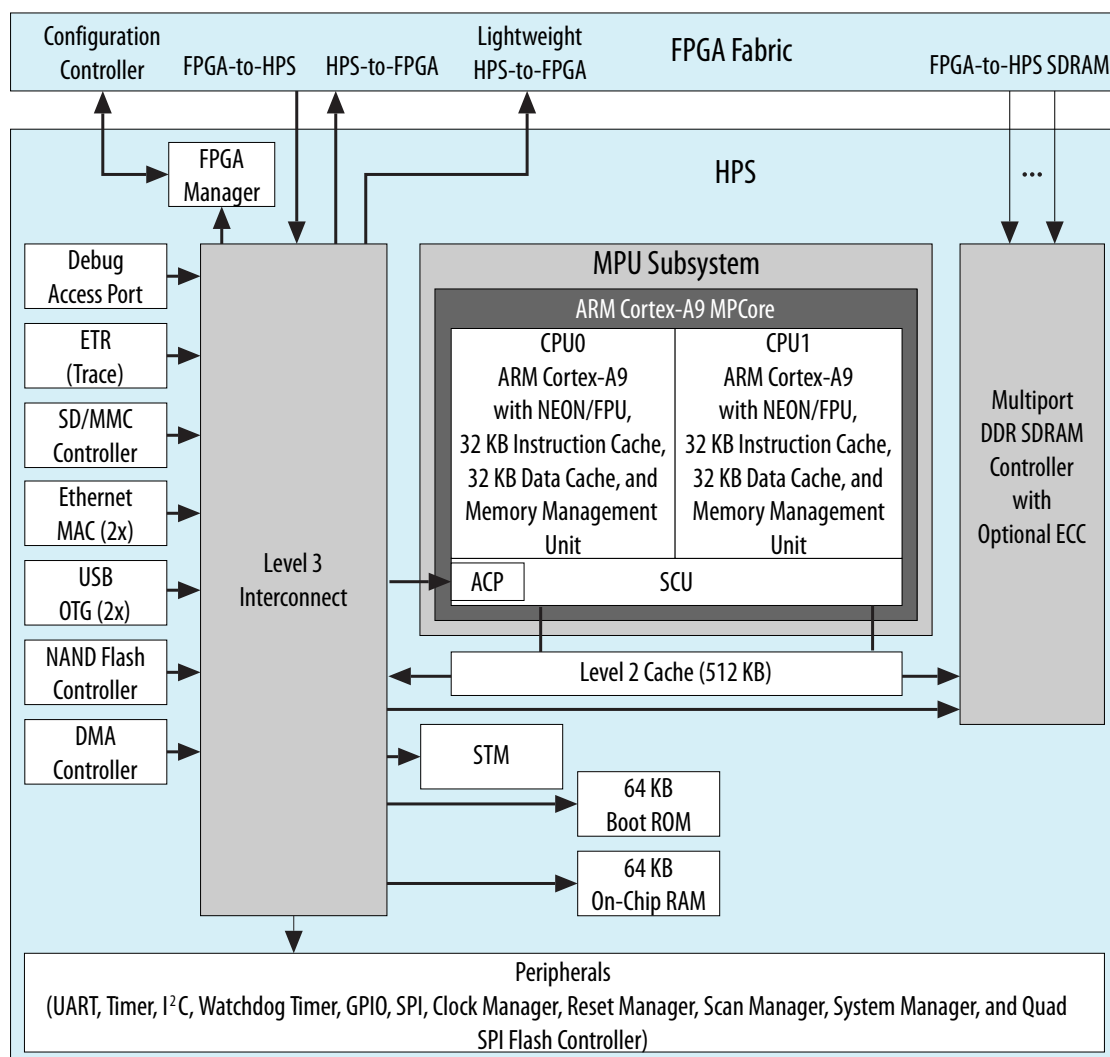
Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

HPS Features

The HPS consists of a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

Figure 12: HPS with Dual-Core ARM Cortex-A9 MPCore Processor



You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Note: Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

Related Information

- [Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines](#)
Provides detailed information about power supply pin connection guidelines and power regulator sharing.
- [Arria V GZ Device Family Pin Connection Guidelines](#)
Provides detailed information about power supply pin connection guidelines and power regulator sharing.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Qsys system integration tool in the Quartus Prime software.

For software development, the ARM-based SoC devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Altera SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Altera sales team.

You can begin device-specific firmware and software development on the Altera SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Related Information

[Altera Worldwide Sales Support](#)

Dynamic and Partial Reconfiguration

The Arria V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA, PCS, and PCIe hard IP blocks with dynamic reconfiguration.

| Date | Version | Changes |
|---------------|------------|---|
| June 2013 | 2013.06.03 | <ul style="list-style-type: none"> Removed statements about contacting Altera for SFF-8431 compliance requirements. Refer to the Transceiver Architecture in Arria V Devices chapter for the requirements. |
| May 2013 | 2013.05.06 | <ul style="list-style-type: none"> Moved all links to the Related Information section of respective topics for easy reference. Added link to the known document issues in the Knowledge Base. Updated the available options, maximum resource counts, and per package information for the Arria V SX and ST device variants. Updated the variable DSP multipliers counts for the Arria V SX and ST device variants. Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature. Added footnote to clarify that MLAB 64 bits depth is available only for Arria V GZ devices. Updated description about power-up sequence requirement for device migration to improve clarity. |
| January 2013 | 2013.01.11 | <ul style="list-style-type: none"> Added the L optional suffix to the Arria V GZ ordering code for the – I3 speed grade. Added a note about the power-up sequence requirement if you plan to migrate your design from the Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices. |
| November 2012 | 2012.11.19 | <ul style="list-style-type: none"> Updated the summary of features. Updated Arria V GZ information regarding 3.3 V I/O support. Removed Arria V GZ engineering sample ordering code. Updated the maximum resource counts for Arria V GX and GZ. Updated Arria V ST ordering codes for transceiver count. Updated transceiver counts for Arria V ST packages. Added simplified floorplan diagrams for Arria V GZ, SX, and ST. Added FPP x32 configuration mode for Arria V GZ only. Updated CvP (PCIe) remote system update support information. Added HPS external memory performance information. Updated template. |
| October 2012 | 3.0 | <ul style="list-style-type: none"> Added Arria V GZ information. Updated Table 1, Table 2, Table 3, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, and Table 21. Added the “Arria V GZ” section. Added Table 8, Table 9 and Table 22. |