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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

Details

Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	925MHz
Primary Attributes	FPGA - 350K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA, FC (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5asxbb3d4f35c4n

Feature	Description
Configuration	<ul style="list-style-type: none">• Tamper protection-comprehensive design protection to protect your valuable IP investments• Enhanced advanced encryption standard (AES) design security features• CvP• Partial and dynamic reconfiguration of the FPGA• Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8, x16, and x32 (Arria V GZ) configuration options• Remote system upgrade

Arria V Device Variants and Packages

Table 3: Device Variants for the Arria V Device Family

Variant	Description
Arria V GX	FPGA with integrated 6.5536 Gbps transceivers that provides bandwidth, cost, and power levels that are optimized for high-volume data and signal-processing applications
Arria V GT	FPGA with integrated 10.3125 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for cost-sensitive data and signal processing applications
Arria V GZ	FPGA with integrated 12.5 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for high-performance and cost-sensitive data and signal processing applications
Arria V SX	SoC with integrated ARM-based HPS and 6.5536 Gbps transceivers
Arria V ST	SoC with integrated ARM-based HPS and 10.3125 Gbps transceivers

Arria V GX

This section provides the available options, maximum resource counts, and package plan for the Arria V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

[Altera Product Selector](#)

Provides the latest information about Altera products.

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
6 Gbps Transceiver		9	9	24	24	24	24	36	36
GPIO ⁽³⁾		416	416	544	544	704	704	704	704
LVD S	Transmitter	67	67	120	120	160	160	160	160
	Receiver	80	80	136	136	176	176	176	176
PCIe Hard IP Block		1	1	2	2	2	2	2	2
Hard Memory Controller		2	2	4	4	4	4	4	4

Related Information

[High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)

Provides the number of LVDS channels in each device package.

Package Plan**Table 5: Package Plan for Arria V GX Devices**

Member Code	F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
A1	336	9	416	9	—	—	—	—
A3	336	9	416	9	—	—	—	—
A5	336	9	384	18	544	24	—	—
A7	336	9	384	18	544	24	—	—
B1	—	—	384	18	544	24	704	24
B3	—	—	384	18	544	24	704	24
B5	—	—	—	—	544	24	704	36
B7	—	—	—	—	544	24	704	36

Arria V GT

This section provides the available options, maximum resource counts, and package plan for the Arria V GT devices.

⁽³⁾ The number of GPIOs does not include transceiver I/Os. In the Quartus® Prime software, the number of user I/Os includes transceiver I/Os.

Resource		Member Code			
		C3	C7	D3	D7
Transceiver	6 Gbps ⁽⁴⁾	3 (9)	6 (24)	6 (24)	6 (36)
	10 Gbps ⁽⁵⁾	4	12	12	20
GPIO ⁽⁶⁾		416	544	704	704
LVDS	Transmitter	68	120	160	160
	Receiver	80	136	176	176
PCIe Hard IP Block		1	2	2	2
Hard Memory Controller		2	4	4	4

Related Information

- [High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)

Provides the number of LVDS channels in each device package.

- [Transceiver Architecture in Arria V Devices](#)

Describes 10 Gbps channels usage conditions and SFF-8431 compliance requirements.

Package Plan

Table 7: Package Plan for Arria V GT Devices

Member Code	F672 (27 mm)			F896 (31 mm)			F1152 (35 mm)			F1517 (40 mm)		
	GPIO	XCVR		GPIO	XCVR		GPIO	XCVR		GPIO	XCVR	
		6-Gbps	10-Gbps		6-Gbps	10-Gbps		6-Gbps	10-Gbps		6-Gbps	10-Gbps
C3	336	3 (9)	4	416	3 (9)	4	—	—	—	—	—	—
C7	—	—	—	384	6 (18)	8	544	6 (24)	12	—	—	—
D3	—	—	—	384	6 (18)	8	544	6 (24)	12	704	6 (24)	12
D7	—	—	—	—	—	—	544	6 (24)	12	704	6 (36)	20

The 6-Gbps transceiver counts are for dedicated 6-Gbps channels. You can also configure any pair of 10-Gbps channels as three 6-Gbps channels—the total number of 6-Gbps channels are shown in brackets. For example, you can also configure the Arria V GT D7 device in the F1517 package with nine 6-Gbps

⁽⁴⁾ The 6 Gbps transceiver counts are for dedicated 6-Gbps channels. You can also configure any pair of 10 Gbps channels as three 6 Gbps channels—the total number of 6 Gbps channels are shown in brackets.

⁽⁵⁾ Chip-to-chip connections only. For 10 Gbps channel usage conditions, refer to the Transceiver Architecture in Arria V Devices chapter.

⁽⁶⁾ The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

and eighteen 10-Gbps, twelve 6-Gbps and sixteen 10-Gbps, fifteen 6-Gbps and fourteen 10-Gbps, or up to thirty-six 6-Gbps with no 10-Gbps channels.

Arria V GZ

This section provides the available options, maximum resource counts, and package plan for the Arria V GZ devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

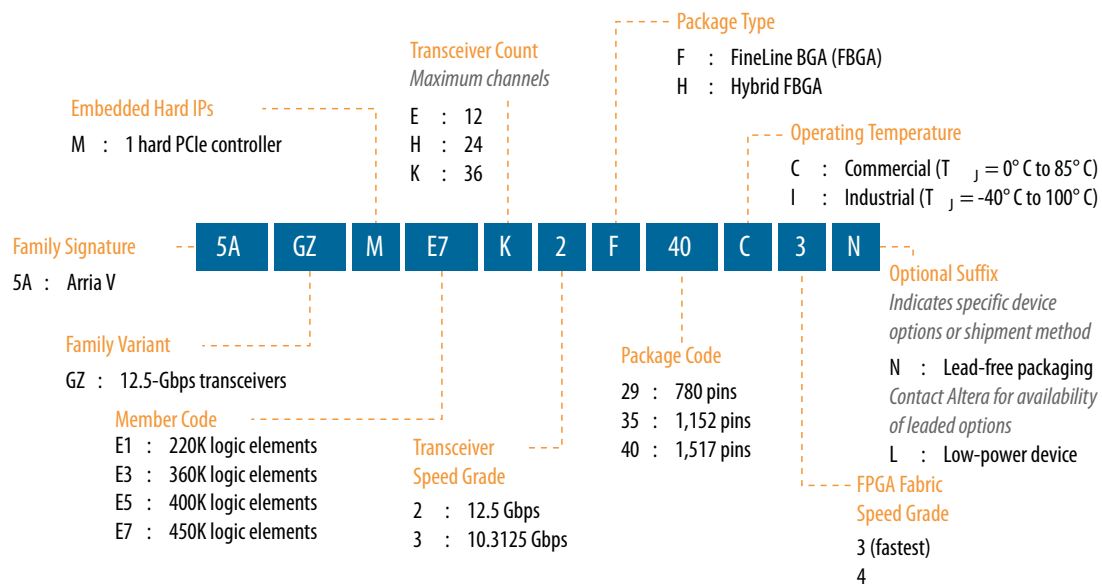
Related Information

Altera Product Selector

Provides the latest information about Altera products.

Available Options

Figure 3: Sample Ordering Code and Available Options for Arria V GZ Devices



Note: Low-power device option is available only for –3 speed grade at industrial temperature

Maximum Resources

Table 8: Maximum Resource Counts for Arria V GZ Devices

Resource	Member Code			
	E1	E3	E5	E7
Logic Elements (LE) (K)	220	360	400	450
ALM	83,020	135,840	150,960	169,800
Register	332,080	543,360	603,840	679,200

Resource		Member Code			
		E1	E3	E5	E7
Memory (Kb)	M20K	11,700	19,140	28,800	34,000
	MLAB	2,594	4,245	4,718	5,306
Variable-precision DSP Block		800	1,044	1,092	1,139
18 x 18 Multiplier		1,600	2,088	2,184	2,278
PLL		20	20	24	24
12.5 Gbps Transceiver		24	24	36	36
GPIO ⁽⁷⁾		414	414	674	674
LVDS	Transmitter	99	99	166	166
	Receiver	108	108	168	168
PCIe Hard IP Block		1	1	1	1

Related Information

[High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)

Provides the number of LVDS channels in each device package.

Package Plan**Table 9: Package Plan for Arria V GZ Devices**

Member Code	H780 (33 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
E1	342	12	414	24	—	—
E3	342	12	414	24	—	—
E5	—	—	534	24	674	36
E7	—	—	534	24	674	36

Arria V SX

This section provides the available options, maximum resource counts, and package plan for the Arria V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

⁽⁷⁾ The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

I/O Vertical Migration for Arria V Devices

Figure 6: Vertical Migration Capability Across Arria V Device Packages and Densities

The arrows indicate the vertical migration paths. Some packages have several migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.

Variant	Member Code	Package				
		F672	F780	F896	F 1152	F1517
Arria V GX	A1					
	A3					
	A5					
	A7					
	B1					
	B3					
	B5					
	B7					
Arria V GT	C3					
	C7					
	D3					
	D7					
Arria V GZ	E1					
	E3					
	E5					
	E7					
Arria V SX	B3					
	B5					
Arria V ST	D3					
	D5					

You can achieve the vertical migration shaded in red if you use only up to 320 GPIOs, up to nine 6 Gbps transceiver channels, and up to four 10 Gbps transceiver (for Arria V GT devices). This migration path is not shown in the Quartus Prime software Pin Migration View.

Note: To verify the pin migration compatibility, use the Pin Migration View window in the Quartus Prime software Pin Planner.

Note: Except for Arria V GX A5 and A7, and Arria V GT C7 devices, all other Arria V GX and GT devices require a specific power-up sequence. If you plan to migrate your design from Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices, your design must adhere to the same required power-up sequence.

Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- Double accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus Prime design software

Table 14: Variable-Precision DSP Block Configurations for Arria V Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters	Two 18 x 18 with accumulate	1
Single-precision floating-point implementations	One 27 x 27	1
Very high precision fixed point implementations	One 36 x 36	2

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. Using two DSP block resources, you can also configure a 36 x 36 multiplier for high-precision applications. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Types of Embedded Memory

The Arria V devices contain two types of memory blocks:

- 20 Kb M20K or 10 Kb M10K blocks—blocks of dedicated memory resources. The M20K and M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Arria V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB. You can also configure these ALMs, in Arria V GZ devices, as ten 64 x 1 blocks, giving you one 64 x 10 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Arria V Devices

Table 16: Embedded Memory Capacity and Distribution in Arria V Devices

Variant	Member Code	M20K		M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Arria V GX	A1	—	—	800	8,000	741	463	8,463
	A3	—	—	1,051	10,510	1538	961	11,471
	A5	—	—	1,180	11,800	1877	1,173	12,973
	A7	—	—	1,366	13,660	2317	1,448	15,108
	B1	—	—	1,510	15,100	2964	1,852	16,952
	B3	—	—	1,726	17,260	3357	2,098	19,358
	B5	—	—	2,054	20,540	4052	2,532	23,072
	B7	—	—	2,414	24,140	4650	2,906	27,046
Arria V GT	C3	—	—	1,051	10,510	1538	961	11,471
	C7	—	—	1,366	13,660	2317	1,448	15,108
	D3	—	—	1,726	17,260	3357	2,098	19,358
	D7	—	—	2,414	24,140	4650	2,906	27,046
Arria V GZ	E1	585	11,700	—	—	4,151	2,594	14,294
	E3	957	19,140	—	—	6,792	4,245	23,385
	E5	1,440	28,800	—	—	7,548	4,718	33,518
	E7	1,700	34,000	—	—	8,490	5,306	39,306
Arria V SX	B3	—	—	1,729	17,290	3223	2,014	19,304
	B5	—	—	2,282	22,820	4253	2,658	25,478

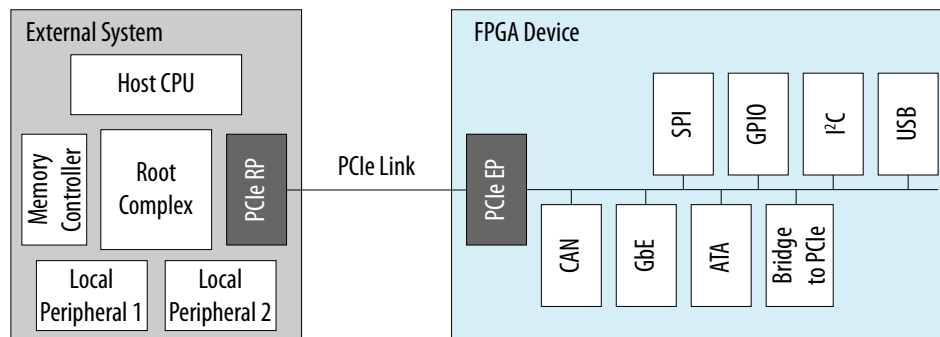
PCIe Gen1, Gen2, and Gen 3 Hard IP

Arria V devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen3, Gen 2, and Gen 1 end point and root port for up to x8 lane configuration.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

Figure 8: PCIe Multifunction for Arria V Devices



The Arria V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Arria V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Arria V device provides improved end-to-end datapath protection using ECC.

External Memory Interface

This section provides an overview of the external memory interface in Arria V devices.

Hard and Soft Memory Controllers

Arria V GX,GT, SX, and ST devices support up to four hard memory controllers for DDR3 and DDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Arria V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Arria V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices, QDR II+, QDR II, and DDR II+ SRAM devices, and RLDRAM II devices for maximum flexibility.

Note: DDR3 SDRAM leveling is supported only in Arria V GZ devices.

Related Information

[External Memory Interface Spec Estimator](#)

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Arria V devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at less than 170 mW
- 10 Gbps transceivers at less than 165 mW
- 6 Gbps transceivers at less than 105 mW

Arria V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left and right outer edges of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

The following figures are graphical representations of a top view of the silicon die, which corresponds to a reverse view for flip chip packages. Different Arria V devices may have different floorplans than the ones shown in the figures.

Figure 10: Device Chip Overview for Arria V GZ Devices

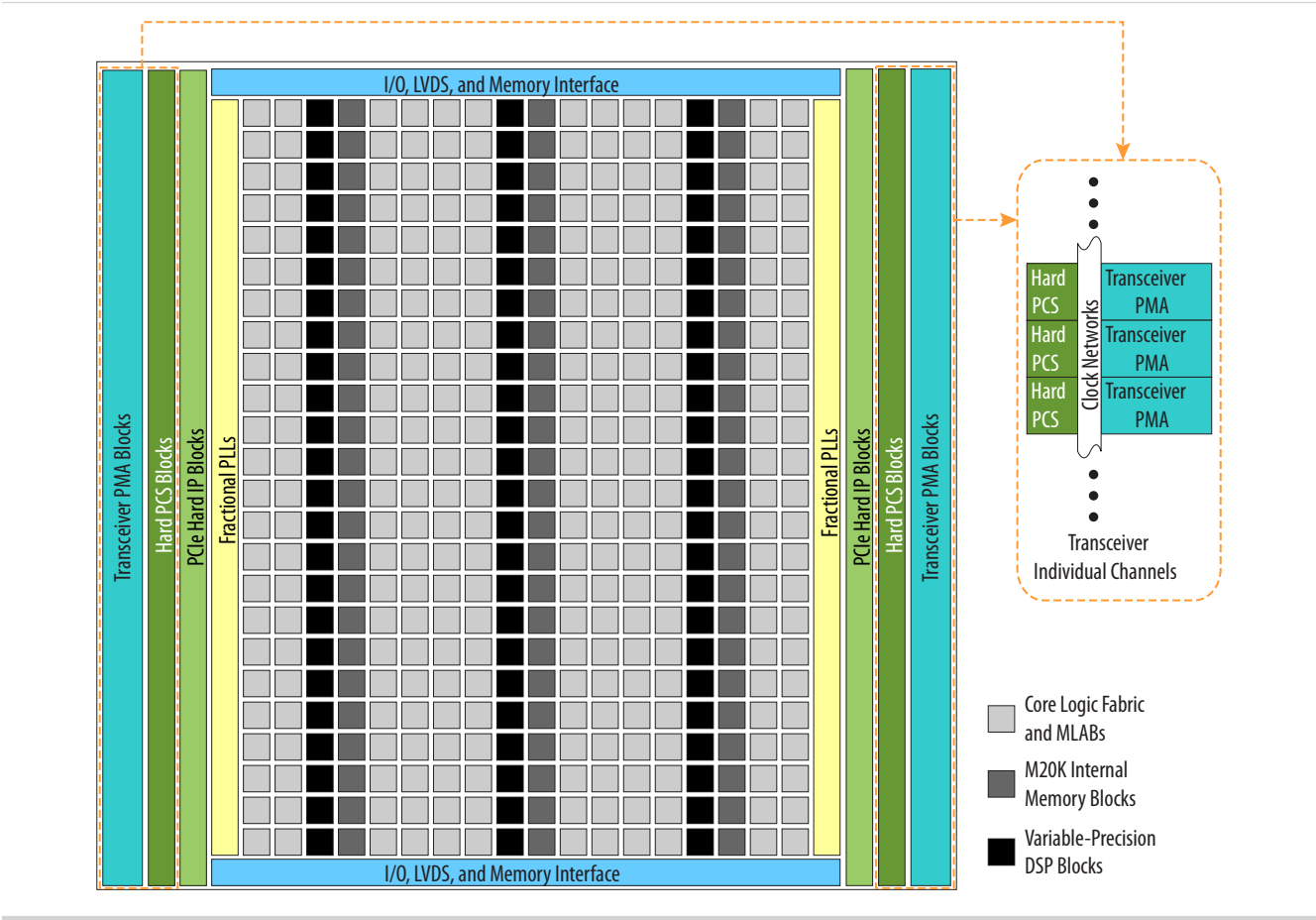
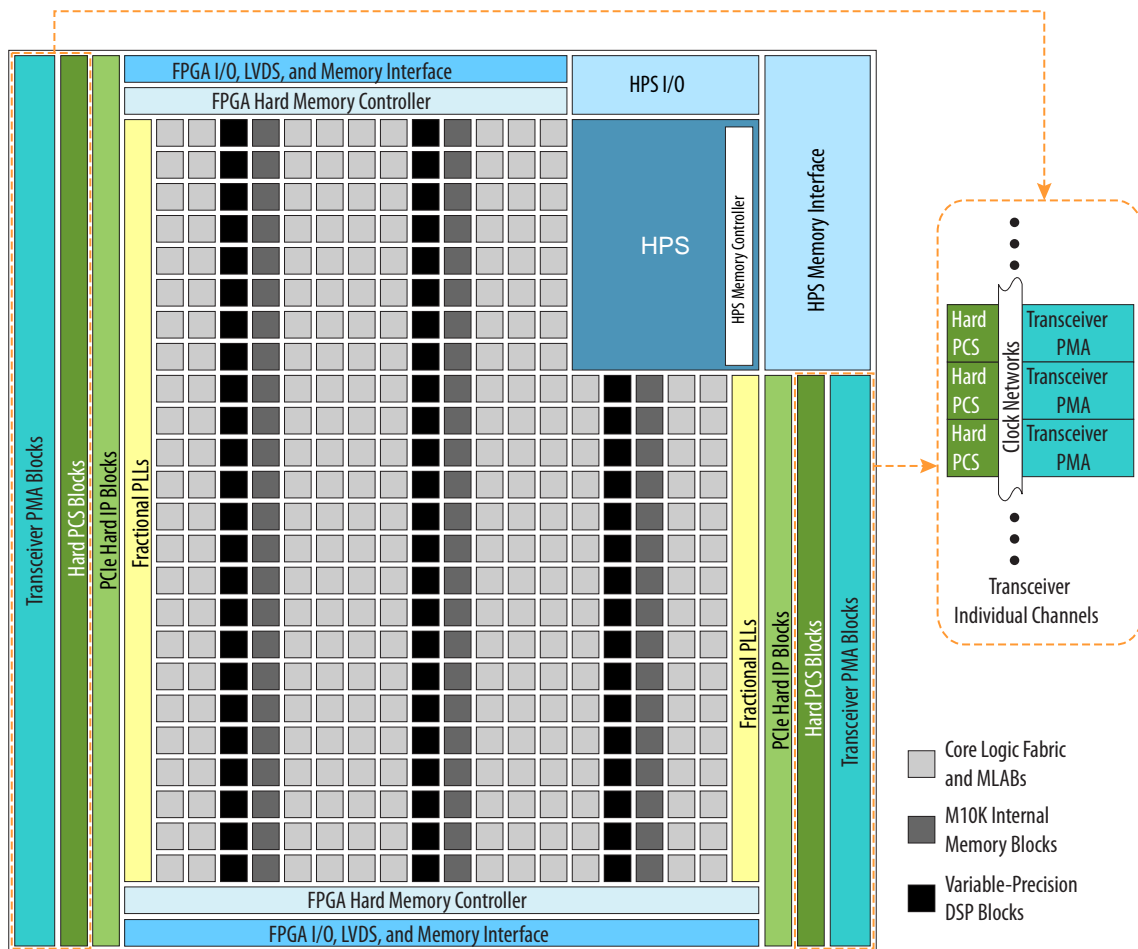


Figure 11: Device Chip Overview for Arria V SX and ST Devices



PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 20: PMA Features of the Transceivers in Arria V Devices

Features	Capability
Backplane support	<ul style="list-style-type: none"> Arria V GX, GT, SX, and ST devices—Driving capability at 6.5536 Gbps with up to 25 dB channel loss Arria V GZ devices—Driving capability at 12.5 Gbps with up to 16 dB channel loss
Chip-to-chip support	<ul style="list-style-type: none"> Arria V GX, GT, SX, and ST devices—Up to 10.3125 Gbps Arria V GZ devices—Up to 12.5 Gbps

Features	Capability
PLL-based clock recovery	Superior jitter tolerance
Programmable serializer and deserializer (SERDES)	Flexible SERDES width
Equalization and pre-emphasis	<ul style="list-style-type: none"> Arria V GX, GT, SX, and ST devices—Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization Arria V GZ devices—4-tap pre-emphasis and de-emphasis
Ring oscillator transmit PLLs	611 Mbps to 10.3125 Gbps
LC oscillator ATX transmit PLLs (Arria V GZ devices only)	600 Mbps to 12.5 Gbps
Input reference clock range	27 MHz to 710 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

PCS Features

The Arria V core logic connects to the PCS through an 8, 10, 16, 20, 32, 40, 64, 66, or 67 bit interface, depending on the transceiver data rate and protocol. Arria V devices contain PCS hard IP to support PCIe Gen1, Gen2, and Gen3, GbE, Serial RapidIO (SRIO), GPON, and CPRI.

All other standard and proprietary protocols within the following speed ranges are also supported:

- 611 Mbps to 6.5536 Gbps—supported through the custom double-width mode (up to 6.5536 Gbps) and custom single-width mode (up to 3.75 Gbps) of the transceiver PCS hard IP.
- 6.5536 Gbps to 10.3125 Gbps—supported through dedicated 80 or 64 bit interface that bypass the PCS hard IP and connects the PMA directly to the core logic. In Arria V GZ, this is supported in the transceiver PCS hard IP.

Table 21: Transceiver PCS Features for Arria V GX, GT, ST, and SX Devices

PCS Support ⁽¹³⁾	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Custom single- and double-width modes	0.611 to ~6.5536	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder 	<ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO
SRIO	1.25 to 6.25		
Serial ATA	1.5, 3.0, 6.0		

⁽¹³⁾ Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

PCS Support ⁽¹³⁾	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
PCIe Gen1 (x1, x2, x4, x8)	2.5 and 5.0	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder PIPE 2.0 interface to the core logic 	<ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO Rate match FIFO PIPE 2.0 interface to the core logic
PCIe Gen2 ⁽¹⁴⁾ (x1, x2, x4)			
GbE	1.25	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder 	<ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO Rate match FIFO
XAUI ⁽¹⁵⁾	3.125	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder XAUI state machine for bonding four channels 	<ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO XAUI state machine for realigning four channels Deskew FIFO circuitry
SDI	0.27 ⁽¹⁶⁾ , 1.485, 2.97	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 	<ul style="list-style-type: none"> Byte deserializer Phase compensation FIFO
GPON ⁽¹⁷⁾	1.25 and 2.5		
CPRI ⁽¹⁸⁾	0.6144 to 6.144	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder TX deterministic latency 	<ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO RX deterministic latency

⁽¹³⁾ Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

⁽¹⁴⁾ PCIe Gen2 is supported only through the PCIe hard IP.

⁽¹⁵⁾ XAUI is supported through the soft PCS.

⁽¹⁶⁾ The 0.27 Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

⁽¹⁷⁾ The GPON standard does not support burst mode.

⁽¹⁸⁾ CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through the soft PCS.

Table 22: Transceiver PCS Features for Arria V GZ Devices

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
Custom PHY	0.6 to 9.80	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding 	<ul style="list-style-type: none"> Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer Byte ordering
GPON	1.25 and 2.5		
Custom 10G PHY	9.98 to 12.5	<ul style="list-style-type: none"> TX FIFO Gear box Bit-slip 	<ul style="list-style-type: none"> RX FIFO Gear box
PCIe Gen1 (x1, x2, x4, x8)	2.5 and 5.0	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding PIPE 2.0 interface to core logic 	<ul style="list-style-type: none"> Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer, Byte ordering PIPE 2.0 interface to core logic
PCIe Gen2 (x1, x2, x4, x8)			
PCIe Gen3 (x1, x2, x4, x8)	8.0	<ul style="list-style-type: none"> Phase compensation FIFO 128B/130B encoder Scrambler Gear box Bit-slip 	<ul style="list-style-type: none"> Block synchronization Rate match FIFO 128B/130B decoder Descrambler Phase compensation FIFO
10GbE	10.3125	<ul style="list-style-type: none"> TX FIFO 64B/66B encoder Scrambler Gear box 	<ul style="list-style-type: none"> RX FIFO 64B/66B decoder Descrambler Block synchronization Gear box
Interlaken	3.125 to 12.5	<ul style="list-style-type: none"> TX FIFO Frame generator CRC-32 generator Scrambler Disparity generator Gear box 	<ul style="list-style-type: none"> RX FIFO Frame generator CRC-32 checker Frame decoder Descrambler Disparity checker Block synchronization Gear box

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
40GBASE-R Ethernet	4 x 10.3125	<ul style="list-style-type: none"> TX FIFO 64B/66B encoder Scrambler Alignment marker insertion Gearbox Block stripper 	<ul style="list-style-type: none"> RX FIFO 64B/66B decoder Descrambler Lane reorder Deskew Alignment marker lock Block synchronization Gear box Destripper
100GBASE-R Ethernet	10 x 10.3125		
40G and 100G OTN	(4 +1) x 11.3	<ul style="list-style-type: none"> TX FIFO Channel bonding Byte serializer 	<ul style="list-style-type: none"> RX FIFO Lane deskew Byte deserializer
	(10 +1) x 11.3		
GbE	1.25	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding GbE state machine 	<ul style="list-style-type: none"> Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer Byte ordering GbE state machine
XAUI	3.125 to 4.25	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding XAUI state machine for bonding four channels 	<ul style="list-style-type: none"> Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer Byte ordering XAUI state machine for realigning four channels
SRIO	1.25 to 6.25	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding SRIO V2.1-compliant x2 and x4 channel bonding 	<ul style="list-style-type: none"> Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer Byte ordering SRIO V2.1-compliant x2 and x4 deskew state machine

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 533 MHz (1066 Mbps data rate).

FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

Partial Reconfiguration

Note: Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Quartus Prime design software. With the Altera solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Table 23: Configuration Modes and Features of Arria V Devices

Arria V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V⁽¹⁹⁾ programming voltages and several configuration modes.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration ⁽²⁰⁾	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—

⁽¹⁹⁾ Arria V GZ does not support 3.3 V.

⁽²⁰⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration ⁽²⁰⁾	Remote System Update
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes ⁽²¹⁾	
	32 bits ⁽²²⁾	100	—	Yes	Yes	—	
CvP (PCIe)	x1, x2, x4, and x8 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—
Configuration via HPS	16 bits	125	—	Yes	Yes	Yes ⁽²¹⁾	Parallel flash loader
	32 bits	100	—	Yes	Yes	—	

Instead of using an external flash or ROM, you can configure the Arria V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Arria V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

Note: Although Arria V GZ devices support PCIe Gen3, you can use only PCIe Gen1 and PCIe Gen2 for CvP configuration scheme.

Related Information

[Configuration via Protocol \(CvP\) Implementation in Altera FPGAs User Guide](#)

Provides more information about CvP.

Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Arria V devices consume less power than previous generation Arria V FPGAs:

- Total device core power consumption—less by up to 50%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Arria V devices contain several hard IP blocks, including PCIe Gen1, Gen2, and Gen3, GbE, SRIO, GPON, and CPRI protocols, that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

⁽²⁰⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

⁽²¹⁾ Supported at a maximum clock rate of 62.5 MHz.

⁽²²⁾ Arria V GZ only

Document Revision History

Date	Version	Changes
December 2015	2015.12.21	<ul style="list-style-type: none"> Updated RoHS and optional suffix information in sample ordering code and available options diagrams for Arria V GX and GT devices. Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.
January 2015	2015.01.23	<ul style="list-style-type: none"> Updated package dimension for Arria V GZ H780 package from 29 mm to 33 mm. Updated dual-core ARM Cortex-A9 MPCore processor maximum frequency from 800 MHz to 1.05 GHz.
December 2013	2013.12.26	<ul style="list-style-type: none"> 10-Gbps Ethernet (10GbE) PCS and Interlaken PCS are for Arria V GZ only. Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. Added link to Altera Product Selector for each device variant. Added leaded package options. Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F896 package from 170 to 250. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1152 package from 350 to 385. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1517 package from 528 to 540. Corrected LVDS Transmitter for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 devices from 121 to 120. Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance. Added x2 for PCIe Gen3, Gen 2, and Gen 1.
August 2013	2013.08.19	<ul style="list-style-type: none"> Removed the note about the PCIe hard IP on the right side of the device in the F896 package of the Arria V GX variant. These devices do not have PCIe hard IP on the right side. Added transceiver speed grade 6 to the available options of the Arria V SX variant. Corrected the maximum LVDS transmitter channel counts for the Arria V GX A1 and A3 devices from 68 to 67. Corrected the maximum FPGA GPIO count for Arria V ST D5 devices from 540 to 528.