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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

#### **Details**

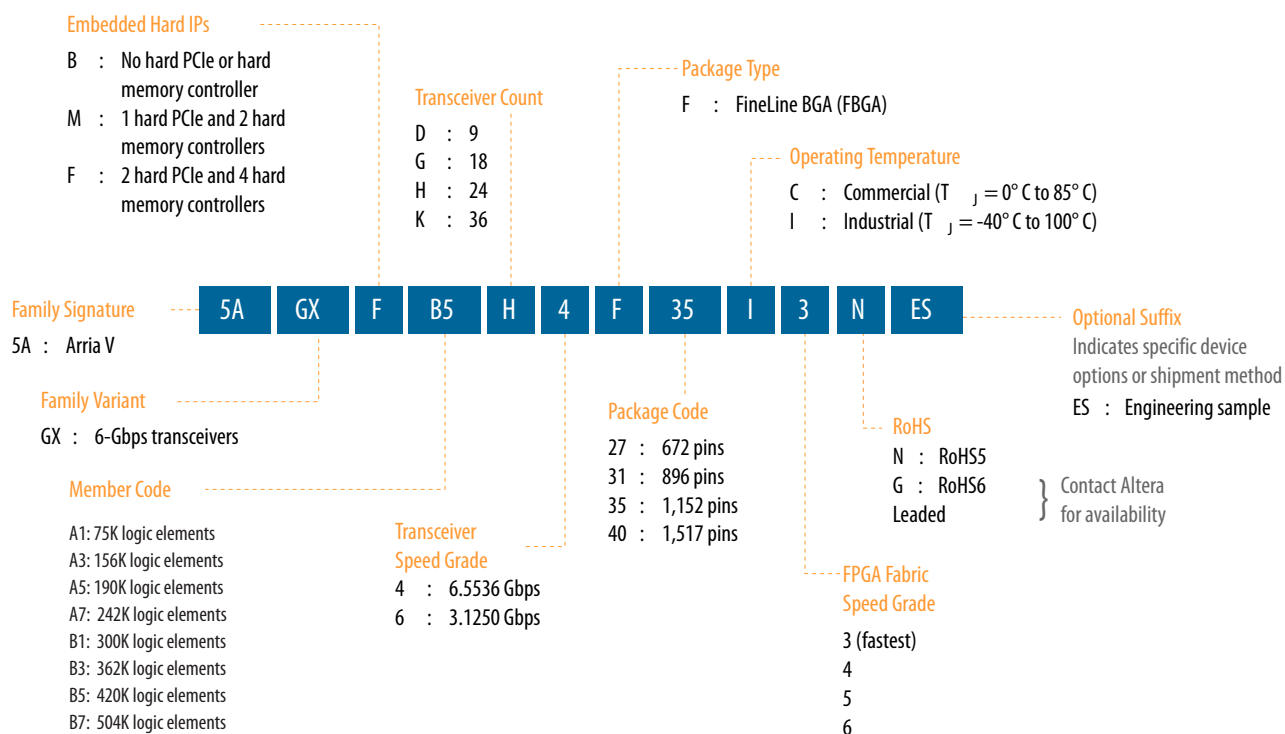
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	700MHz
Primary Attributes	FPGA - 350K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA, FC (40x40)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5asxbb3d6f40c6n">https://www.e-xfl.com/product-detail/intel/5asxbb3d6f40c6n</a>

Feature	Description
FPGA General-purpose I/Os (GPIOs)	<ul style="list-style-type: none"> <li>1.6 Gbps LVDS receiver and transmitter</li> <li>800 MHz/1.6 Gbps external memory interface</li> <li>On-chip termination (OCT)</li> <li>3.3 V support <sup>(2)</sup></li> </ul>
External Memory Interface	<p>Memory interfaces with low latency:</p> <ul style="list-style-type: none"> <li>Hard memory controller-up to 1.066 Gbps</li> <li>Soft memory controller-up to 1.6 Gbps</li> </ul>
Low-power high-speed serial interface	<ul style="list-style-type: none"> <li>600 Mbps to 12.5 Gbps integrated transceiver speed</li> <li>Less than 105 mW per channel at 6 Gbps, less than 165 mW per channel at 10 Gbps, and less than 170 mW per channel at 12.5 Gbps</li> <li>Transmit pre-emphasis and receiver equalization</li> <li>Dynamic partial reconfiguration of individual channels</li> <li>Physical medium attachment (PMA) with soft PCS that supports 9.8304 Gbps CPRI ( Arria V GT and ST only)</li> <li>PMA with hard PCS that supports up to 9.8 Gbps CPRI ( Arria V GZ only)</li> <li>Hard PCS that supports 10GBASE-R and 10GBASE-KR ( Arria V GZ only)</li> </ul>
HPS ( Arria V SX and ST devices only)	<ul style="list-style-type: none"> <li>Dual-core ARM Cortex-A9 MPCore processor—up to 1.05 GHz maximum frequency with support for symmetric and asymmetric multiprocessing</li> <li>Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, serial peripheral interface (SPI), I2C interface, and up to 85 HPS GPIO interfaces</li> <li>System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers</li> <li>On-chip RAM and boot ROM</li> <li>HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa</li> <li>FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller</li> <li>ARM CoreSight™ JTAG debug access port, trace port, and on-chip trace storage</li> </ul>

<sup>(2)</sup> Arria V GZ devices support 3.3 V with a 3.0 V V<sub>CCIO</sub>.

## Available Options

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



## Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
Logic Elements (LE) (K)		75	156	190	242	300	362	420	504
ALM		28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240
Register		113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960
Mem ory (Kb)	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
	MLAB	463	961	1,173	1,448	1,852	2,098	2,532	2,906
Variable-precision DSP Block		240	396	600	800	920	1,045	1,092	1,156
18 x 18 Multiplier		480	792	1,200	1,600	1,840	2,090	2,184	2,312
PLL		10	10	12	12	12	12	16	16

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
6 Gbps Transceiver		9	9	24	24	24	24	36	36
GPIO <sup>(3)</sup>		416	416	544	544	704	704	704	704
LVD S	Transmitter	67	67	120	120	160	160	160	160
	Receiver	80	80	136	136	176	176	176	176
PCIe Hard IP Block		1	1	2	2	2	2	2	2
Hard Memory Controller		2	2	4	4	4	4	4	4

**Related Information**

[High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)

Provides the number of LVDS channels in each device package.

**Package Plan****Table 5: Package Plan for Arria V GX Devices**

Member Code	F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
A1	336	9	416	9	—	—	—	—
A3	336	9	416	9	—	—	—	—
A5	336	9	384	18	544	24	—	—
A7	336	9	384	18	544	24	—	—
B1	—	—	384	18	544	24	704	24
B3	—	—	384	18	544	24	704	24
B5	—	—	—	—	544	24	704	36
B7	—	—	—	—	544	24	704	36

**Arria V GT**

This section provides the available options, maximum resource counts, and package plan for the Arria V GT devices.

<sup>(3)</sup> The number of GPIOs does not include transceiver I/Os. In the Quartus® Prime software, the number of user I/Os includes transceiver I/Os.

and eighteen 10-Gbps, twelve 6-Gbps and sixteen 10-Gbps, fifteen 6-Gbps and fourteen 10-Gbps, or up to thirty-six 6-Gbps with no 10-Gbps channels.

## Arria V GZ

This section provides the available options, maximum resource counts, and package plan for the Arria V GZ devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

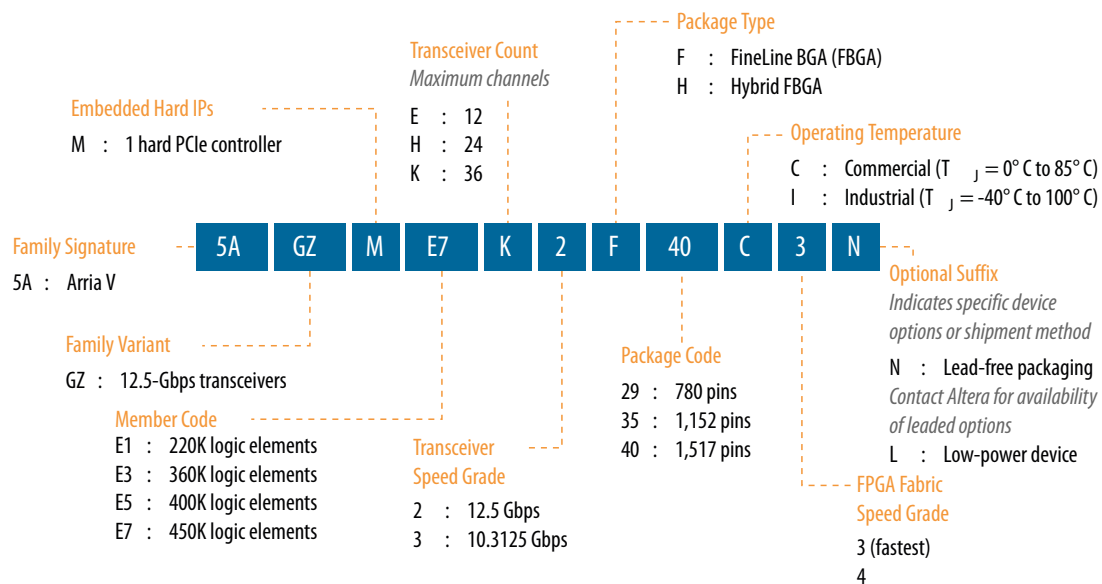
### Related Information

#### Altera Product Selector

Provides the latest information about Altera products.

## Available Options

Figure 3: Sample Ordering Code and Available Options for Arria V GZ Devices



Note: Low-power device option is available only for –3 speed grade at industrial temperature

## Maximum Resources

Table 8: Maximum Resource Counts for Arria V GZ Devices

Resource	Member Code			
	E1	E3	E5	E7
Logic Elements (LE) (K)	220	360	400	450
ALM	83,020	135,840	150,960	169,800
Register	332,080	543,360	603,840	679,200

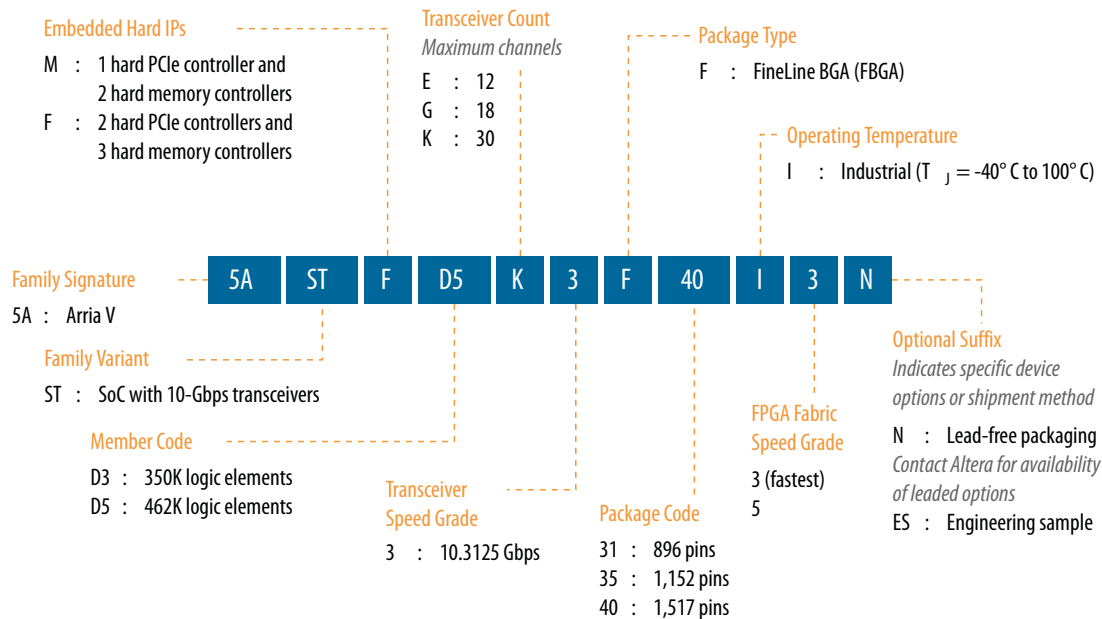
## Related Information

[Altera Product Selector](#)

Provides the latest information about Altera products.

## Available Options

Figure 5: Sample Ordering Code and Available Options for Arria V ST Devices



## Maximum Resources

Table 12: Maximum Resource Counts for Arria V ST Devices

Resource		Member Code	
		D3	D5
Logic Elements (LE) (K)		350	462
ALM		132,075	174,340
Register		528,300	697,360
Memory (Kb)	M10K	17,290	22,820
	MLAB	2,014	2,658
Variable-precision DSP Block		809	1,090
18 x 18 Multiplier		1,618	2,180
FPGA PLL		14	14
HPS PLL		3	3
Transceiver	6-Gbps	30	30
	10-Gbps <sup>(9)</sup>	16	16

## Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- Double accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus Prime design software

**Table 14: Variable-Precision DSP Block Configurations for Arria V Devices**

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters	Two 18 x 18 with accumulate	1
Single-precision floating-point implementations	One 27 x 27	1
Very high precision fixed point implementations	One 36 x 36	2

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. Using two DSP block resources, you can also configure a 36 x 36 multiplier for high-precision applications. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

## Types of Embedded Memory

The Arria V devices contain two types of memory blocks:

- 20 Kb M20K or 10 Kb M10K blocks—blocks of dedicated memory resources. The M20K and M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Arria V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB. You can also configure these ALMs, in Arria V GZ devices, as ten 64 x 1 blocks, giving you one 64 x 10 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Arria V Devices

Table 16: Embedded Memory Capacity and Distribution in Arria V Devices

Variant	Member Code	M20K		M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Arria V GX	A1	—	—	800	8,000	741	463	8,463
	A3	—	—	1,051	10,510	1538	961	11,471
	A5	—	—	1,180	11,800	1877	1,173	12,973
	A7	—	—	1,366	13,660	2317	1,448	15,108
	B1	—	—	1,510	15,100	2964	1,852	16,952
	B3	—	—	1,726	17,260	3357	2,098	19,358
	B5	—	—	2,054	20,540	4052	2,532	23,072
	B7	—	—	2,414	24,140	4650	2,906	27,046
Arria V GT	C3	—	—	1,051	10,510	1538	961	11,471
	C7	—	—	1,366	13,660	2317	1,448	15,108
	D3	—	—	1,726	17,260	3357	2,098	19,358
	D7	—	—	2,414	24,140	4650	2,906	27,046
Arria V GZ	E1	585	11,700	—	—	4,151	2,594	14,294
	E3	957	19,140	—	—	6,792	4,245	23,385
	E5	1,440	28,800	—	—	7,548	4,718	33,518
	E7	1,700	34,000	—	—	8,490	5,306	39,306
Arria V SX	B3	—	—	1,729	17,290	3223	2,014	19,304
	B5	—	—	2,282	22,820	4253	2,658	25,478



Variant	Member Code	M20K		M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Arria V ST	D3	—	—	1,729	17,290	3223	2,014	19,304
	D5	—	—	2,282	22,820	4253	2,658	25,478

## Embedded Memory Configurations

**Table 17: Supported Embedded Memory Block Configurations for Arria V Devices**

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64 <sup>(11)</sup>	x10
M20K	512	x40
	1K	x20
	2K	x10
	4K	x5
	8K	x2
	16K	x1
M10K	256	x40 or x32
	512	x20 or x16
	1K	x10 or x8
	2K	x5 or x4
	4K	x2
	8K	x1

## Clock Networks and PLL Clock Sources

650 MHz Arria V devices have 16 global clock networks capable of up to operation. The clock network architecture is based on Altera's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

**Note:** To reduce power consumption, the Quartus Prime software identifies all unused sections of the clock network and powers them down.

<sup>(11)</sup> Available for Arria V GZ devices only.

## PLL Features

The PLLs in the Arria V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Counter reconfiguration
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- Dynamic phase shift
- Zero delay buffers

## Fractional PLL

In addition to integer PLLs, the Arria V devices use a fractional PLL architecture. The devices have up to 16 PLLs, each with 18 output counters. One fractional PLL can use up to 18 output counters and two adjacent fractional PLLs share the 18 output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

## FPGA General Purpose I/O

Arria V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage ( $V_{OD}$ ) and programmable pre-emphasis
- On-chip parallel termination ( $R_T$  OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Unused voltage reference ( $V_{REF}$ ) pins that can be configured as user I/Os (Arria V GX, GT, SX, and ST only)
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

## External Memory Performance

**Table 18: External Memory Interface Performance in Arria V Devices**

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)	
		Arria V GX, GT, SX, and ST	Arria V GX, GT, SX, and ST	Arria V GZ
DDR3 SDRAM	1.5	533	667	800
	1.35	533	600	800
DDR2 SDRAM	1.8	400	400	400
LPDDR2 SDRAM	1.2	—	400	—
RLDRAM 3	1.2	—	—	667
RLDRAM II	1.8	—	400	533
	1.5	—	400	533
QDR II+ SRAM	1.8	—	400	500
	1.5	—	400	500
QDR II SRAM	1.8	—	400	333
	1.5	—	400	333
DDR II+ SRAM <sup>(12)</sup>	1.8	—	400	—
	1.5	—	400	—

### Related Information

#### [External Memory Interface Spec Estimator](#)

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

## HPS External Memory Performance

**Table 19: HPS External Memory Interface Performance**

The hard processor system (HPS) is available in Arria V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	533
	1.35	533
LPDDR2 SDRAM	1.2	333

<sup>(12)</sup> Not available as Altera® IP.

#### Related Information

##### [External Memory Interface Spec Estimator](#)

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

## Low-Power Serial Transceivers

Arria V devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at less than 170 mW
- 10 Gbps transceivers at less than 165 mW
- 6 Gbps transceivers at less than 105 mW

Arria V transceivers are designed to be compliant with a wide range of protocols and data rates.

## Transceiver Channels

The transceivers are positioned on the left and right outer edges of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

The following figures are graphical representations of a top view of the silicon die, which corresponds to a reverse view for flip chip packages. Different Arria V devices may have different floorplans than the ones shown in the figures.

Figure 9: Device Chip Overview for Arria V GX and GT Devices

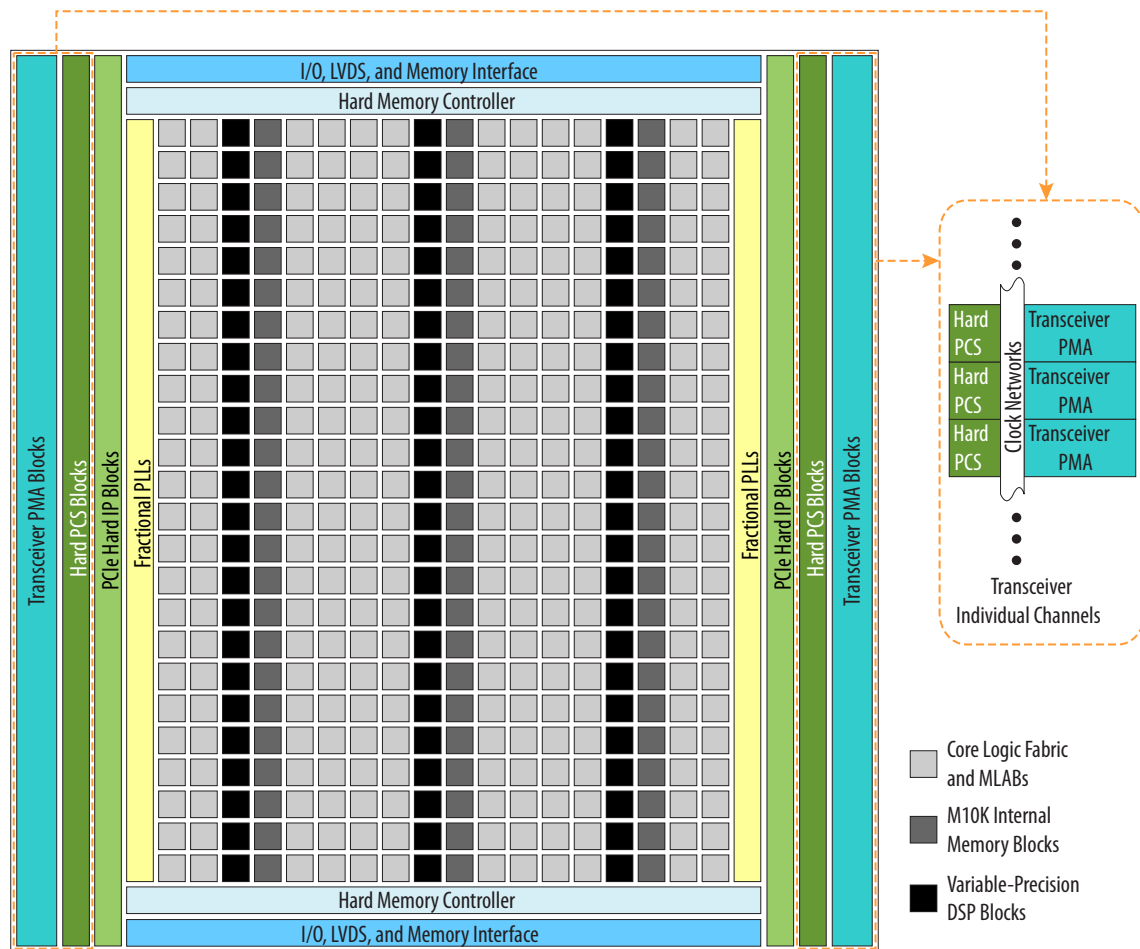


Figure 10: Device Chip Overview for Arria V GZ Devices

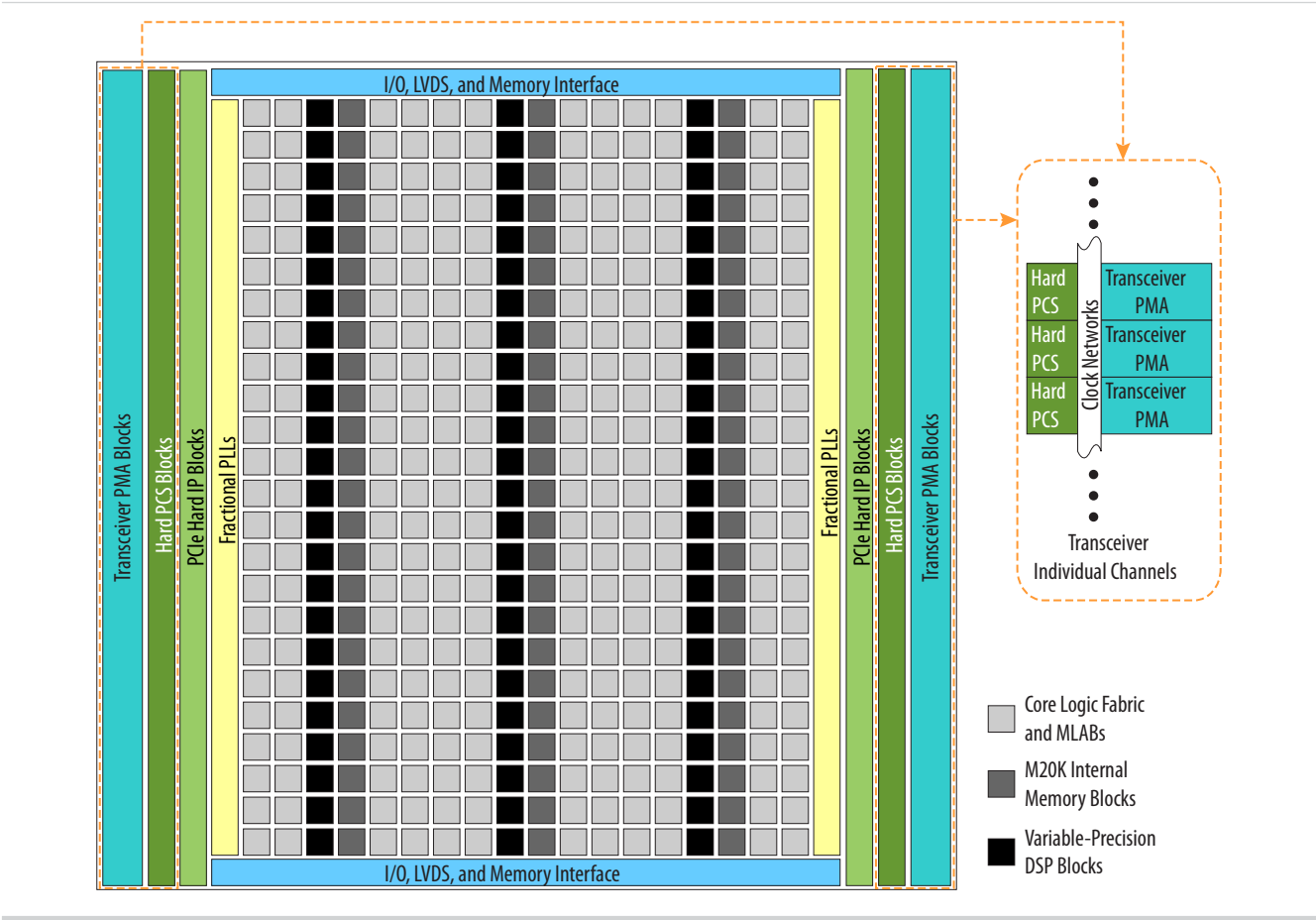


Table 22: Transceiver PCS Features for Arria V GZ Devices

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
Custom PHY	0.6 to 9.80	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>Bit-slip</li> <li>Channel bonding</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>Deskew FIFO</li> <li>Rate match FIFO</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Byte ordering</li> </ul>
GPON	1.25 and 2.5		
Custom 10G PHY	9.98 to 12.5	<ul style="list-style-type: none"> <li>TX FIFO</li> <li>Gear box</li> <li>Bit-slip</li> </ul>	<ul style="list-style-type: none"> <li>RX FIFO</li> <li>Gear box</li> </ul>
PCIe Gen1 (x1, x2, x4, x8)	2.5 and 5.0	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>Bit-slip</li> <li>Channel bonding</li> <li>PIPE 2.0 interface to core logic</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>Deskew FIFO</li> <li>Rate match FIFO</li> <li>8B/10B decoder</li> <li>Byte deserializer,</li> <li>Byte ordering</li> <li>PIPE 2.0 interface to core logic</li> </ul>
PCIe Gen2 (x1, x2, x4, x8)			
PCIe Gen3 (x1, x2, x4, x8)	8.0	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>128B/130B encoder</li> <li>Scrambler</li> <li>Gear box</li> <li>Bit-slip</li> </ul>	<ul style="list-style-type: none"> <li>Block synchronization</li> <li>Rate match FIFO</li> <li>128B/130B decoder</li> <li>Descrambler</li> <li>Phase compensation FIFO</li> </ul>
10GbE	10.3125	<ul style="list-style-type: none"> <li>TX FIFO</li> <li>64B/66B encoder</li> <li>Scrambler</li> <li>Gear box</li> </ul>	<ul style="list-style-type: none"> <li>RX FIFO</li> <li>64B/66B decoder</li> <li>Descrambler</li> <li>Block synchronization</li> <li>Gear box</li> </ul>
Interlaken	3.125 to 12.5	<ul style="list-style-type: none"> <li>TX FIFO</li> <li>Frame generator</li> <li>CRC-32 generator</li> <li>Scrambler</li> <li>Disparity generator</li> <li>Gear box</li> </ul>	<ul style="list-style-type: none"> <li>RX FIFO</li> <li>Frame generator</li> <li>CRC-32 checker</li> <li>Frame decoder</li> <li>Descrambler</li> <li>Disparity checker</li> <li>Block synchronization</li> <li>Gear box</li> </ul>

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
40GBASE-R Ethernet	4 x 10.3125	<ul style="list-style-type: none"> <li>TX FIFO</li> <li>64B/66B encoder</li> <li>Scrambler</li> <li>Alignment marker insertion</li> <li>Gearbox</li> <li>Block stripper</li> </ul>	<ul style="list-style-type: none"> <li>RX FIFO</li> <li>64B/66B decoder</li> <li>Descrambler</li> <li>Lane reorder</li> <li>Deskew</li> <li>Alignment marker lock</li> <li>Block synchronization</li> <li>Gear box</li> <li>Destripper</li> </ul>
100GBASE-R Ethernet	10 x 10.3125		
40G and 100G OTN	(4 +1) x 11.3	<ul style="list-style-type: none"> <li>TX FIFO</li> <li>Channel bonding</li> <li>Byte serializer</li> </ul>	<ul style="list-style-type: none"> <li>RX FIFO</li> <li>Lane deskew</li> <li>Byte deserializer</li> </ul>
	(10 +1) x 11.3		
GbE	1.25	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>Bit-slip</li> <li>Channel bonding</li> <li>GbE state machine</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>Deskew FIFO</li> <li>Rate match FIFO</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Byte ordering</li> <li>GbE state machine</li> </ul>
XAUI	3.125 to 4.25	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>Bit-slip</li> <li>Channel bonding</li> <li>XAUI state machine for bonding four channels</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>Deskew FIFO</li> <li>Rate match FIFO</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Byte ordering</li> <li>XAUI state machine for realigning four channels</li> </ul>
SRIO	1.25 to 6.25	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>Bit-slip</li> <li>Channel bonding</li> <li>SRIO V2.1-compliant x2 and x4 channel bonding</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>Deskew FIFO</li> <li>Rate match FIFO</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Byte ordering</li> <li>SRIO V2.1-compliant x2 and x4 deskew state machine</li> </ul>



## SoC with HPS

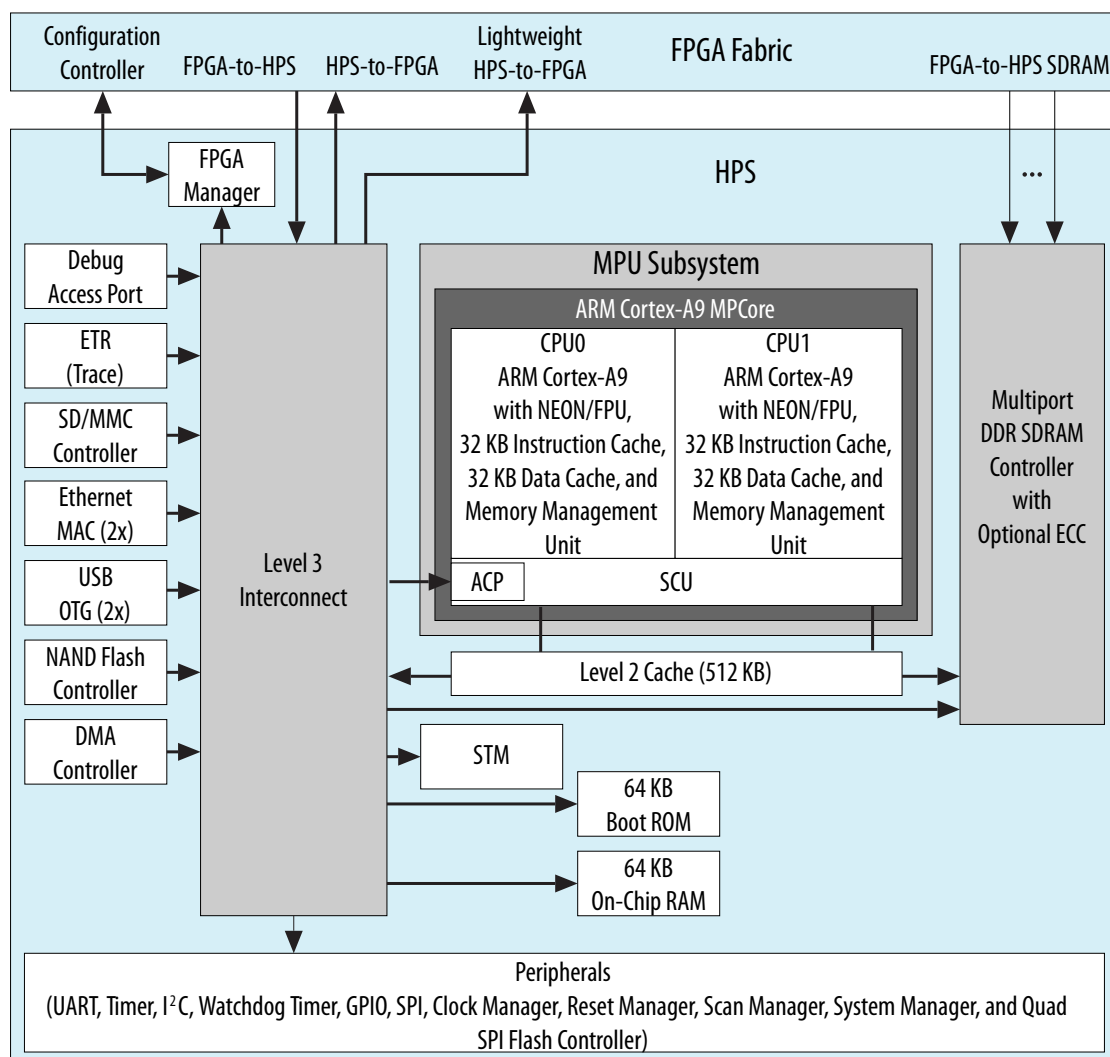
Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

## HPS Features

The HPS consists of a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

**Figure 12: HPS with Dual-Core ARM Cortex-A9 MPCore Processor**



## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

## HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 533 MHz (1066 Mbps data rate).

## FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

## Partial Reconfiguration

**Note:** Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Quartus Prime design software. With the Altera solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

## Enhanced Configuration and Configuration via Protocol

**Table 23: Configuration Modes and Features of Arria V Devices**

Arria V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V<sup>(19)</sup> programming voltages and several configuration modes.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration <sup>(20)</sup>	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—

<sup>(19)</sup> Arria V GZ does not support 3.3 V.

<sup>(20)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration <sup>(20)</sup>	Remote System Update
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes <sup>(21)</sup>	
	32 bits <sup>(22)</sup>	100	—	Yes	Yes	—	
CvP (PCIe)	x1, x2, x4, and x8 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—
Configuration via HPS	16 bits	125	—	Yes	Yes	Yes <sup>(21)</sup>	Parallel flash loader
	32 bits	100	—	Yes	Yes	—	

Instead of using an external flash or ROM, you can configure the Arria V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Arria V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

**Note:** Although Arria V GZ devices support PCIe Gen3, you can use only PCIe Gen1 and PCIe Gen2 for CvP configuration scheme.

#### Related Information

#### [Configuration via Protocol \(CvP\) Implementation in Altera FPGAs User Guide](#)

Provides more information about CvP.

## Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Arria V devices consume less power than previous generation Arria V FPGAs:

- Total device core power consumption—less by up to 50%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Arria V devices contain several hard IP blocks, including PCIe Gen1, Gen2, and Gen3, GbE, SRIO, GPON, and CPRI protocols, that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

<sup>(20)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

<sup>(21)</sup> Supported at a maximum clock rate of 62.5 MHz.

<sup>(22)</sup> Arria V GZ only

Date	Version	Changes
July 2012	2.1	<ul style="list-style-type: none"> <li>Added –I3 speed grade to Figure 1 for Arria V GX devices.</li> <li>Updated the 6-Gbps transceiver speed from 6.553 Gbps to 6.5536 Gbps in Figure 3 and Figure 1.</li> </ul>
June 2012	2.0	<ul style="list-style-type: none"> <li>Restructured the document.</li> <li>Added the “Embedded Memory Capacity” and “Embedded Memory Configurations” sections.</li> <li>Added Table 1, Table 3, Table 12, Table 15, and Table 16.</li> <li>Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 13, Table 14, and Table 19.</li> <li>Updated Figure 1, Figure 2, Figure 3, Figure 4, and Figure 8.</li> <li>Updated the “FPGA Configuration and Processor Booting” and “Hardware and Software Development” sections.</li> <li>Text edits throughout the document.</li> </ul>
February 2012	1.3	<ul style="list-style-type: none"> <li>Updated Table 1–7 and Table 1–8.</li> <li>Updated Figure 1–9 and Figure 1–10.</li> <li>Minor text edits.</li> </ul>
December 2011	1.2	Minor text edits.
November 2011	1.1	<ul style="list-style-type: none"> <li>Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–6, Table 1–7, Table 1–9, and Table 1–10.</li> <li>Added “SoC FPGA with HPS” section.</li> <li>Updated “Clock Networks and PLL Clock Sources” and “Ordering Information” sections.</li> <li>Updated Figure 1–5.</li> <li>Added Figure 1–6.</li> <li>Minor text edits.</li> </ul>
August 2011	1.0	Initial release.