Intel - 5ASXBB5D4F35I5N Datasheet





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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

Details

Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore [™] with CoreSight [™]
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 462K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA, FC (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5asxbb5d4f35i5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Feature		Description			
	Variable-precision DSP Memory controller (Arria V GX, GT, SX, and ST only)	 Native support for up to four signal processing precision levels: Three 9 x 9, two 18 x 18, or one 27 x 27 multiplier in the same variable-precision DSP block One 36 x 36 multiplier using two variable-precision DSP blocks (Arria V GZ devices only) 64-bit accumulator and cascade for systolic finite impulse responses (FIRs) Embedded internal coefficient memory Preadder/subtractor for improved efficiency 			
Embedded Hard IP blocks	Embedded transceiver I/O	 Custom implementation: Arria V GX and SX devices—up to 6.5536 Gbps Arria V GT and ST devices—up to 10.3125 Gbps Arria V GZ devices—up to 12.5 Gbps PCI Express[®] (PCIe[®]) Gen2 (x1, x2, or x4) and Gen1 (x1, x2, x4, or x8) hard IP with multifunction support, endpoint, and root port PCIe Gen3 (x1, x2, x4, or x8) support (Arria V GZ only) Gbps Ethernet (GbE) and XAUI physical coding sublayer (PCS) Common Public Radio Interface (CPRI) PCS Gigabit-capable passive optical network (GPON) PCS 10-Gbps Ethernet (10GbE) PCS (Arria V GZ only) Serial RapidIO[®] (SRIO) PCS Interlaken PCS (Arria V GZ only) 			
Clock networks	 Up to 650 MHz glo Global, quadrant, a Clock networks that 	Up to 650 MHz global clock network Global, quadrant, and peripheral clock networks Clock networks that are not used can be powered down to reduce dynamic power			
Phase-locked loops (PLLs)	 High-resolution fractional PLLs Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) Integer mode and fractional mode LC oscillator ATX transmitter PLLs (Arria V GZ only) 				



Feature	Description
Configuration	 Tamper protection-comprehensive design protection to protect your valuable IP investments Enhanced advanced encryption standard (AES) design security features CvP Partial and dynamic reconfiguration of the FPGA Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8, x16, and x32 (Arria V GZ) configuration options Remote system upgrade

Arria V Device Variants and Packages

Table 3: Device Variants for the Arria V Device Family

Variant	Description
Arria V GX	FPGA with integrated 6.5536 Gbps transceivers that provides bandwidth, cost, and power levels that are optimized for high-volume data and signal-processing applications
Arria V GT	FPGA with integrated 10.3125 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for cost-sensitive data and signal processing applications
Arria V GZ	FPGA with integrated 12.5 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for high-performance and cost-sensitive data and signal processing applications
Arria V SX	SoC with integrated ARM-based HPS and 6.5536 Gbps transceivers
Arria V ST	SoC with integrated ARM-based HPS and 10.3125 Gbps transceivers

Arria V GX

This section provides the available options, maximum resource counts, and package plan for the Arria V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector

Provides the latest information about Altera products.



Available Options

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

Posourco		Member Code							
neso	urce	A1	A3	A5	A7	B1	B3	B5	Β7
Logic I (LE) (I	Elements K)	75	156	190	242	300	362	420	504
ALM		28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240
Registe	er	113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960
Mem	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
ory (Kb)	MLAB	463	961	1,173	1,448	1,852	2,098	2,532	2,906
Variab precisi Block	le- on DSP	240	396	600	800	920	1,045	1,092	1,156
18 x 18 Multip	3 llier	480	792	1,200	1,600	1,840	2,090	2,184	2,312
PLL		10	10	12	12	12	12	16	16

Arria V Device Overview



Available Options

8

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector

Provides the latest information about Altera products.

Available Options

Figure 2: Sample Ordering Code and Available Options for Arria V GT Devices



Maximum Resources

Table 6: Maximum Resource Counts for Arria V GT Devices

Pecourco		Member Code				
nest		C3	С7	D3	D7	
Logic Elemer	nts (LE) (K)	156	242	362	504	
ALM		58,900	91,680	136,880	190,240	
Register	Register		366,720	547,520	760,960	
Memory	M10K	10,510	13,660	17,260	24,140	
(Kb)	MLAB	961	1,448	2,098	2,906	
Variable-precision DSP Block		396	800	1,045	1,156	
18 x 18 Multiplier		792	1,600	2,090	2,312	
PLL		10	12	12	16	

Arria V Device Overview



Resource		Member Code					
Nesc		E1	E3	E5	E7		
Memory	M20K	11,700	19,140	28,800	34,000		
(Kb)	MLAB	2,594	4,245	4,718	5,306		
Variable-prec	Variable-precision DSP Block		1,044	1,092	1,139		
18 x 18 Multiplier		1,600	2,088	2,184	2,278		
PLL		20	20	24	24		
12.5 Gbps Tra	ansceiver	24	24	36	36		
GPIO ⁽⁷⁾	GPIO ⁽⁷⁾		414	674	674		
LVDS	Transmitter	99	99	166	166		
LVDS	Receiver	108	108	168	168		
PCIe Hard IP	Block	1	1	1	1		

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook

Provides the number of LVDS channels in each device package.

Package Plan

Table 9: Package Plan for Arria V GZ Devices

Member Code	H780 (33 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
E1	342	12	414	24	_	—
E3	342	12	414	24	_	_
E5			534	24	674	36
E7			534	24	674	36

Arria V SX

This section provides the available options, maximum resource counts, and package plan for the Arria V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Arria V Device Overview



⁽⁷⁾ The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

12 Available Options

Related Information

Altera Product Selector

Provides the latest information about Altera products.

Available Options

Figure 4: Sample Ordering Code and Available Options for Arria V SX Devices

The –3 FPGA fabric speed grade is available only for industrial temperature devices.



Maximum Resources

Table 10: Maximum Resource Counts for Arria V SX Devices

Poso		Member Code			
nesu	uice	B3	B5		
Logic Elements (LE)	(K)	350	462		
ALM		132,075	174,340		
Register		528,300	697,360		
Memory (Kb)	M10K	17,290	22,820		
Welliory (RD)	MLAB	2,014	2,658		
Variable-precision D	SP Block	809	1,090		
18 x 18 Multiplier		1,618	2,180		

Arria V Device Overview



Related Information

Altera Product Selector

Provides the latest information about Altera products.

Available Options

Figure 5: Sample Ordering Code and Available Options for Arria V ST Devices



Maximum Resources

Table 12: Maximum Resource Counts for Arria V ST Devices

Decouver		Member Code			
Reso	ource	D3	D5		
Logic Elements (LE)	(K)	350	462		
ALM		132,075	174,340		
Register		528,300	697,360		
Momory (Kb)	M10K	17,290	22,820		
Memory (RD)	MLAB	2,014	2,658		
Variable-precision D	SP Block	809	1,090		
18 x 18 Multiplier		1,618	2,180		
FPGA PLL	FPGA PLL		14		
HPS PLL		3	3		
Transceiver	6-Gbps	30	30		
114115001701	10-Gbps ⁽⁹⁾	16	16		

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Arria V Device Overview



I/O Vertical Migration for Arria V Devices

Figure 6: Vertical Migration Capability Across Arria V Device Packages and Densities

The arrows indicate the vertical migration paths. Some packages have several migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.

Mariant	Member	Package					
variant	Code	F6	72	F780	F896	F 1152	F1517
	A1						
	A3						
	A5					1	
Arria V CY	A7	•					
	B1						1
	B3						
	B5						
	B7						
	C3				•		
Arria V GT	С7						
	D3						
	D7					•	•
	E1					•	
Arria V G7	E3			•			
	E5						•
	E7					•	
Arria V SX	B3					•	
	B5						
Arria V ST	D3						
	D5				•	•	•

You can achieve the vertical migration shaded in red if you use only up to 320 GPIOs, up to nine 6 Gbps transceiver channels, and up to four 10 Gbps transceiver (for Arria V GT devices). This migration path is not shown in the Quartus Prime software Pin Migration View.

- **Note:** To verify the pin migration compatibility, use the Pin Migration View window in the Quartus Prime software Pin Planner.
- **Note:** Except for Arria V GX A5 and A7, and Arria V GT C7 devices, all other Arria V GX and GT devices require a specific power-up sequence. If you plan to migrate your design from Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices, your design must adhere to the same required power-up sequence.

Arria V Device Overview



Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- Double accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus Prime design software

Table 14: Variable-Precision DSP Block Configurations for Arria V Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters	Two 18 x 18 with accumulate	1
Single-precision floating- point implementations	One 27 x 27	1
Very high precision fixed point implementations	One 36 x 36	2

You can configure each DSP block during compilation as independent three $9 \ge 9$, two $18 \ge 18$, or one 27 ≥ 27 multipliers. Using two DSP block resources, you can also configure a $36 \ge 36$ multiplier for high-precision applications. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Arria V Device Overview



External Memory Performance

Intorfaco	Voltage	Hard Controller (MHz)	Soft Controller (MHz)		
interface	(V)	Arria V GX, GT, SX, and ST	Arria V GX, GT, SX, and ST	Arria V GZ	
	1.5	533	667	800	
DDR5 5DRAM	1.35	533	600	800	
DDR2 SDRAM	1.8	400	400	400	
LPDDR2 SDRAM	1.2	_	400	_	
RLDRAM 3	1.2	—	_	667	
	1.8		400	533	
	1.5	_	400	533	
QDR II+ SRAM	1.8	—	400	500	
	1.5	_	400	500	
QDR II SRAM	1.8	—	400	333	
	1.5	—	400	333	
DDR II+	1.8		400		
SRAM ⁽¹²⁾	1.5		400	_	

Table 18: External Memory Interface Performance in Arria V Devices

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 19: HPS External Memory Interface Performance

The hard processor system (HPS) is available in Arria V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
	1.5	533
DDRJ SDRAM	1.35	533
LPDDR2 SDRAM	1.2	333

Arria V Device Overview



⁽¹²⁾ Not available as Altera[®] IP.



Figure 11: Device Chip Overview for Arria V SX and ST Devices

PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 20: PMA Features of the Transceivers in Arria V Devices

Features	Capability
Backplane support	 Arria V GX, GT, SX, and ST devices—Driving capability at 6.5536 Gbps with up to 25 dB channel loss Arria V GZ devices—Driving capability at 12.5 Gbps with up to 16 dB channel loss
Chip-to-chip support	 Arria V GX, GT, SX, and ST devices—Up to 10.3125 Gbps Arria V GZ devices—Up to 12.5 Gbps

Arria V Device Overview



Features	Capability
PLL-based clock recovery	Superior jitter tolerance
Programmable serializer and deserializer (SERDES)	Flexible SERDES width
Equalization and pre-emphasis	 Arria V GX, GT, SX, and ST devices—Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization Arria V GZ devices—4-tap pre-emphasis and de-emphasis
Ring oscillator transmit PLLs	611 Mbps to 10.3125 Gbps
LC oscillator ATX transmit PLLs (Arria V GZ devices only)	600 Mbps to 12.5 Gbps
Input reference clock range	27 MHz to 710 MHz
Transceiver dynamic reconfigu- ration	Allows the reconfiguration of a single channel without affecting the operation of other channels

PCS Features

The Arria V core logic connects to the PCS through an 8, 10, 16, 20, 32, 40, 64, 66, or 67 bit interface, depending on the transceiver data rate and protocol. Arria V devices contain PCS hard IP to support PCIe Gen1, Gen2, and Gen3, GbE, Serial RapidIO (SRIO), GPON, and CPRI.

All other standard and proprietary protocols within the following speed ranges are also supported:

- 611 Mbps to 6.5536 Gbps—supported through the custom double-width mode (up to 6.5536 Gbps) and custom single-width mode (up to 3.75 Gbps) of the transceiver PCS hard IP.
- 6.5536 Gbps to 10.3125 Gbps—supported through dedicated 80 or 64 bit interface that bypass the PCS hard IP and connects the PMA directly to the core logic. In Arria V GZ, this is supported in the transceiver PCS hard IP.

Table 21: Transceiver PCS Features for Arria V GX, GT, ST, and SX Devices

PCS Support ⁽¹³⁾	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Custom single- and double-width modes	0.611 to ~6.5536	Phase compensation FIFO	Word aligner8B/10B decoder
SRIO	1.25 to 6.25	 Byte serializer 8B/10B encoder 	• Byte deserializer
Serial ATA	1.5, 3.0, 6.0		Phase compensation FIFO

Arria V Device Overview

Altera Corporation



⁽¹³⁾ Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

PCS Features

PCS Support ⁽¹³⁾	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
PCIe Gen1 (x1, x2, x4, x8) PCIe Gen2 ⁽¹⁴⁾ (x1, x2, x4)	2.5 and 5.0	 Phase compensation FIFO Byte serializer 8B/10B encoder PIPE 2.0 interface to the core logic 	 Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO Rate match FIFO PIPE 2.0 interface to the core logic
GbE	1.25	 Phase compensation FIFO Byte serializer 8B/10B encoder 	 Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO Rate match FIFO
XAUI ⁽¹⁵⁾	3.125	 Phase compensation FIFO Byte serializer 8B/10B encoder XAUI state machine for bonding four channels 	 Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO XAUI state machine for realigning four channels Deskew FIFO circuitry
SDI	0.27 ⁽¹⁶⁾ , 1.485, 2.97	 Phase compensation FIFO Byte serializer 	 Byte deserializer Phase compensation FIFO
GPON ⁽¹⁷⁾	1.25 and 2.5		
CPRI ⁽¹⁸⁾	0.6144 to 6.144	 Phase compensation FIFO Byte serializer 8B/10B encoder TX deterministic latency 	 Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO RX deterministic latency

Arria V Device Overview



⁽¹³⁾ Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

⁽¹⁴⁾ PCIe Gen2 is supported only through the PCIe hard IP.

⁽¹⁵⁾ XAUI is supported through the soft PCS.

⁽¹⁶⁾ The 0.27 Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

⁽¹⁷⁾ The GPON standard does not support burst mode.

⁽¹⁸⁾ CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through the soft PCS.

PCS Features

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
40GBASE-R Ethernet 100GBASE-R Ethernet	4 x 10.3125 10 x 10.3125	 TX FIFO 64B/66B encoder Scrambler Alignment marker insertion Gearbox Block stripper 	 RX FIFO 64B/66B decoder Descrambler Lane reorder Deskew Alignment marker lock Block synchronization Gear box Destripper
40G and 100G OTN	(4 +1) x 11.3 (10 +1) x 11.3	TX FIFOChannel bondingByte serializer	 RX FIFO Lane deskew Byte deserializer
GbE	1.25	 Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding GbE state machine 	 Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer Byte ordering GbE state machine
XAUI	3.125 to 4.25	 Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding XAUI state machine for bonding four channels 	 Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer Byte ordering XAUI state machine for realigning four channels
SRIO	1.25 to 6.25	 Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding SRIO V2.1-compliant x2 and x4 channel bonding 	 Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer Byte ordering SRIO V2.1-compliant x2 and x4 deskew state machine

Arria V Device Overview



SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

HPS Features

The HPS consists of a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

Figure 12: HPS with Dual-Core ARM Cortex-A9 MPCore Processor



Arria V Device Overview



You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Note: Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

Related Information

• Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides detailed information about power supply pin connection guidelines and power regulator sharing.

• Arria V GZ Device Family Pin Connection Guidelines Provides detailed information about power supply pin connection guidelines and power regulator sharing.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Qsys system integration tool in the Quartus Prime software.

For software development, the ARM-based SoC devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Altera SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks[®], and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Altera sales team.

You can begin device-specific firmware and software development on the Altera SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Related Information

Altera Worldwide Sales Support

Dynamic and Partial Reconfiguration

The Arria V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA, PCS, and PCIe hard IP blocks with dynamic reconfiguration.

Arria V Device Overview

Altera Corporation



Partial Reconfiguration

Note: Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Quartus Prime design software. With the Altera solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Table 23: Configuration Modes and Features of Arria V Devices

	, .			1 0	0		0
Mode	Data Width	Max Clock Rate (MHz)	Max Data[Rate (Mbps)	Decompressio	Design Security R	Partial econfiguratio (20)	Remote System Update
AS through the EPCS and EPCQ serial configura- tion device	1 bit, 4 bits	100		Yes	Yes		Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	_	_

Arria V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V⁽¹⁹⁾ programming voltages and several configuration modes.

Arria V Device Overview



⁽¹⁹⁾ Arria V GZ does not support 3.3 V.

⁽²⁰⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Altera Corporation

Mode	Data Width	Max Clock Rate (MHz)	Max DataI Rate (Mbps)	Decompressio	Design Security F	Partial econfiguratio (20)	Remote System Update
	8 bits	125	-	Yes	Yes	_	
FPP	16 bits	125	_	Yes	Yes	Yes ⁽²¹⁾	Parallel flash loader
	32 bits ⁽²²⁾	100	_	Yes	Yes		
CvP (PCIe)	x1, x2, x4, and x8 lanes		_	Yes	Yes	Yes	_
JTAG	1 bit	33	33	_	_	_	
Configuration	16 bits	125	_	Yes	Yes	Yes (21)	Darallel flash loader
via HPS	32 bits	100	—	Yes	Yes		

Instead of using an external flash or ROM, you can configure the Arria V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Arria V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

Note: Although Arria V GZ devices support PCIe Gen3, you can use only PCIe Gen1 and PCIe Gen2 for CvP configuration scheme.

Related Information

Configuration via Protocol (CvP) Implementation in Altera FPGAs User Guide Provides more information about CvP.

Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Arria V devices consume less power than previous generation Arria V FPGAs:

- Total device core power consumption—less by up to 50%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Arria V devices contain several hard IP blocks, including PCIe Gen1, Gen2, and Gen3, GbE, SRIO, GPON, and CPRI protocols, that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

Arria V Device Overview

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⁽²⁰⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

⁽²¹⁾ Supported at a maximum clock rate of 62.5 MHz.

⁽²²⁾ Arria V GZ only

Document Revision History

Date	Version	Changes
December 2015	2015.12.21	 Updated RoHS and optional suffix information in sample ordering code and available options diagrams for Arria V GX and GT devices. Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.
January 2015	2015.01.23	 Updated package dimension for Arria V GZ H780 package from 29 mm to 33 mm. Updated dual-core ARM Cortex-A9 MPCore processor maximum frequency from 800 MHz to 1.05 GHz.
December 2013	2013.12.26	 10-Gbps Ethernet (10GbE) PCS and Interlaken PCS are for Arria V GZ only. Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. Added link to Altera Product Selector for each device variant. Added leaded package options. Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F896 package from 170 to 250. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1512 package from 350 to 385. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1517 package from 528 to 540. Corrected LVDS Transmitter for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 devices from 121 to 120. Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance. Added x2 for PCIe Gen3, Gen 2, and Gen 1.
August 2013	2013.08.19	 Removed the note about the PCIe hard IP on the right side of the device in the F896 package of the Arria V GX variant. These devices do not have PCIe hard IP on the right side. Added transceiver speed grade 6 to the available options of the Arria V SX variant. Corrected the maximum LVDS transmitter channel counts for the Arria V GX A1 and A3 devices from 68 to 67. Corrected the maximum FPGA GPIO count for Arria V ST D5 devices from 540 to 528.

Arria V Device Overview



Date	Version	Changes
July 2012	2.1	 Added –13 speed grade to Figure 1 for Arria V GX devices. Updated the 6-Gbps transceiver speed from 6.553 Gbps to 6.5536 Gbps in Figure 3 and Figure 1.
June 2012	2.0	 Restructured the document. Added the "Embedded Memory Capacity" and "Embedded Memory Configurations" sections. Added Table 1, Table 3, Table 12, Table 15, and Table 16. Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 13, Table 14, and Table 19. Updated Figure 1, Figure 2, Figure 3, Figure 4, and Figure 8. Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections. Text edits throughout the document.
February 2012	1.3	 Updated Table 1–7 and Table 1–8. Updated Figure 1–9 and Figure 1–10. Minor text edits.
December 2011	1.2	Minor text edits.
November 2011	1.1	 Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–6, Table 1–7, Table 1–9, and Table 1–10. Added "SoC FPGA with HPS" section. Updated "Clock Networks and PLL Clock Sources" and "Ordering Information" sections. Updated Figure 1–5. Added Figure 1–6. Minor text edits.
August 2011	1.0	Initial release.

