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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

[Embedded - System On Chip \(SoC\)](#) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are [Embedded - System On Chip \(SoC\)](#)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

Details

Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	700MHz
Primary Attributes	FPGA - 462K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA, FC (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5asxb5d6f31c6n

Advantage	Supporting Feature
Lowest system cost	<ul style="list-style-type: none"> Requires as few as four power supplies to operate Available in thermal composite flip chip ball-grid array (BGA) packaging Includes innovative features such as Configuration via Protocol (CvP), partial reconfiguration, and design security

Summary of Arria V Features

Table 2: Summary of Features for Arria V Devices

Feature	Description
Technology	<ul style="list-style-type: none"> TSMC's 28-nm process technology: <ul style="list-style-type: none"> Arria V GX, GT, SX, and ST—28-nm low power (28LP) process Arria V GZ—28-nm high performance (28HP) process Lowest static power in its class (less than 1.2 W for 500K logic elements (LEs) at 85°C junction under typical conditions) 0.85 V, 1.1 V, or 1.15 V core nominal voltage
Packaging	<ul style="list-style-type: none"> Thermal composite flip chip BGA packaging Multiple device densities with identical package footprints for seamless migration between different device densities Leaded⁽¹⁾, lead-free (Pb-free), and RoHS-compliant options
High-performance FPGA fabric	<ul style="list-style-type: none"> Enhanced 8-input ALM with four registers Improved routing architecture to reduce congestion and improve compilation time
Internal memory blocks	<ul style="list-style-type: none"> M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) (Arria V GX, GT, SX, and ST devices only) M20K—20-Kb memory blocks with hard ECC (Arria V GZ devices only) Memory logic array block (MLAB)-640-bit distributed LUTRAM where you can use up to 50% of the ALMs as MLAB memory

⁽¹⁾ Contact Altera for availability.

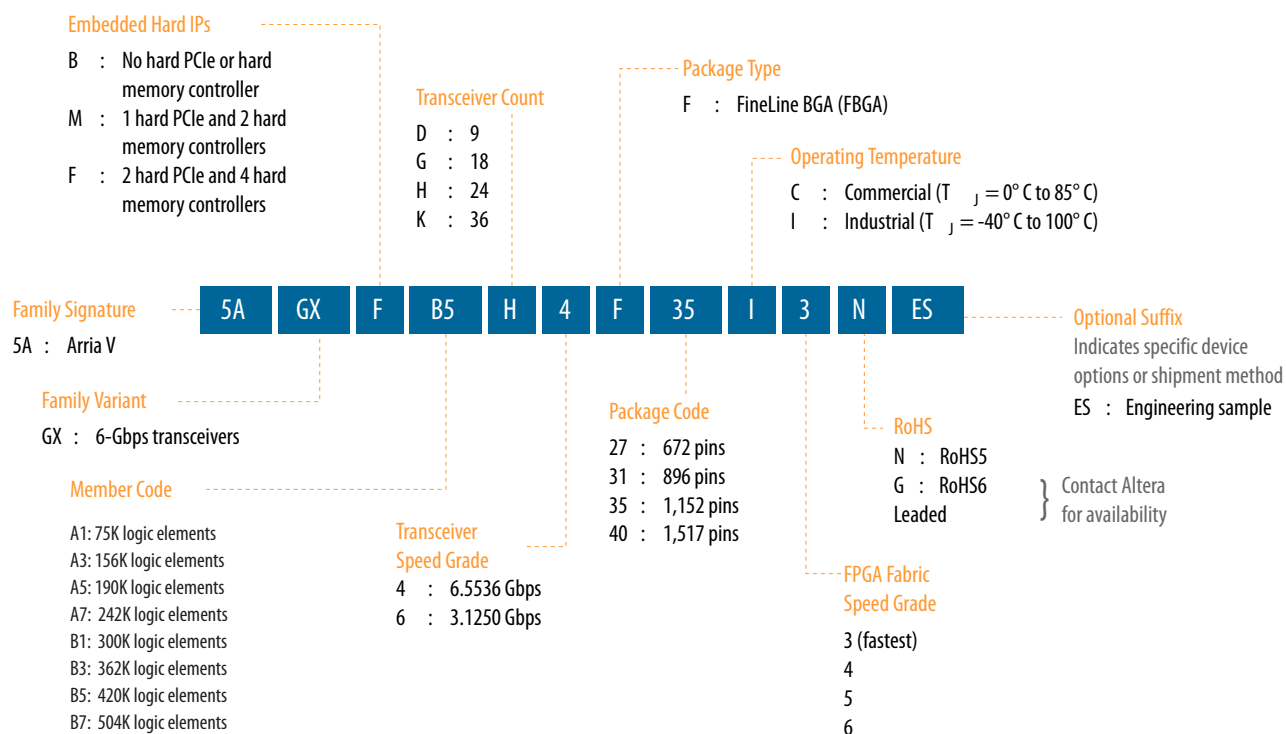
Feature	Description
FPGA General-purpose I/Os (GPIOs)	<ul style="list-style-type: none"> 1.6 Gbps LVDS receiver and transmitter 800 MHz/1.6 Gbps external memory interface On-chip termination (OCT) 3.3 V support ⁽²⁾
External Memory Interface	<p>Memory interfaces with low latency:</p> <ul style="list-style-type: none"> Hard memory controller-up to 1.066 Gbps Soft memory controller-up to 1.6 Gbps
Low-power high-speed serial interface	<ul style="list-style-type: none"> 600 Mbps to 12.5 Gbps integrated transceiver speed Less than 105 mW per channel at 6 Gbps, less than 165 mW per channel at 10 Gbps, and less than 170 mW per channel at 12.5 Gbps Transmit pre-emphasis and receiver equalization Dynamic partial reconfiguration of individual channels Physical medium attachment (PMA) with soft PCS that supports 9.8304 Gbps CPRI (Arria V GT and ST only) PMA with hard PCS that supports up to 9.8 Gbps CPRI (Arria V GZ only) Hard PCS that supports 10GBASE-R and 10GBASE-KR (Arria V GZ only)
HPS (Arria V SX and ST devices only)	<ul style="list-style-type: none"> Dual-core ARM Cortex-A9 MPCore processor—up to 1.05 GHz maximum frequency with support for symmetric and asymmetric multiprocessing Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, serial peripheral interface (SPI), I2C interface, and up to 85 HPS GPIO interfaces System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers On-chip RAM and boot ROM HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller ARM CoreSight™ JTAG debug access port, trace port, and on-chip trace storage

⁽²⁾ Arria V GZ devices support 3.3 V with a 3.0 V V_{CCIO}.



Available Options

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
Logic Elements (LE) (K)		75	156	190	242	300	362	420	504
ALM		28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240
Register		113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960
Mem ory (Kb)	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
	MLAB	463	961	1,173	1,448	1,852	2,098	2,532	2,906
Variable-precision DSP Block		240	396	600	800	920	1,045	1,092	1,156
18 x 18 Multiplier		480	792	1,200	1,600	1,840	2,090	2,184	2,312
PLL		10	10	12	12	12	12	16	16

and eighteen 10-Gbps, twelve 6-Gbps and sixteen 10-Gbps, fifteen 6-Gbps and fourteen 10-Gbps, or up to thirty-six 6-Gbps with no 10-Gbps channels.

Arria V GZ

This section provides the available options, maximum resource counts, and package plan for the Arria V GZ devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

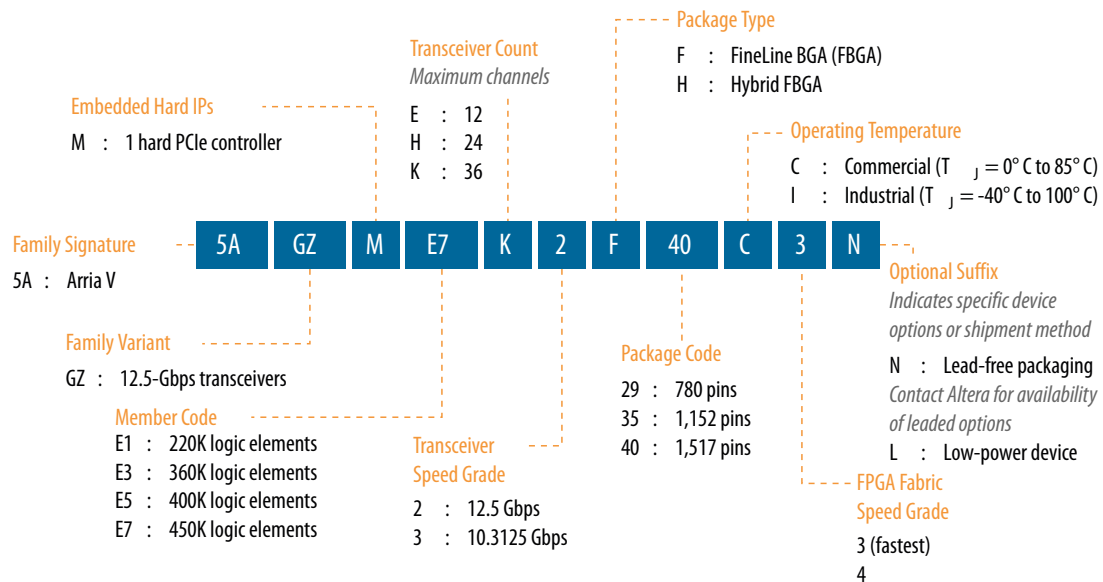
Related Information

Altera Product Selector

Provides the latest information about Altera products.

Available Options

Figure 3: Sample Ordering Code and Available Options for Arria V GZ Devices



Maximum Resources

Table 8: Maximum Resource Counts for Arria V GZ Devices

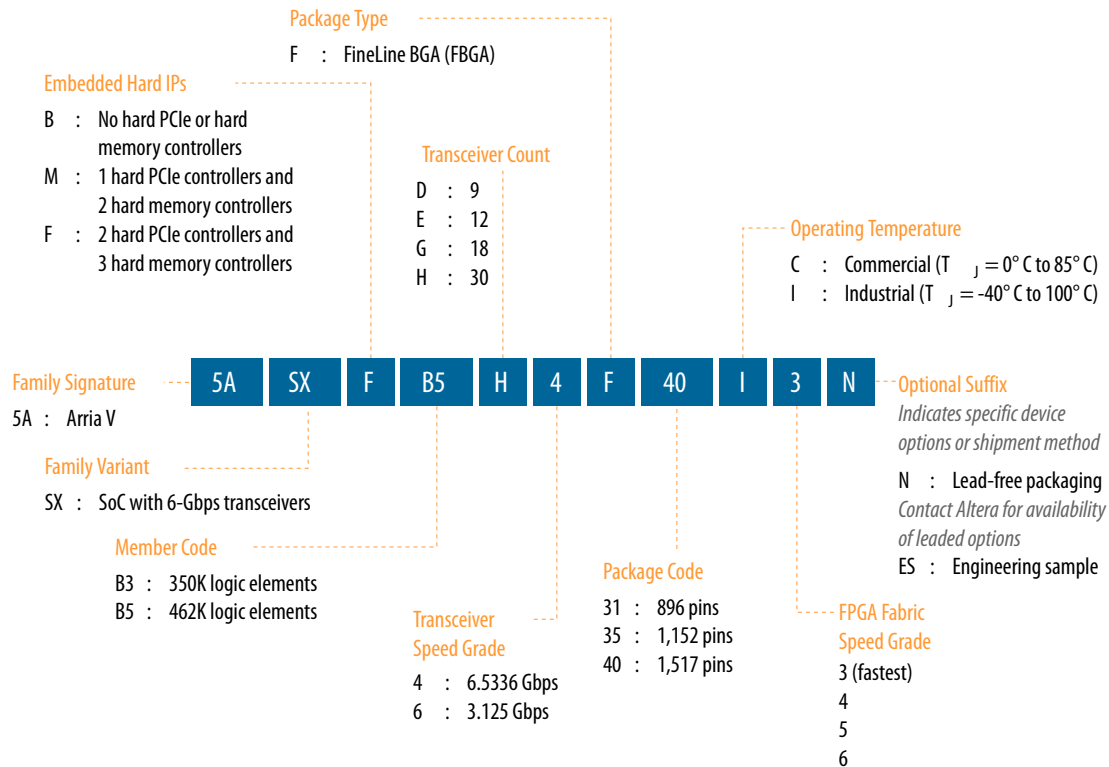
Resource	Member Code			
	E1	E3	E5	E7
Logic Elements (LE) (K)	220	360	400	450
ALM	83,020	135,840	150,960	169,800
Register	332,080	543,360	603,840	679,200

Related Information**Altera Product Selector**

Provides the latest information about Altera products.

Available Options**Figure 4: Sample Ordering Code and Available Options for Arria V SX Devices**

The –3 FPGA fabric speed grade is available only for industrial temperature devices.

**Maximum Resources****Table 10: Maximum Resource Counts for Arria V SX Devices**

Resource		Member Code	
		B3	B5
Logic Elements (LE) (K)		350	462
ALM		132,075	174,340
Register		528,300	697,360
Memory (Kb)	M10K	17,290	22,820
	MLAB	2,014	2,658
Variable-precision DSP Block		809	1,090
18 x 18 Multiplier		1,618	2,180

I/O Vertical Migration for Arria V Devices

Figure 6: Vertical Migration Capability Across Arria V Device Packages and Densities

The arrows indicate the vertical migration paths. Some packages have several migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.

Variant	Member Code	Package				
		F672	F780	F896	F 1152	F1517
Arria V GX	A1					
	A3					
	A5					
	A7					
	B1					
	B3					
	B5					
	B7					
Arria V GT	C3					
	C7					
	D3					
	D7					
Arria V GZ	E1					
	E3					
	E5					
	E7					
Arria V SX	B3					
	B5					
Arria V ST	D3					
	D5					

You can achieve the vertical migration shaded in red if you use only up to 320 GPIOs, up to nine 6 Gbps transceiver channels, and up to four 10 Gbps transceiver (for Arria V GT devices). This migration path is not shown in the Quartus Prime software Pin Migration View.

Note: To verify the pin migration compatibility, use the Pin Migration View window in the Quartus Prime software Pin Planner.

Note: Except for Arria V GX A5 and A7, and Arria V GT C7 devices, all other Arria V GX and GT devices require a specific power-up sequence. If you plan to migrate your design from Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices, your design must adhere to the same required power-up sequence.

Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- Double accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus Prime design software

Table 14: Variable-Precision DSP Block Configurations for Arria V Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters	Two 18 x 18 with accumulate	1
Single-precision floating-point implementations	One 27 x 27	1
Very high precision fixed point implementations	One 36 x 36	2

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. Using two DSP block resources, you can also configure a 36 x 36 multiplier for high-precision applications. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Table 15: Number of Multipliers in Arria V Devices

The table lists the variable-precision DSP resources by bit precision for each Arria V device.

Variant	Member Code	Variable-precision DSP Block	Independent Input and Output Multiplications Operator				18 x 18 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier	36 x 36 Multiplier		
Arria V GX	A1	240	720	480	240	—	240	240
	A3	396	1,188	792	396	—	396	396
	A5	600	1,800	1,200	600	—	600	600
	A7	800	2,400	1,600	800	—	800	800
	B1	920	2,760	1,840	920	—	920	920
	B3	1,045	3,135	2,090	1,045	—	1,045	1,045
	B5	1,092	3,276	2,184	1,092	—	1,092	1,092
	B7	1,156	3,468	2,312	1,156	—	1,156	1,156
Arria V GT	C3	396	1,188	792	396	—	396	396
	C7	800	2,400	1,600	800	—	800	800
	D3	1,045	3,135	2,090	1,045	—	1,045	1,045
	D7	1,156	3,468	2,312	1,156	—	1,156	1,156
Arria V GZ	E1	800	2,400	1,600	800	400	800	800
	E3	1,044	3,132	2,088	1,044	522	1,044	1,044
	E5	1,092	3,276	2,184	1,092	546	1,092	1,092
	E7	1,139	3,417	2,278	1,139	569	1,139	1,139
Arria V SX	B3	809	2,427	1,618	809	—	809	809
	B5	1,090	3,270	2,180	1,090	—	1,090	1,090
Arria V ST	D3	809	2,427	1,618	809	—	809	809
	D5	1,090	3,270	2,180	1,090	—	1,090	1,090

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

Types of Embedded Memory

The Arria V devices contain two types of memory blocks:

- 20 Kb M20K or 10 Kb M10K blocks—blocks of dedicated memory resources. The M20K and M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Arria V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB. You can also configure these ALMs, in Arria V GZ devices, as ten 64 x 1 blocks, giving you one 64 x 10 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Arria V Devices

Table 16: Embedded Memory Capacity and Distribution in Arria V Devices

Variant	Member Code	M20K		M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Arria V GX	A1	—	—	800	8,000	741	463	8,463
	A3	—	—	1,051	10,510	1538	961	11,471
	A5	—	—	1,180	11,800	1877	1,173	12,973
	A7	—	—	1,366	13,660	2317	1,448	15,108
	B1	—	—	1,510	15,100	2964	1,852	16,952
	B3	—	—	1,726	17,260	3357	2,098	19,358
	B5	—	—	2,054	20,540	4052	2,532	23,072
	B7	—	—	2,414	24,140	4650	2,906	27,046
Arria V GT	C3	—	—	1,051	10,510	1538	961	11,471
	C7	—	—	1,366	13,660	2317	1,448	15,108
	D3	—	—	1,726	17,260	3357	2,098	19,358
	D7	—	—	2,414	24,140	4650	2,906	27,046
Arria V GZ	E1	585	11,700	—	—	4,151	2,594	14,294
	E3	957	19,140	—	—	6,792	4,245	23,385
	E5	1,440	28,800	—	—	7,548	4,718	33,518
	E7	1,700	34,000	—	—	8,490	5,306	39,306
Arria V SX	B3	—	—	1,729	17,290	3223	2,014	19,304
	B5	—	—	2,282	22,820	4253	2,658	25,478

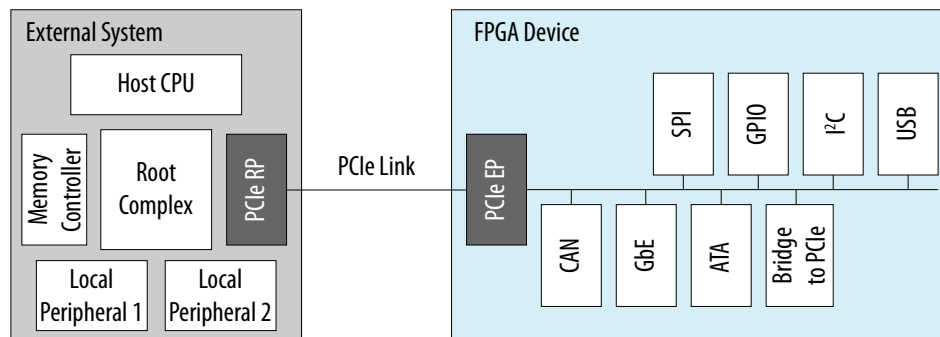
PCIe Gen1, Gen2, and Gen 3 Hard IP

Arria V devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen3, Gen 2, and Gen 1 end point and root port for up to x8 lane configuration.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

Figure 8: PCIe Multifunction for Arria V Devices



The Arria V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Arria V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Arria V device provides improved end-to-end datapath protection using ECC.

External Memory Interface

This section provides an overview of the external memory interface in Arria V devices.

Hard and Soft Memory Controllers

Arria V GX,GT, SX, and ST devices support up to four hard memory controllers for DDR3 and DDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Arria V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Arria V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices, QDR II+, QDR II, and DDR II+ SRAM devices, and RLDRAM II devices for maximum flexibility.

Note: DDR3 SDRAM leveling is supported only in Arria V GZ devices.

External Memory Performance

Table 18: External Memory Interface Performance in Arria V Devices

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)	
		Arria V GX, GT, SX, and ST	Arria V GX, GT, SX, and ST	Arria V GZ
DDR3 SDRAM	1.5	533	667	800
	1.35	533	600	800
DDR2 SDRAM	1.8	400	400	400
LPDDR2 SDRAM	1.2	—	400	—
RLDRAM 3	1.2	—	—	667
RLDRAM II	1.8	—	400	533
	1.5	—	400	533
QDR II+ SRAM	1.8	—	400	500
	1.5	—	400	500
QDR II SRAM	1.8	—	400	333
	1.5	—	400	333
DDR II+ SRAM ⁽¹²⁾	1.8	—	400	—
	1.5	—	400	—

Related Information

[External Memory Interface Spec Estimator](#)

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 19: HPS External Memory Interface Performance

The hard processor system (HPS) is available in Arria V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	533
	1.35	533
LPDDR2 SDRAM	1.2	333

⁽¹²⁾ Not available as Altera® IP.

Related Information

[External Memory Interface Spec Estimator](#)

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Arria V devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at less than 170 mW
- 10 Gbps transceivers at less than 165 mW
- 6 Gbps transceivers at less than 105 mW

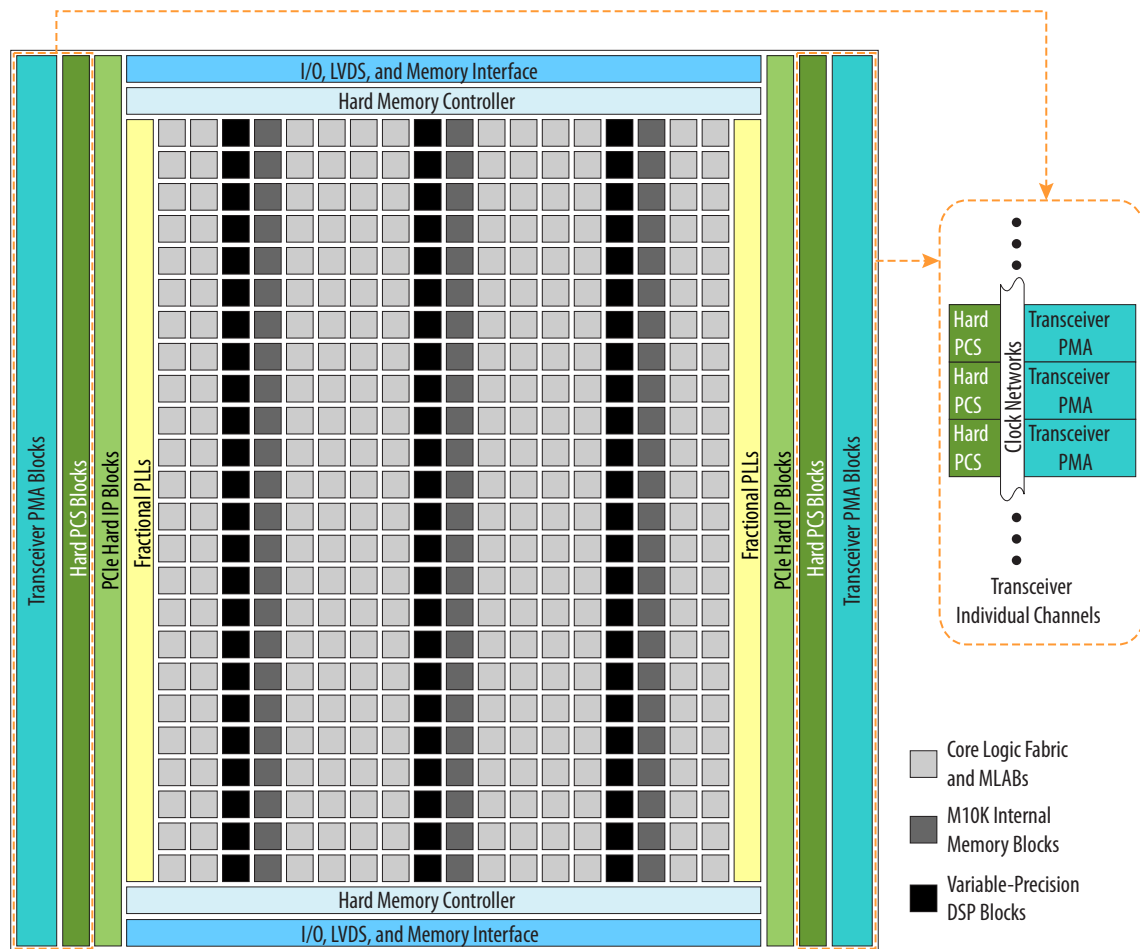
Arria V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left and right outer edges of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

The following figures are graphical representations of a top view of the silicon die, which corresponds to a reverse view for flip chip packages. Different Arria V devices may have different floorplans than the ones shown in the figures.

Figure 9: Device Chip Overview for Arria V GX and GT Devices



PCS Support ⁽¹³⁾	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
PCIe Gen1 (x1, x2, x4, x8)	2.5 and 5.0	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder PIPE 2.0 interface to the core logic 	<ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO Rate match FIFO PIPE 2.0 interface to the core logic
PCIe Gen2 ⁽¹⁴⁾ (x1, x2, x4)			
GbE	1.25	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder 	<ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO Rate match FIFO
XAUI ⁽¹⁵⁾	3.125	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder XAUI state machine for bonding four channels 	<ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO XAUI state machine for realigning four channels Deskew FIFO circuitry
SDI	0.27 ⁽¹⁶⁾ , 1.485, 2.97	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 	<ul style="list-style-type: none"> Byte deserializer Phase compensation FIFO
GPON ⁽¹⁷⁾	1.25 and 2.5		
CPRI ⁽¹⁸⁾	0.6144 to 6.144	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder TX deterministic latency 	<ul style="list-style-type: none"> Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO RX deterministic latency

⁽¹³⁾ Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

⁽¹⁴⁾ PCIe Gen2 is supported only through the PCIe hard IP.

⁽¹⁵⁾ XAUI is supported through the soft PCS.

⁽¹⁶⁾ The 0.27 Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

⁽¹⁷⁾ The GPON standard does not support burst mode.

⁽¹⁸⁾ CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through the soft PCS.

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
40GBASE-R Ethernet	4 x 10.3125	<ul style="list-style-type: none"> TX FIFO 64B/66B encoder Scrambler Alignment marker insertion Gearbox Block stripper 	<ul style="list-style-type: none"> RX FIFO 64B/66B decoder Descrambler Lane reorder Deskew Alignment marker lock Block synchronization Gear box Destripper
100GBASE-R Ethernet	10 x 10.3125		
40G and 100G OTN	(4 +1) x 11.3	<ul style="list-style-type: none"> TX FIFO Channel bonding Byte serializer 	<ul style="list-style-type: none"> RX FIFO Lane deskew Byte deserializer
	(10 +1) x 11.3		
GbE	1.25	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding GbE state machine 	<ul style="list-style-type: none"> Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer Byte ordering GbE state machine
XAUI	3.125 to 4.25	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding XAUI state machine for bonding four channels 	<ul style="list-style-type: none"> Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer Byte ordering XAUI state machine for realigning four channels
SRIO	1.25 to 6.25	<ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Bit-slip Channel bonding SRIO V2.1-compliant x2 and x4 channel bonding 	<ul style="list-style-type: none"> Word aligner Deskew FIFO Rate match FIFO 8B/10B decoder Byte deserializer Byte ordering SRIO V2.1-compliant x2 and x4 deskew state machine

SoC with HPS

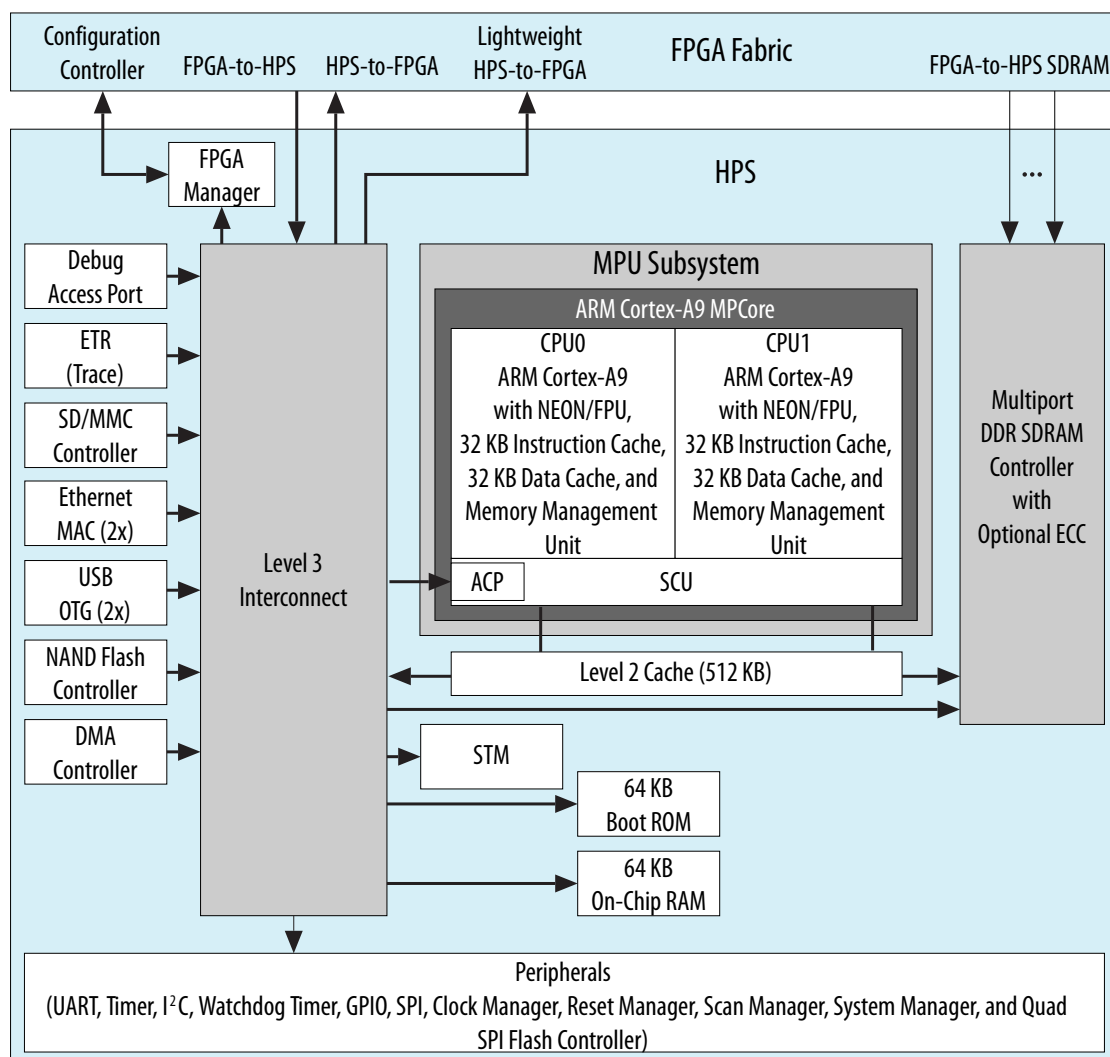
Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

HPS Features

The HPS consists of a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

Figure 12: HPS with Dual-Core ARM Cortex-A9 MPCore Processor



Partial Reconfiguration

Note: Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Quartus Prime design software. With the Altera solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Table 23: Configuration Modes and Features of Arria V Devices

Arria V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V⁽¹⁹⁾ programming voltages and several configuration modes.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration ⁽²⁰⁾	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—

⁽¹⁹⁾ Arria V GZ does not support 3.3 V.

⁽²⁰⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration ⁽²⁰⁾	Remote System Update
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes ⁽²¹⁾	
	32 bits ⁽²²⁾	100	—	Yes	Yes	—	
CvP (PCIe)	x1, x2, x4, and x8 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—
Configuration via HPS	16 bits	125	—	Yes	Yes	Yes ⁽²¹⁾	Parallel flash loader
	32 bits	100	—	Yes	Yes	—	

Instead of using an external flash or ROM, you can configure the Arria V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Arria V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

Note: Although Arria V GZ devices support PCIe Gen3, you can use only PCIe Gen1 and PCIe Gen2 for CvP configuration scheme.

Related Information

[Configuration via Protocol \(CvP\) Implementation in Altera FPGAs User Guide](#)

Provides more information about CvP.

Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Arria V devices consume less power than previous generation Arria V FPGAs:

- Total device core power consumption—less by up to 50%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Arria V devices contain several hard IP blocks, including PCIe Gen1, Gen2, and Gen3, GbE, SRIO, GPON, and CPRI protocols, that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

⁽²⁰⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

⁽²¹⁾ Supported at a maximum clock rate of 62.5 MHz.

⁽²²⁾ Arria V GZ only

Document Revision History

Date	Version	Changes
December 2015	2015.12.21	<ul style="list-style-type: none"> Updated RoHS and optional suffix information in sample ordering code and available options diagrams for Arria V GX and GT devices. Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.
January 2015	2015.01.23	<ul style="list-style-type: none"> Updated package dimension for Arria V GZ H780 package from 29 mm to 33 mm. Updated dual-core ARM Cortex-A9 MPCore processor maximum frequency from 800 MHz to 1.05 GHz.
December 2013	2013.12.26	<ul style="list-style-type: none"> 10-Gbps Ethernet (10GbE) PCS and Interlaken PCS are for Arria V GZ only. Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. Added link to Altera Product Selector for each device variant. Added leaded package options. Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F896 package from 170 to 250. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1152 package from 350 to 385. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1517 package from 528 to 540. Corrected LVDS Transmitter for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 devices from 121 to 120. Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance. Added x2 for PCIe Gen3, Gen 2, and Gen 1.
August 2013	2013.08.19	<ul style="list-style-type: none"> Removed the note about the PCIe hard IP on the right side of the device in the F896 package of the Arria V GX variant. These devices do not have PCIe hard IP on the right side. Added transceiver speed grade 6 to the available options of the Arria V SX variant. Corrected the maximum LVDS transmitter channel counts for the Arria V GX A1 and A3 devices from 68 to 67. Corrected the maximum FPGA GPIO count for Arria V ST D5 devices from 540 to 528.

Date	Version	Changes
June 2013	2013.06.03	<ul style="list-style-type: none">Removed statements about contacting Altera for SFF-8431 compliance requirements. Refer to the Transceiver Architecture in Arria V Devices chapter for the requirements.
May 2013	2013.05.06	<ul style="list-style-type: none">Moved all links to the Related Information section of respective topics for easy reference.Added link to the known document issues in the Knowledge Base.Updated the available options, maximum resource counts, and per package information for the Arria V SX and ST device variants.Updated the variable DSP multipliers counts for the Arria V SX and ST device variants.Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature.Added footnote to clarify that MLAB 64 bits depth is available only for Arria V GZ devices.Updated description about power-up sequence requirement for device migration to improve clarity.
January 2013	2013.01.11	<ul style="list-style-type: none">Added the L optional suffix to the Arria V GZ ordering code for the – I3 speed grade.Added a note about the power-up sequence requirement if you plan to migrate your design from the Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices.
November 2012	2012.11.19	<ul style="list-style-type: none">Updated the summary of features.Updated Arria V GZ information regarding 3.3 V I/O support.Removed Arria V GZ engineering sample ordering code.Updated the maximum resource counts for Arria V GX and GZ.Updated Arria V ST ordering codes for transceiver count.Updated transceiver counts for Arria V ST packages.Added simplified floorplan diagrams for Arria V GZ, SX, and ST.Added FPP x32 configuration mode for Arria V GZ only.Updated CvP (PCIe) remote system update support information.Added HPS external memory performance information.Updated template.
October 2012	3.0	<ul style="list-style-type: none">Added Arria V GZ information.Updated Table 1, Table 2, Table 3, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, and Table 21.Added the “Arria V GZ” section.Added Table 8, Table 9 and Table 22.